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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	832
Number of Logic Elements/Cells	6656
Total RAM Bits	65536
Number of I/O	424
Number of Gates	342000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	600-BGA
Supplier Device Package	600-BGA (45x45)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epf10k130ebc600-1">https://www.e-xfl.com/product-detail/intel/epf10k130ebc600-1</a>

**Table 5. FLEX 10KE Performance**

Application	Resources Used		Performance			Units
	LEs	EABs	-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	
16-bit loadable counter	16	0	285	250	200	MHz
16-bit accumulator	16	0	285	250	200	MHz
16-to-1 multiplexer (1)	10	0	3.5	4.9	7.0	ns
16-bit multiplier with 3-stage pipeline (2)	592	0	156	131	93	MHz
256 × 16 RAM read cycle speed (2)	0	1	196	154	118	MHz
256 × 16 RAM write cycle speed (2)	0	1	185	143	106	MHz

**Notes:**

- (1) This application uses combinatorial inputs and outputs.  
 (2) This application uses registered inputs and outputs.

Table 6 shows FLEX 10KE performance for more complex designs. These designs are available as Altera MegaCore® functions.

**Table 6. FLEX 10KE Performance for Complex Designs**

Application	LEs Used	Performance			Units
		-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	
8-bit, 16-tap parallel finite impulse response (FIR) filter	597	192	156	116	MSPS
8-bit, 512-point fast Fourier transform (FFT) function	1,854	23.4	28.7	38.9	μs (1)
		113	92	68	MHz
a16450 universal asynchronous receiver/transmitter (UART)	342	36	28	20.5	MHz

**Note:**

- (1) These values are for calculation time. Calculation time = number of clocks required /  $f_{\max}$ . Number of clocks required = ceiling  $[\log_2 (\text{points})/2] \times [\text{points} + 14 + \text{ceiling}]$



For more information on FLEX device configuration, see the following documents:

- *Configuration Devices for APEX & FLEX Devices Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *MasterBlaster Download Cable Data Sheet*
- *Application Note 116 (Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices)*

FLEX 10KE devices are supported by the Altera development systems, which are integrated packages that offer schematic, text (including AHDL), and waveform design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, and device configuration. The Altera software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The Altera software works easily with common gate array EDA tools for synthesis and simulation. For example, the Altera software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the Altera software contains EDA libraries that use device-specific features such as carry chains, which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the Altera development system includes DesignWare functions that are optimized for the FLEX 10KE architecture.

The Altera development system runs on Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800.



See the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet* for more information.

EABs provide flexible options for driving and controlling clock signals. Different clocks and clock enables can be used for reading and writing to the EAB. Registers can be independently inserted on the data input, EAB output, write address, write enable signals, read address, and read enable signals. The global signals and the EAB local interconnect can drive write enable, read enable, and clock enable signals. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control write enable, read enable, clear, clock, and clock enable signals.

An EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs (see [Figures 2 and 4](#)). The column interconnect, which is adjacent to the EAB, has twice as many channels as other columns in the device.

## Logic Array Block

An LAB consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure to the FLEX 10KE architecture, facilitating efficient routing with optimum device utilization and high performance (see [Figure 7](#)).

Figure 9 shows how an  $n$ -bit full adder can be implemented in  $n + 1$  LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for an accumulator function. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal.

Figure 9. FLEX 10KE Carry Chain Operation ( $n$ -Bit Full Adder)

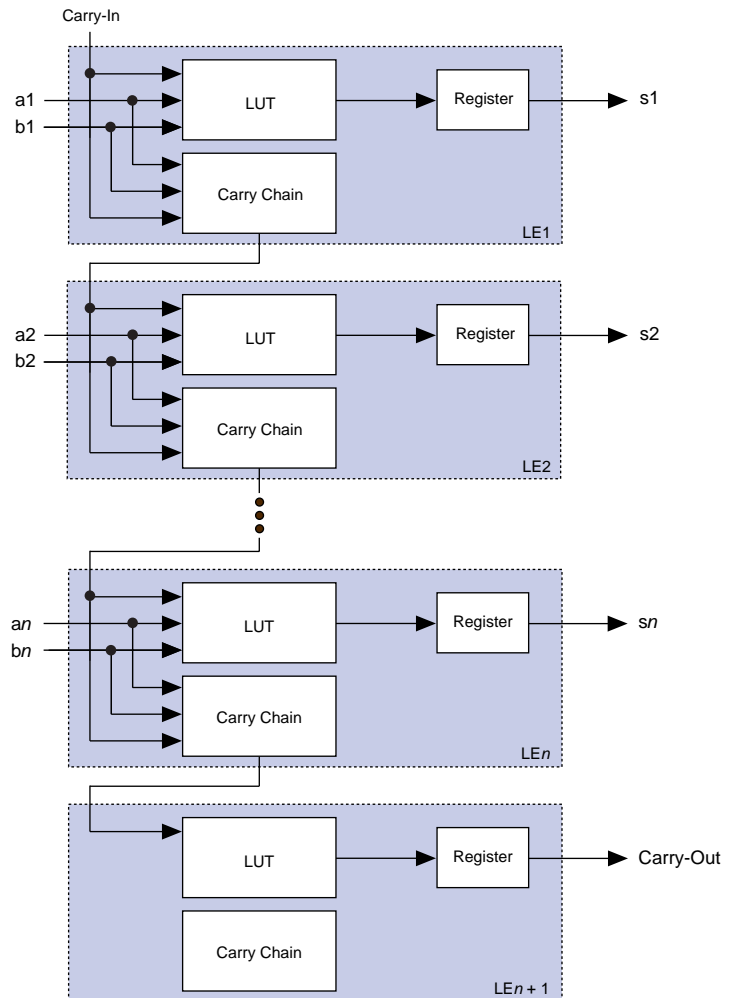
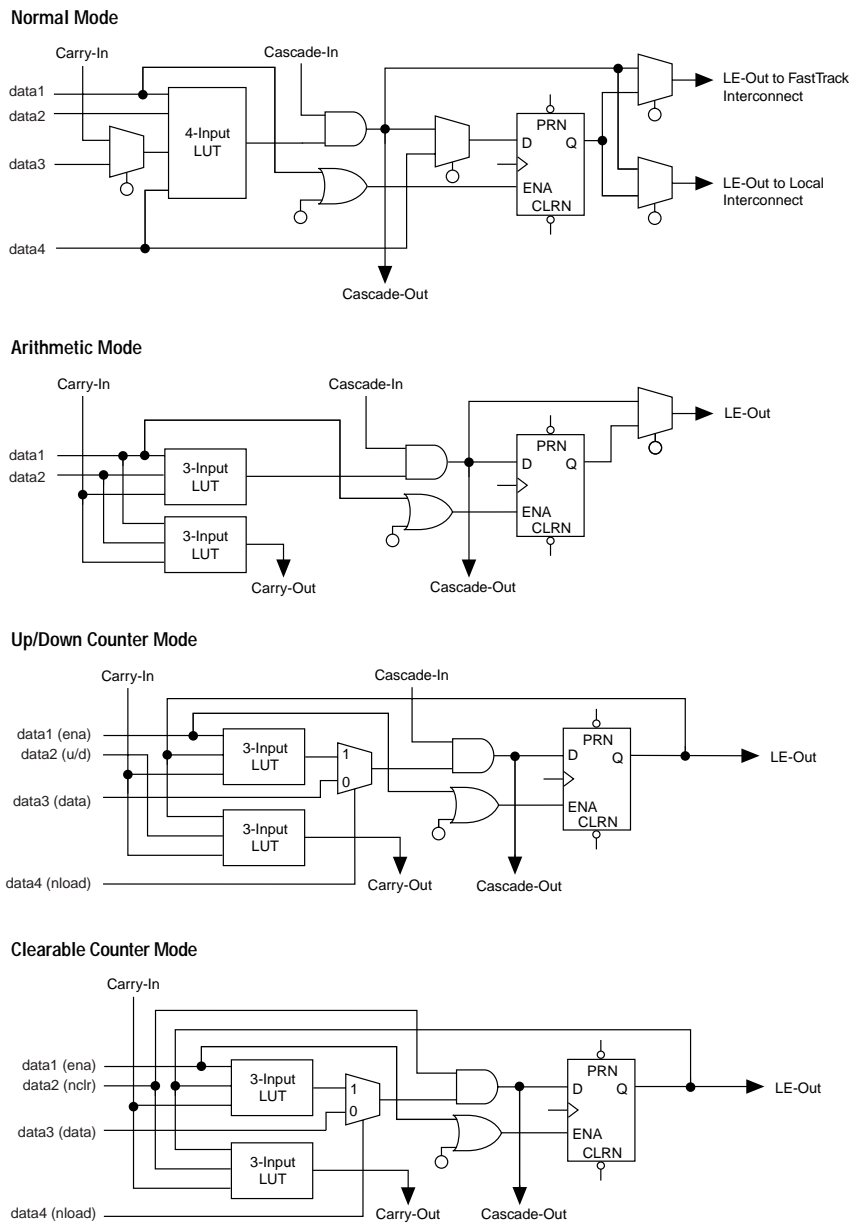


Figure 11 shows the LE operating modes.

Figure 11. FLEX 10KE LE Operating Modes



## FastTrack Interconnect Routing Structure

In the FLEX 10KE architecture, connections between LEs, EABs, and device I/O pins are provided by the FastTrack Interconnect routing structure, which is a series of continuous horizontal and vertical routing channels that traverses the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect routing structure consists of row and column interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect. The row interconnect can drive I/O pins and feed other LABs in the row. The column interconnect routes signals between rows and can drive I/O pins.

Row channels drive into the LAB or EAB local interconnect. The row signal is buffered at every LAB or EAB to reduce the effect of fan-out on delay. A row channel can be driven by an LE or by one of three column channels. These four signals feed dual 4-to-1 multiplexers that connect to two specific row channels. These multiplexers, which are connected to each LE, allow column channels to drive row channels even when all eight LEs in a LAB drive the row interconnect.

Each column of LABs or EABs is served by a dedicated column interconnect. The column interconnect that serves the EABs has twice as many channels as other column interconnects. The column interconnect can then drive I/O pins or another row's interconnect to route the signals to other LABs or EABs in the device. A signal from the column interconnect, which can be either the output of a LE or an input from an I/O pin, must be routed to the row interconnect before it can enter a LAB or EAB. Each row channel that is driven by an IOE or EAB can drive one specific column channel.

Access to row and column channels can be switched between LEs in adjacent pairs of LABs. For example, a LE in one LAB can drive the row and column channels normally driven by a particular LE in the adjacent LAB in the same row, and vice versa. This flexibility enables routing resources to be used more efficiently (see [Figure 13](#)).

Figure 13. FLEX 10KE LAB Connections to Row & Column Interconnect

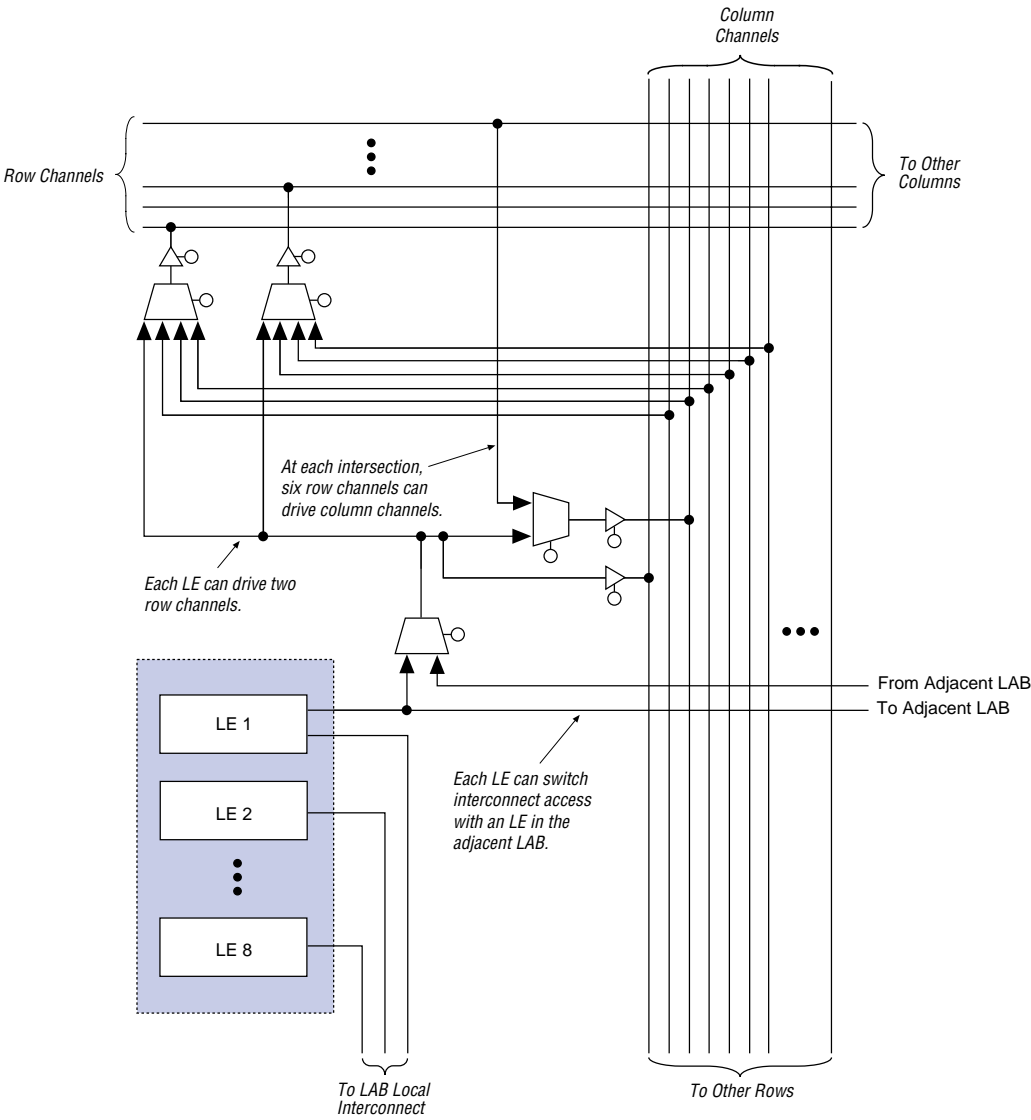
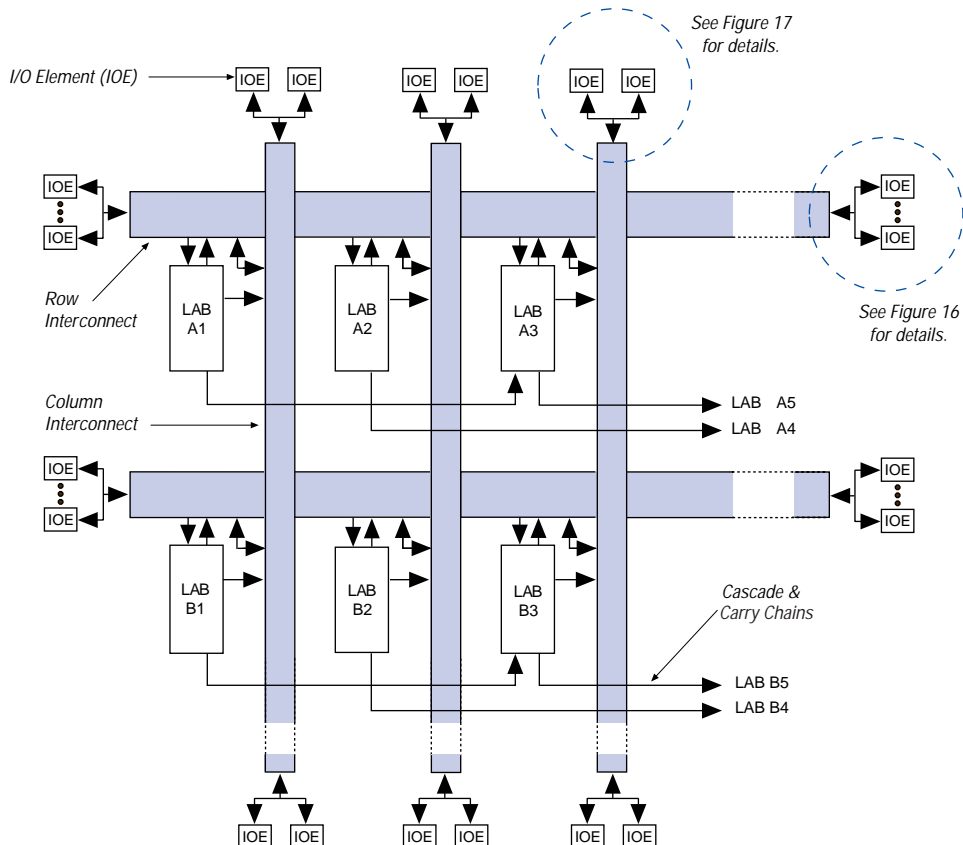


Figure 14. FLEX 10KE Interconnect Resources



## I/O Element

An IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. In some cases, using an LE register for an input register will result in a faster setup time than using an IOE register. IOEs can be used as input, output, or bidirectional pins. For bidirectional registered I/O implementation, the output register should be in the IOE, and the data input and output enable registers should be LE registers placed adjacent to the bidirectional pin. The Altera Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. [Figure 15](#) shows the bidirectional I/O registers.

When dedicated inputs drive non-inverted and inverted peripheral clears, clock enables, and output enables, two signals on the peripheral control bus will be used.

Tables 8 and 9 list the sources for each peripheral control signal, and show how the output enable, clock enable, clock, and clear signals share 12 peripheral control signals. The tables also show the rows that can drive global signals.

*Table 8. Peripheral Bus Sources for EPF10K30E, EPF10K50E & EPF10K50S Devices*

Peripheral Control Signal	EPF10K30E	EPF10K50E EPF10K50S
OE0	Row A	Row A
OE1	Row B	Row B
OE2	Row C	Row D
OE3	Row D	Row F
OE4	Row E	Row H
OE5	Row F	Row J
CLKENA0/CLK0/GLOBAL0	Row A	Row A
CLKENA1/OE6/GLOBAL1	Row B	Row C
CLKENA2/CLR0	Row C	Row E
CLKENA3/OE7/GLOBAL2	Row D	Row G
CLKENA4/CLR1	Row E	Row I
CLKENA5/CLK1/GLOBAL3	Row F	Row J

## SameFrame Pin-Outs

FLEX 10KE devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EPF10K30E device in a 256-pin FineLine BGA package to an EPF10K200S device in a 672-pin FineLine BGA package.

The Altera software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software generates pin-outs describing how to lay out a board to take advantage of this migration (see [Figure 18](#)).

*Figure 18. SameFrame Pin-Out Example*

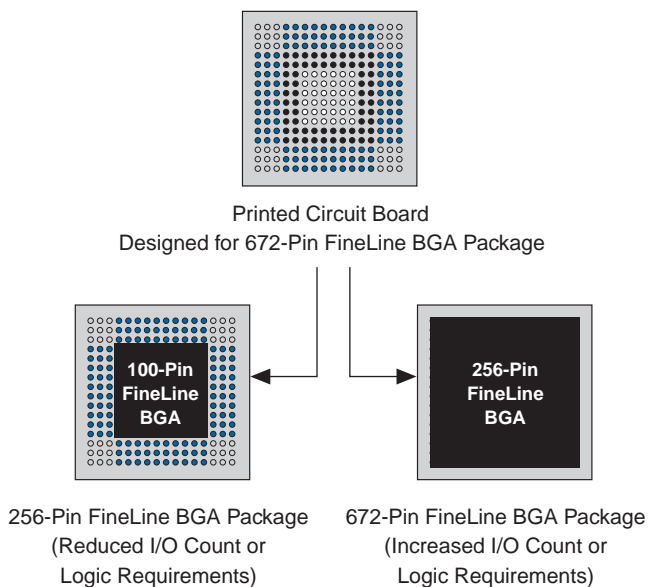


Figure 22 shows the required relationship between  $V_{CCIO}$  and  $V_{CCINT}$  for 3.3-V PCI compliance.

Figure 22. Relationship between  $V_{CCIO}$  &  $V_{CCINT}$  for 3.3-V PCI Compliance

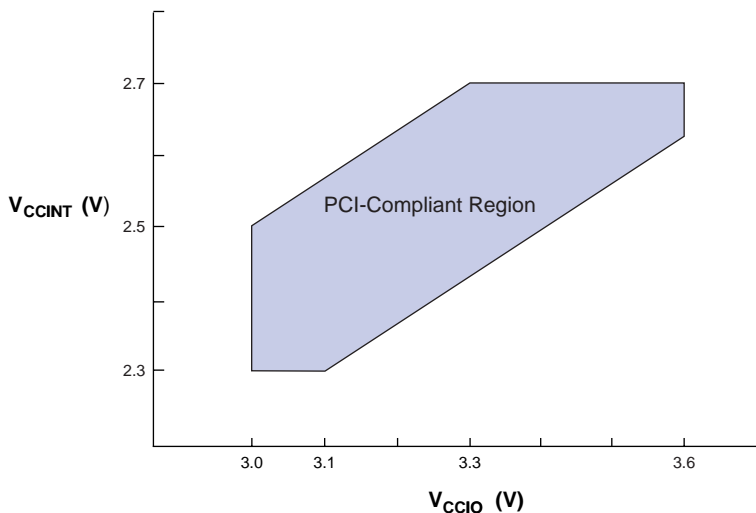


Figure 23 shows the typical output drive characteristics of FLEX 10KE devices with 3.3-V and 2.5-V  $V_{CCIO}$ . The output driver is compliant to the 3.3-V **PCI Local Bus Specification, Revision 2.2** (when  $V_{CCIO}$  pins are connected to 3.3 V). FLEX 10KE devices with a -1 speed grade also comply with the drive strength requirements of the **PCI Local Bus Specification, Revision 2.2** (when  $V_{CCINT}$  pins are powered with a minimum supply of 2.375 V, and  $V_{CCIO}$  pins are connected to 3.3 V). Therefore, these devices can be used in open 5.0-V PCI systems.

Figure 25. FLEX 10KE Device LE Timing Model

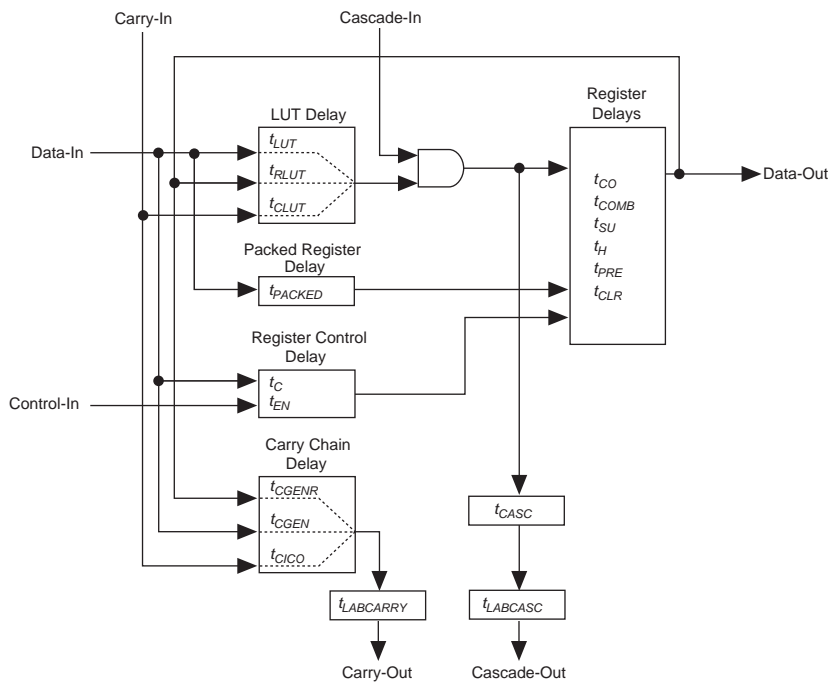


Table 43. EPF10K50E External Timing Parameters Notes (1), (2)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{DRR}}$		8.5		10.0		13.5	ns
$t_{\text{INSU}}$	2.7		3.2		4.3		ns
$t_{\text{INH}}$	0.0		0.0		0.0		ns
$t_{\text{OUTCO}}$	2.0	4.5	2.0	5.2	2.0	7.3	ns
$t_{\text{PCISU}}$	3.0		4.2		-		ns
$t_{\text{PCIH}}$	0.0		0.0		-		ns
$t_{\text{PCICO}}$	2.0	6.0	2.0	7.7	-	-	ns

Table 44. EPF10K50E External Bidirectional Timing Parameters Notes (1), (2)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	2.7		3.2		4.3		ns
$t_{\text{INHBIDIR}}$	0.0		0.0		0.0		ns
$t_{\text{OUTCOBIDIR}}$	2.0	4.5	2.0	5.2	2.0	7.3	ns
$t_{\text{XZBIDIR}}$		6.8		7.8		10.1	ns
$t_{\text{ZXBIDIR}}$		6.8		7.8		10.1	ns

**Notes to tables:**

- (1) All timing parameters are described in Tables 24 through 30 in this data sheet.  
 (2) These parameters are specified by characterization.

Tables 45 through 51 show EPF10K100E device internal and external timing parameters.

Table 45. EPF10K100E Device LE Timing Microparameters Note (1)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{LUT}}$		0.7		1.0		1.5	ns
$t_{\text{CLUT}}$		0.5		0.7		0.9	ns
$t_{\text{RLUT}}$		0.6		0.8		1.1	ns
$t_{\text{PACKED}}$		0.3		0.4		0.5	ns
$t_{\text{EN}}$		0.2		0.3		0.3	ns
$t_{\text{CICO}}$		0.1		0.1		0.2	ns
$t_{\text{CGEN}}$		0.4		0.5		0.7	ns

Table 48. EPF10K100E Device EAB Internal Timing Macroparameters (Part 2 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABWCOMB}$	5.9		7.7		10.3		ns
$t_{EABWCREG}$	5.4		7.0		9.4		ns
$t_{EABDD}$		3.4		4.5		5.9	ns
$t_{EABDATACO}$		0.5		0.7		0.8	ns
$t_{EABDATASU}$	0.8		1.0		1.4		ns
$t_{EABDATAH}$	0.1		0.1		0.2		ns
$t_{EABWESU}$	1.1		1.4		1.9		ns
$t_{EABWEH}$	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.0		1.3		1.7		ns
$t_{EABWDH}$	0.2		0.2		0.3		ns
$t_{EABWASU}$	4.1		5.2		6.8		ns
$t_{EABWAH}$	0.0		0.0		0.0		ns
$t_{EABWO}$		3.4		4.5		5.9	ns

Table 49. EPF10K100E Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		3.1		3.6		4.4	ns
$t_{DIN2LE}$		0.3		0.4		0.5	ns
$t_{DIN2DATA}$		1.6		1.8		2.0	ns
$t_{DCLK2IOE}$		0.8		1.1		1.4	ns
$t_{DCLK2LE}$		0.3		0.4		0.5	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		1.5		2.5		3.4	ns
$t_{SAMECOLUMN}$		0.4		1.0		1.6	ns
$t_{DIFFROW}$		1.9		3.5		5.0	ns
$t_{TROWROWS}$		3.4		6.0		8.4	ns
$t_{LEPERIPH}$		4.3		5.4		6.5	ns
$t_{LABCARRY}$		0.5		0.7		0.9	ns
$t_{LABCASC}$		0.8		1.0		1.4	ns

Tables 52 through 58 show EPF10K130E device internal and external timing parameters.

**Table 52. EPF10K130E Device LE Timing Microparameters** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{LUT}$		0.6		0.9		1.3	ns
$t_{CLUT}$		0.6		0.8		1.0	ns
$t_{RLUT}$		0.7		0.9		0.2	ns
$t_{PACKED}$		0.3		0.5		0.6	ns
$t_{EN}$		0.2		0.3		0.4	ns
$t_{CICO}$		0.1		0.1		0.2	ns
$t_{CGEN}$		0.4		0.6		0.8	ns
$t_{CGENR}$		0.1		0.1		0.2	ns
$t_{CASC}$		0.6		0.9		1.2	ns
$t_C$		0.3		0.5		0.6	ns
$t_{CO}$		0.5		0.7		0.8	ns
$t_{COMB}$		0.3		0.5		0.6	ns
$t_{SU}$	0.5		0.7		0.8		ns
$t_H$	0.6		0.7		1.0		ns
$t_{PRE}$		0.9		1.2		1.6	ns
$t_{CLR}$		0.9		1.2		1.6	ns
$t_{CH}$	1.5		1.5		2.5		ns
$t_{CL}$	1.5		1.5		2.5		ns

**Table 53. EPF10K130E Device IOE Timing Microparameters** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{IOD}$		1.3		1.5		2.0	ns
$t_{IOC}$		0.0		0.0		0.0	ns
$t_{IOCO}$		0.6		0.8		1.0	ns
$t_{IOCOMB}$		0.6		0.8		1.0	ns
$t_{IOSU}$	1.0		1.2		1.6		ns
$t_{IOH}$	0.9		0.9		1.4		ns
$t_{IOCLR}$		0.6		0.8		1.0	ns
$t_{OD1}$		2.8		4.1		5.5	ns
$t_{OD2}$		2.8		4.1		5.5	ns

Table 68. EPF10K50S Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.7		2.4		3.2	ns
$t_{EABDATA2}$		0.4		0.6		0.8	ns
$t_{EABWE1}$		1.0		1.4		1.9	ns
$t_{EABWE2}$		0.0		0.0		0.0	ns
$t_{EABRE1}$		0.0		0.0		0.0	
$t_{EABRE2}$		0.4		0.6		0.8	
$t_{EABCLK}$		0.0		0.0		0.0	ns
$t_{EABCO}$		0.8		1.1		1.5	ns
$t_{EABYPASS}$		0.0		0.0		0.0	ns
$t_{EABSU}$	0.7		1.0		1.3		ns
$t_{EABH}$	0.4		0.6		0.8		ns
$t_{EABCLR}$	0.8		1.1		1.5		
$t_{AA}$		2.0		2.8		3.8	ns
$t_{WP}$	2.0		2.8		3.8		ns
$t_{RP}$	1.0		1.4		1.9		
$t_{WDSU}$	0.5		0.7		0.9		ns
$t_{WDH}$	0.1		0.1		0.2		ns
$t_{WASU}$	1.0		1.4		1.9		ns
$t_{WAH}$	1.5		2.1		2.9		ns
$t_{RASU}$	1.5		2.1		2.8		
$t_{RAH}$	0.1		0.1		0.2		
$t_{WO}$		2.1		2.9		4.0	ns
$t_{DD}$		2.1		2.9		4.0	ns
$t_{EABOUT}$		0.0		0.0		0.0	ns
$t_{EABCH}$	1.5		2.0		2.5		ns
$t_{EABCL}$	1.5		2.0		2.5		ns

Table 69. EPF10K50S Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABAA}$		3.7		5.2		7.0	ns
$t_{EABRCCOMB}$	3.7		5.2		7.0		ns
$t_{EABRCREG}$	3.5		4.9		6.6		ns
$t_{EABWP}$	2.0		2.8		3.8		ns
$t_{EABWCCOMB}$	4.5		6.3		8.6		ns
$t_{EABWCREG}$	5.6		7.8		10.6		ns
$t_{EABDD}$		3.8		5.3		7.2	ns
$t_{EABDATACO}$		0.8		1.1		1.5	ns
$t_{EABDATASU}$	1.1		1.6		2.1		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	0.7		1.0		1.3		ns
$t_{EABWEH}$	0.4		0.6		0.8		ns
$t_{EABWDSU}$	1.2		1.7		2.2		ns
$t_{EABWDH}$	0.0		0.0		0.0		ns
$t_{EABWASU}$	1.6		2.3		3.0		ns
$t_{EABWAH}$	0.9		1.2		1.8		ns
$t_{EABWO}$		3.1		4.3		5.9	ns

Table 70. EPF10K50S Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		3.1		3.7		4.6	ns
$t_{DIN2LE}$		1.7		2.1		2.7	ns
$t_{DIN2DATA}$		2.7		3.1		5.1	ns
$t_{DCLK2IOE}$		1.6		1.9		2.6	ns
$t_{DCLK2LE}$		1.7		2.1		2.7	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		1.5		1.7		2.4	ns
$t_{SAMECOLUMN}$		1.0		1.3		2.1	ns
$t_{DIFFROW}$		2.5		3.0		4.5	ns
$t_{TWOROWS}$		4.0		4.7		6.9	ns
$t_{LEPERIPH}$		2.6		2.9		3.4	ns
$t_{LABCARRY}$		0.1		0.2		0.2	ns
$t_{LABCASC}$		0.8		1.0		1.3	ns

# Power Consumption

The supply power (P) for FLEX 10KE devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = (I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC} + P_{IO}$$

The  $I_{CCACTIVE}$  value depends on the switching frequency and the application logic. This value is calculated based on the amount of current that each LE typically consumes. The  $P_{IO}$  value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in [Application Note 74 \(Evaluating Power for Altera Devices\)](#).

Compared to the rest of the device, the embedded array consumes a negligible amount of power. Therefore, the embedded array can be ignored when calculating supply current.

The  $I_{CCACTIVE}$  value can be calculated with the following equation:

$$I_{CCACTIVE} = K \times f_{MAX} \times N \times \text{tog}_{LC} \times \frac{\mu A}{MHz \times LE}$$

Where:

- $f_{MAX}$  = Maximum operating frequency in MHz
- $N$  = Total number of LEs used in the device
- $\text{tog}_{LC}$  = Average percent of LEs toggling at each clock (typically 12.5%)
- $K$  = Constant

**Table 80** provides the constant (K) values for FLEX 10KE devices.

Table 80. FLEX 10KE K Constant Values	
Device	K Value
EPF10K30E	4.5
EPF10K50E	4.8
EPF10K50S	4.5
EPF10K100E	4.5
EPF10K130E	4.6
EPF10K200E	4.8
EPF10K200S	4.6

This calculation provides an  $I_{CC}$  estimate based on typical conditions with no output load. The actual  $I_{CC}$  should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Additionally, the Altera software offers several features that help plan for future device migration by preventing the use of conflicting I/O pins.

*Table 81. I/O Counts for FLEX 10KA & FLEX 10KE Devices*

FLEX 10KA		FLEX 10KE	
Device	I/O Count	Device	I/O Count
EPF10K30AF256	191	EPF10K30EF256	176
EPF10K30AF484	246	EPF10K30EF484	220
EPF10K50VB356	274	EPF10K50SB356	220
EPF10K50VF484	291	EPF10K50EF484	254
EPF10K50VF484	291	EPF10K50SF484	254
EPF10K100AF484	369	EPF10K100EF484	338

## Configuration Schemes

The configuration data for a FLEX 10KE device can be loaded with one of five configuration schemes (see [Table 82](#)), chosen on the basis of the target application. An EPC1, EPC2, or EPC16 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of a FLEX 10KE device, allowing automatic configuration on system power-up.

Multiple FLEX 10KE devices can be configured in any of the five configuration schemes by connecting the configuration enable ( $\overline{nCE}$ ) and configuration enable output ( $\overline{nCEO}$ ) pins on each device. Additional FLEX 10K, FLEX 10KA, FLEX 10KE, and FLEX 6000 devices can be configured in the same serial chain.

*Table 82. Data Sources for FLEX 10KE Configuration*

Configuration Scheme	Data Source
Configuration device	EPC1, EPC2, or EPC16 configuration device
Passive serial (PS)	BitBlaster, ByteBlasterMV, or MasterBlaster download cables, or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	BitBlaster or ByteBlasterMV download cables, or microprocessor with a Jam STAPL file or JBC file



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