



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

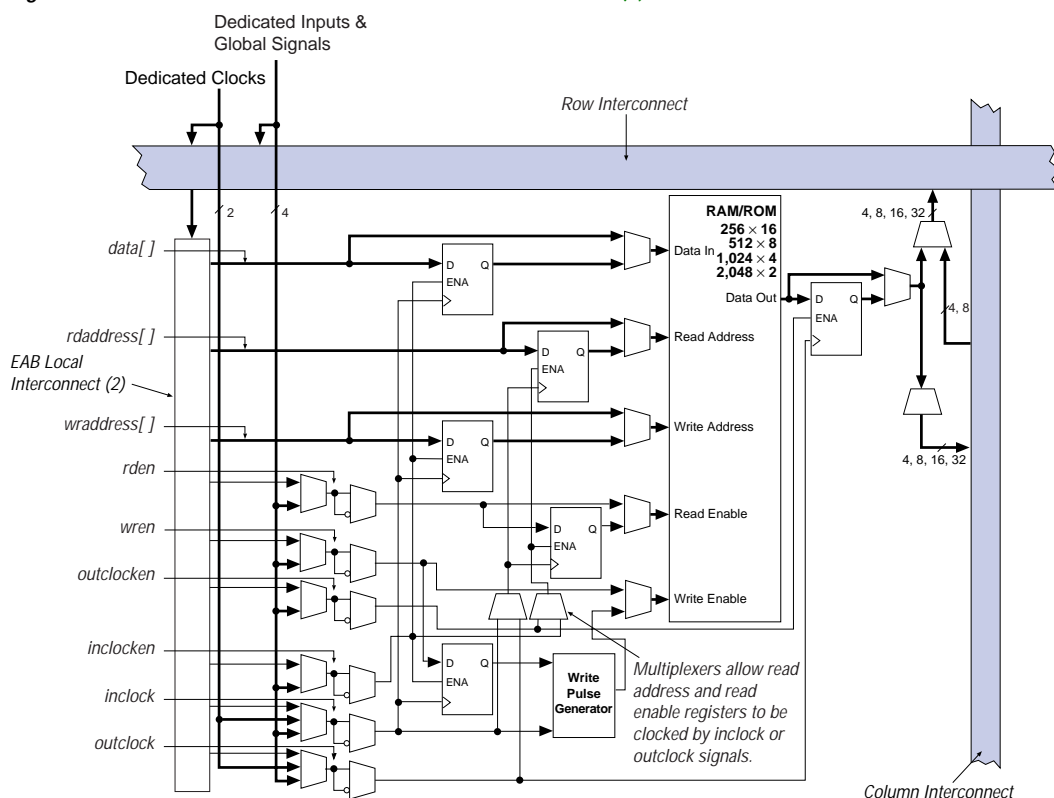
#### Details

Product Status	Obsolete
Number of LABs/CLBs	832
Number of Logic Elements/Cells	6656
Total RAM Bits	65536
Number of I/O	369
Number of Gates	342000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epf10k130efc484-1x">https://www.e-xfl.com/product-detail/intel/epf10k130efc484-1x</a>

The EAB can also be used for bidirectional, dual-port memory applications where two ports read or write simultaneously. To implement this type of dual-port memory, two EABs are used to support two simultaneous read or writes.

Alternatively, one clock and clock enable can be used to control the input registers of the EAB, while a different clock and clock enable control the output registers (see Figure 2).

Figure 2. FLEX 10KE Device in Dual-Port RAM Mode *Notes (1)*

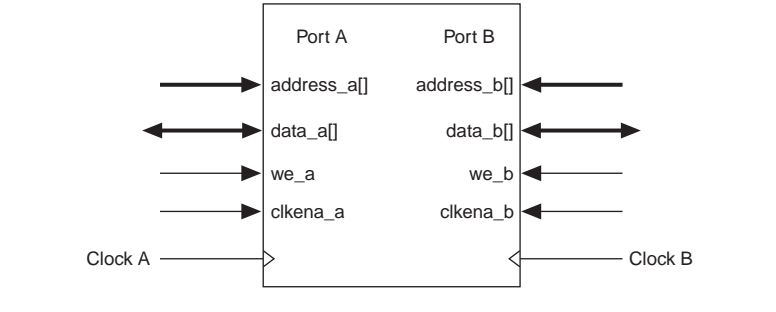


**Notes:**

- (1) All registers can be asynchronously cleared by EAB local interconnect signals, global signals, or the chip-wide reset.
- (2) EPF10K30E and EPF10K50E devices have 88 EAB local interconnect channels; EPF10K100E, EPF10K130E, and EPF10K200E devices have 104 EAB local interconnect channels.

The EAB can also use Altera megafunctions to implement dual-port RAM applications where both ports can read or write, as shown in [Figure 3](#).

Figure 3. FLEX 10KE EAB in Dual-Port RAM Mode



The FLEX 10KE EAB can be used in a single-port mode, which is useful for backward-compatibility with FLEX 10K designs (see [Figure 4](#)).

### Clearable Counter Mode

The clearable counter mode is similar to the up/down counter mode, but supports a synchronous clear instead of the up/down control. The clear function is substituted for the cascade-in signal in the up/down counter mode. Use 2 three-input LUTs: one generates the counter data, and the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer. The output of this multiplexer is ANDed with a synchronous clear signal.

### *Internal Tri-State Emulation*

Internal tri-state emulation provides internal tri-states without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable (OE) signals select which signal drives the bus. However, if multiple OE signals are active, contending signals can be driven onto the bus. Conversely, if no OE signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The Altera software automatically implements tri-state bus functionality with a multiplexer.

### *Clear & Preset Logic Control*

Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. The clear and preset control structure of the LE asynchronously loads signals into a register. Either LABCTRL1 or LABCTRL2 can control the asynchronous clear. Alternatively, the register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

During compilation, the Altera Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six modes chosen during design entry:

- Asynchronous clear
- Asynchronous preset
- Asynchronous clear and preset
- Asynchronous load with clear
- Asynchronous load with preset
- Asynchronous load without clear or preset

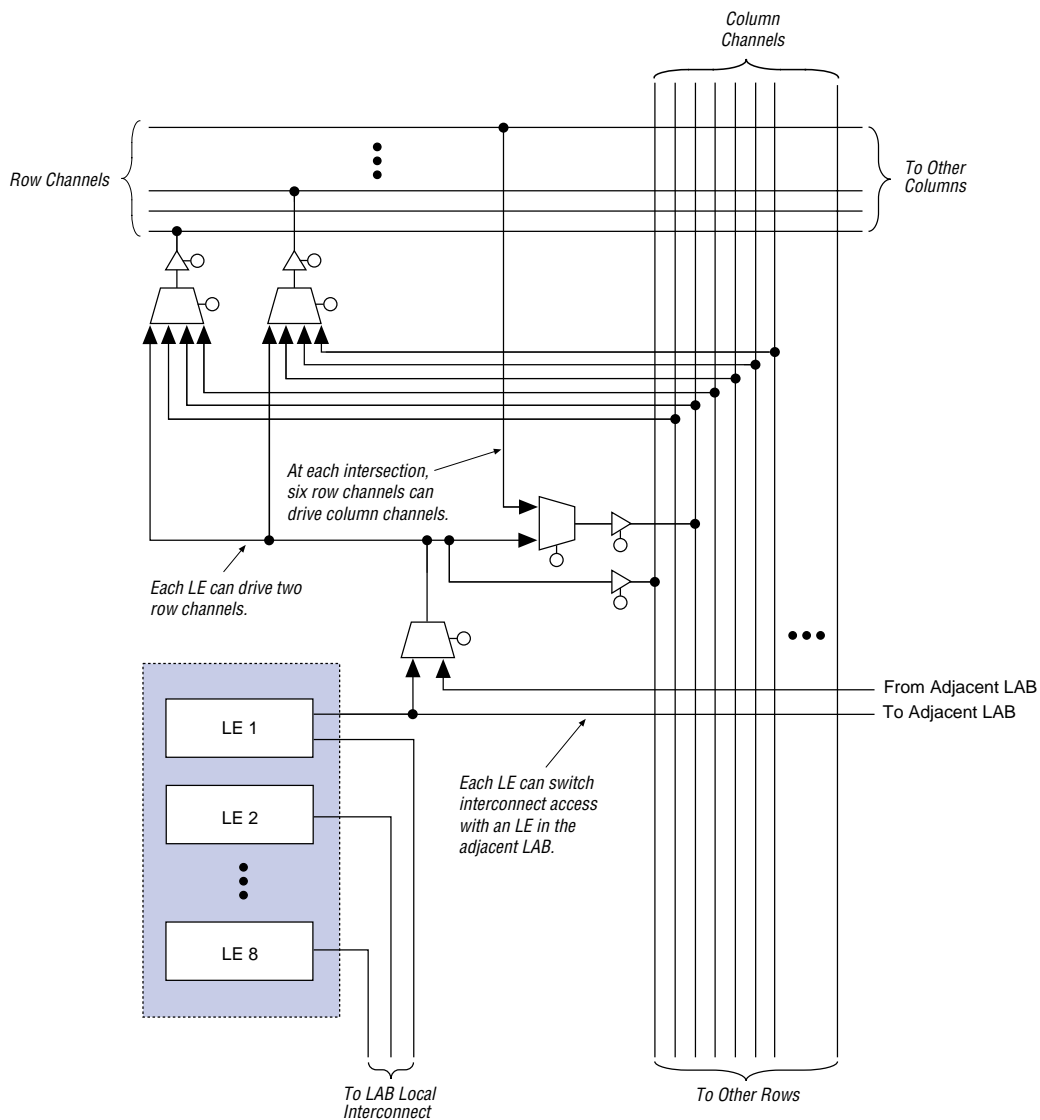
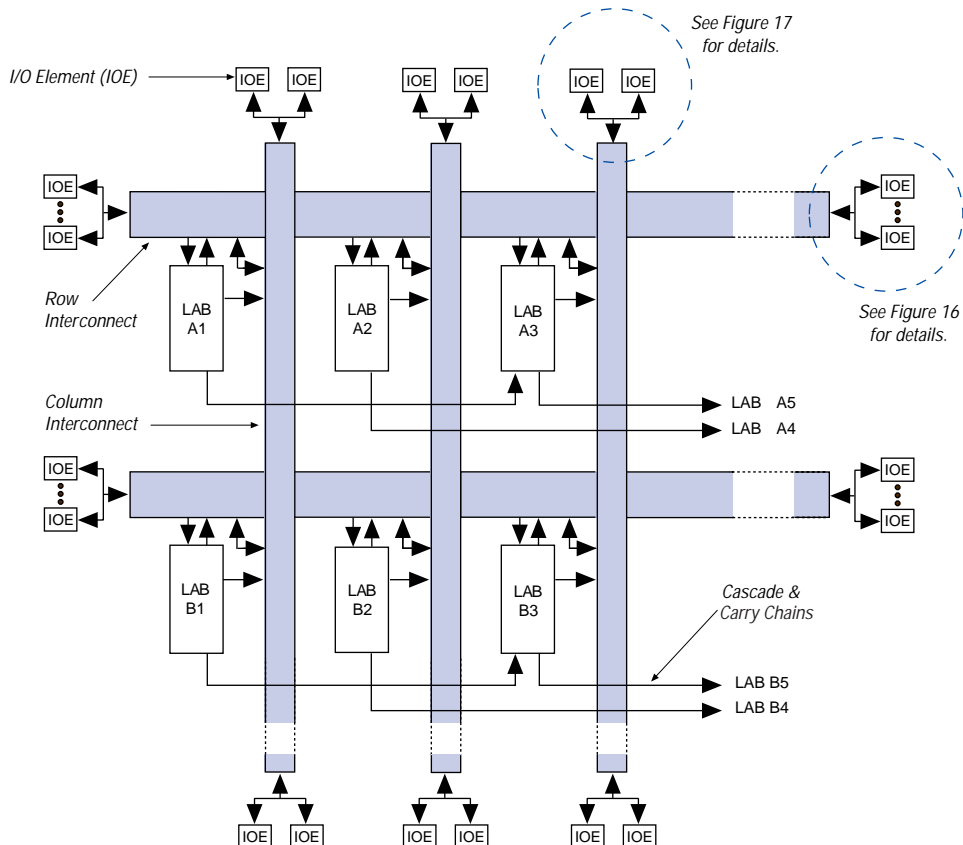


Figure 14. FLEX 10KE Interconnect Resources



## I/O Element

An IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. In some cases, using an LE register for an input register will result in a faster setup time than using an IOE register. IOEs can be used as input, output, or bidirectional pins. For bidirectional registered I/O implementation, the output register should be in the IOE, and the data input and output enable registers should be LE registers placed adjacent to the bidirectional pin. The Altera Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. [Figure 15](#) shows the bidirectional I/O registers.

On all FLEX 10KE devices (except EPF10K50E and EPF10K200E devices), the input path from the I/O pad to the FastTrack Interconnect has a programmable delay element that can be used to guarantee a zero hold time. EPF10K50S and EPF10K200S devices also support this feature. Depending on the placement of the IOE relative to what it is driving, the designer may choose to turn on the programmable delay to ensure a zero hold time or turn it off to minimize setup time. This feature is used to reduce setup time for complex pin-to-register paths (e.g., PCI designs).

Each IOE selects the clock, clear, clock enable, and output enable controls from a network of I/O control signals called the peripheral control bus. The peripheral control bus uses high-speed drivers to minimize signal skew across the device and provides up to 12 peripheral control signals that can be allocated as follows:

- Up to eight output enable signals
- Up to six clock enable signals
- Up to two clock signals
- Up to two clear signals

If more than six clock enable or eight output enable signals are required, each IOE on the device can be controlled by clock enable and output enable signals driven by specific LEs. In addition to the two clock signals available on the peripheral control bus, each IOE can use one of two dedicated clock pins. Each peripheral control signal can be driven by any of the dedicated input pins or the first LE of each LAB in a particular row. In addition, a LE in a different row can drive a column interconnect, which causes a row interconnect to drive the peripheral control signal. The chip-wide reset signal resets all IOE registers, overriding any other control signals.

When a dedicated clock pin drives IOE registers, it can be inverted for all IOEs in the device. All IOEs must use the same sense of the clock. For example, if any IOE uses the inverted clock, all IOEs must use the inverted clock and no IOE can use the non-inverted clock. However, LEs can still use the true or complement of the clock on a LAB-by-LAB basis.

The incoming signal may be inverted at the dedicated clock pin and will drive all IOEs. For the true and complement of a clock to be used to drive IOEs, drive it into both global clock pins. One global clock pin will supply the true, and the other will supply the complement.

When the true and complement of a dedicated input drives IOE clocks, two signals on the peripheral control bus are consumed, one for each sense of the clock.

*Table 9. Peripheral Bus Sources for EPF10K100E, EPF10K130E, EPF10K200E & EPF10K200S Devices*

Peripheral Control Signal	EPF10K100E	EPF10K130E	EPF10K200E EPF10K200S
OE0	Row A	Row C	Row G
OE1	Row C	Row E	Row I
OE2	Row E	Row G	Row K
OE3	Row L	Row N	Row R
OE4	Row I	Row K	Row O
OE5	Row K	Row M	Row Q
CLKENA0/CLK0/GLOBAL0	Row F	Row H	Row L
CLKENA1/OE6/GLOBAL1	Row D	Row F	Row J
CLKENA2/CLR0	Row B	Row D	Row H
CLKENA3/OE7/GLOBAL2	Row H	Row J	Row N
CLKENA4/CLR1	Row J	Row L	Row P
CLKENA5/CLK1/GLOBAL3	Row G	Row I	Row M

Signals on the peripheral control bus can also drive the four global signals, referred to as GLOBAL0 through GLOBAL3 in [Tables 8 and 9](#). An internally generated signal can drive a global signal, providing the same low-skew, low-delay characteristics as a signal driven by an input pin. An LE drives the global signal by driving a row line that drives the peripheral bus, which then drives the global signal. This feature is ideal for internally generated clear or clock signals with high fan-out. However, internally driven global signals offer no advantage over the general-purpose interconnect for routing data signals. The dedicated input pin should be driven to a known logic state (such as ground) and not be allowed to float.

The chip-wide output enable pin is an active-high pin (DEV\_OE) that can be used to tri-state all pins on the device. This option can be set in the Altera software. On EPF10K50E and EPF10K200E devices, the built-in I/O pin pull-up resistors (which are active during configuration) are active when the chip-wide output enable pin is asserted. The registers in the IOE can also be reset by the chip-wide reset pin.

### Row-to-IOE Connections

When an IOE is used as an input signal, it can drive two separate row channels. The signal is accessible by all LEs within that row. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the row channels. Up to eight IOEs connect to each side of each row channel (see Figure 16).

**Figure 16. FLEX 10KE Row-to-IOE Connections**

The values for  $m$  and  $n$  are provided in Table 10.

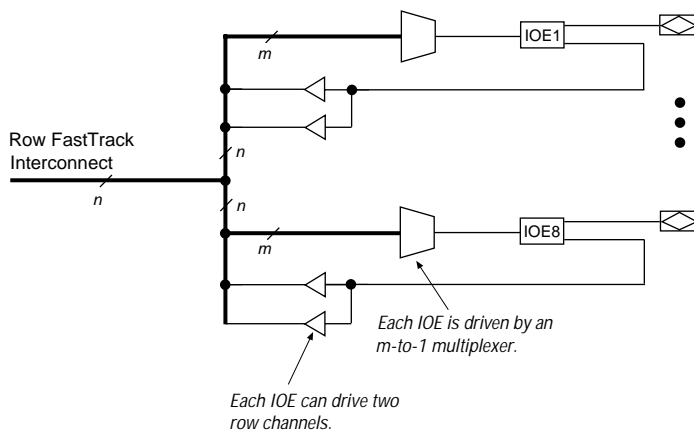


Table 10 lists the FLEX 10KE row-to-IOE interconnect resources.

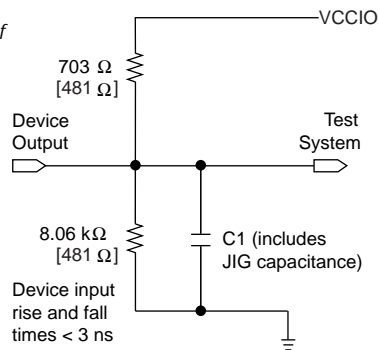
Table 10. FLEX 10KE Row-to-IOE Interconnect Resources		
Device	Channels per Row ( $n$ )	Row Channels per Pin ( $m$ )
EPF10K30E	216	27
EPF10K50E EPF10K50S	216	27
EPF10K100E	312	39
EPF10K130E	312	39
EPF10K200E EPF10K200S	312	39

## Generic Testing

Each FLEX 10KE device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for FLEX 10KE devices are made under conditions equivalent to those shown in [Figure 21](#). Multiple test patterns can be used to configure devices during all stages of the production flow.

**Figure 21. FLEX 10KE AC Test Conditions**

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V devices or outputs. Numbers without brackets are for 3.3-V devices or outputs.



## Operating Conditions

[Tables 19](#) through [23](#) provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V FLEX 10KE devices.

**Table 19. FLEX 10KE 2.5-V Device Absolute Maximum Ratings** *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage	With respect to ground (2)	–0.5	3.6	V
$V_{CCIO}$			–0.5	4.6	V
$V_I$	DC input voltage		–2.0	5.75	V
$I_{OUT}$	DC output current, per pin		–25	25	mA
$T_{STG}$	Storage temperature	No bias	–65	150	°C
$T_{AMB}$	Ambient temperature	Under bias	–65	135	°C
$T_J$	Junction temperature	PQFP, TQFP, BGA, and FineLine BGA packages, under bias		135	°C
		Ceramic PGA packages, under bias		150	°C

Figure 26. FLEX 10KE Device IOE Timing Model

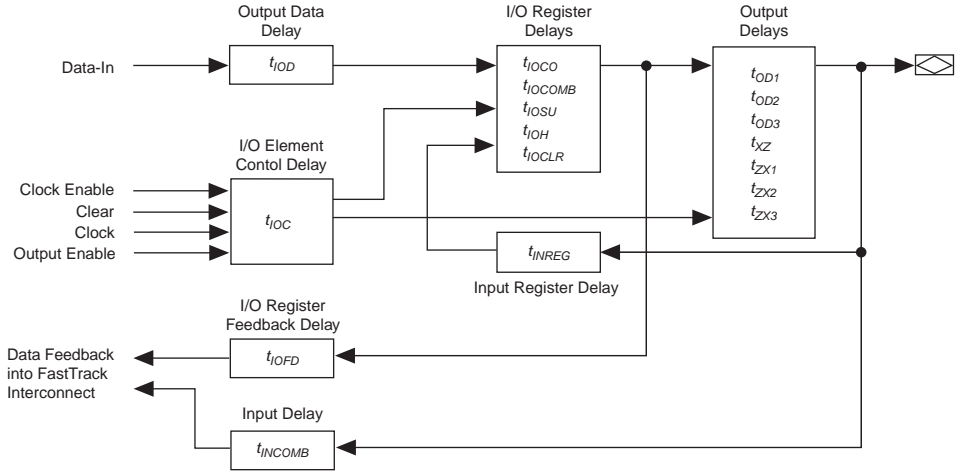
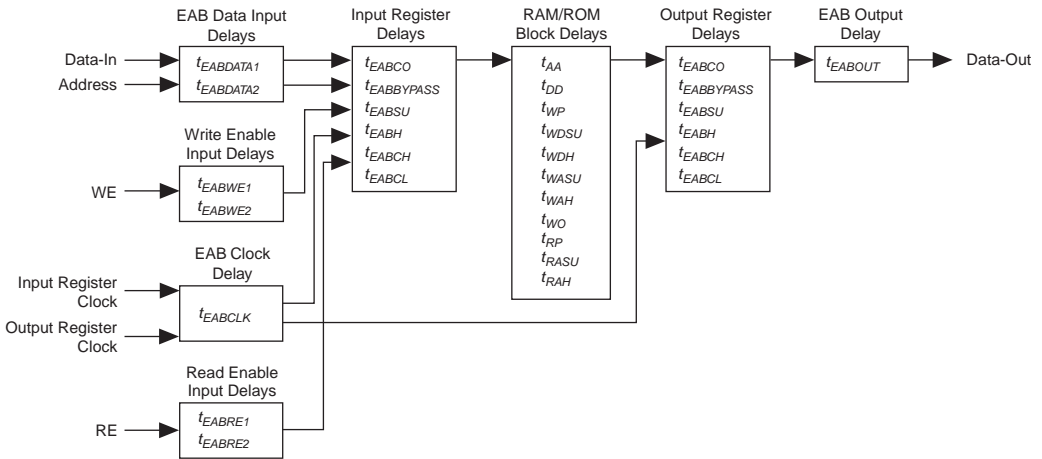


Figure 27. FLEX 10KE Device EAB Timing Model



**Table 30. External Bidirectional Timing Parameters** *Note (9)*

Symbol	Parameter	Conditions
$t_{\text{INSUBIDIR}}$	Setup time for bi-directional pins with global clock at same-row or same-column LE register	
$t_{\text{INHBIDIR}}$	Hold time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{\text{INH}}$	Hold time with global clock at IOE register	
$t_{\text{OUTCOBIDIR}}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	C1 = 35 pF
$t_{\text{XZBIDIR}}$	Synchronous IOE output buffer disable delay	C1 = 35 pF
$t_{\text{ZXBIDIR}}$	Synchronous IOE output buffer enable delay, slow slew rate= off	C1 = 35 pF

**Notes to tables:**

- (1) Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.
- (2) Operating conditions:  $V_{\text{CCIO}} = 3.3 \text{ V} \pm 10\%$  for commercial or industrial use.
- (3) Operating conditions:  $V_{\text{CCIO}} = 2.5 \text{ V} \pm 5\%$  for commercial or industrial use in EPF10K30E, EPF10K50S, EPF10K100E, EPF10K130E, and EPF10K200S devices.
- (4) Operating conditions:  $V_{\text{CCIO}} = 3.3 \text{ V}$ .
- (5) Because the RAM in the EAB is self-timed, this parameter can be ignored when the  $\text{WE}$  signal is registered.
- (6) EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.
- (7) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.
- (8) Contact Altera Applications for test circuit specifications and test conditions.
- (9) This timing parameter is sample-tested only.
- (10) This parameter is measured with the measurement and test conditions, including load, specified in the PCI Local Bus Specification, revision 2.2.

Table 38. EPF10K50E Device LE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_H$	0.9		1.0		1.4		ns
$t_{PRE}$		0.5		0.6		0.8	ns
$t_{CLR}$		0.5		0.6		0.8	ns
$t_{CH}$	2.0		2.5		3.0		ns
$t_{CL}$	2.0		2.5		3.0		ns

Table 39. EPF10K50E Device IOE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{IOD}$		2.2		2.4		3.3	ns
$t_{IOC}$		0.3		0.3		0.5	ns
$t_{IOCO}$		1.0		1.0		1.4	ns
$t_{IOCOMB}$		0.0		0.0		0.2	ns
$t_{IOSU}$	1.0		1.2		1.7		ns
$t_{IOH}$	0.3		0.3		0.5		ns
$t_{IOCLR}$		0.9		1.0		1.4	ns
$t_{OD1}$		0.8		0.9		1.2	ns
$t_{OD2}$		0.3		0.4		0.7	ns
$t_{OD3}$		3.0		3.5		3.5	ns
$t_{XZ}$		1.4		1.7		2.3	ns
$t_{ZX1}$		1.4		1.7		2.3	ns
$t_{ZX2}$		0.9		1.2		1.8	ns
$t_{ZX3}$		3.6		4.3		4.6	ns
$t_{INREG}$		4.9		5.8		7.8	ns
$t_{IOFD}$		2.8		3.3		4.5	ns
$t_{INCOMB}$		2.8		3.3		4.5	ns

Table 56. EPF10K130E Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		2.8		3.5		4.4	ns
$t_{DIN2LE}$		0.7		1.2		1.6	ns
$t_{DIN2DATA}$		1.6		1.9		2.2	ns
$t_{DCLK2IOE}$		1.6		2.1		2.7	ns
$t_{DCLK2LE}$		0.7		1.2		1.6	ns
$t_{SAMELAB}$		0.1		0.2		0.2	ns
$t_{SAMEROW}$		1.9		3.4		5.1	ns
$t_{SAMECOLUMN}$		0.9		2.6		4.4	ns
$t_{DIFFROW}$		2.8		6.0		9.5	ns
$t_{TWOROWS}$		4.7		9.4		14.6	ns
$t_{LEPERIPH}$		3.1		4.7		6.9	ns
$t_{LABCARRY}$		0.6		0.8		1.0	ns
$t_{LABCASC}$		0.9		1.2		1.6	ns

Table 57. EPF10K130E External Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DRR}$		9.0		12.0		16.0	ns
$t_{INSU}^{(3)}$	1.9		2.1		3.0		ns
$t_{INH}^{(3)}$	0.0		0.0		0.0		ns
$t_{OUTCO}^{(3)}$	2.0	5.0	2.0	7.0	2.0	9.2	ns
$t_{INSU}^{(4)}$	0.9		1.1		—		ns
$t_{INH}^{(4)}$	0.0		0.0		—		ns
$t_{OUTCO}^{(4)}$	0.5	4.0	0.5	6.0	—	—	ns
$t_{PCISU}$	3.0		6.2		—		ns
$t_{PCIH}$	0.0		0.0		—		ns
$t_{PCICO}$	2.0	6.0	2.0	6.9	—	—	ns

Table 61. EPF10K200E Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		2.0		2.4		3.2	ns
$t_{EABDATA1}$		0.4		0.5		0.6	ns
$t_{EABWE1}$		1.4		1.7		2.3	ns
$t_{EABWE2}$		0.0		0.0		0.0	ns
$t_{EABRE1}$		0		0		0	ns
$t_{EABRE2}$		0.4		0.5		0.6	ns
$t_{EABCLK}$		0.0		0.0		0.0	ns
$t_{EABCO}$		0.8		0.9		1.2	ns
$t_{EABYPASS}$		0.0		0.1		0.1	ns
$t_{EABSU}$	0.9		1.1		1.5		ns
$t_{EABH}$	0.4		0.5		0.6		ns
$t_{EABCLR}$	0.8		0.9		1.2		ns
$t_{AA}$		3.1		3.7		4.9	ns
$t_{WP}$	3.3		4.0		5.3		ns
$t_{RP}$	0.9		1.1		1.5		ns
$t_{WDSU}$	0.9		1.1		1.5		ns
$t_{WDH}$	0.1		0.1		0.1		ns
$t_{WASU}$	1.3		1.6		2.1		ns
$t_{WAH}$	2.1		2.5		3.3		ns
$t_{RASU}$	2.2		2.6		3.5		ns
$t_{RAH}$	0.1		0.1		0.2		ns
$t_{WO}$		2.0		2.4		3.2	ns
$t_{DD}$		2.0		2.4		3.2	ns
$t_{EABOUT}$		0.0		0.1		0.1	ns
$t_{EABCH}$	1.5		2.0		2.5		ns
$t_{EABCL}$	3.3		4.0		5.3		ns

Table 62. EPF10K200E Device EAB Internal Timing Macroparameters (Part 1 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABAA}$		5.1		6.4		8.4	ns
$t_{EABRCOMB}$	5.1		6.4		8.4		ns
$t_{EABRCREG}$	4.8		5.7		7.6		ns
$t_{EABWP}$	3.3		4.0		5.3		ns

Table 68. EPF10K50S Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.7		2.4		3.2	ns
$t_{EABDATA2}$		0.4		0.6		0.8	ns
$t_{EABWE1}$		1.0		1.4		1.9	ns
$t_{EABWE2}$		0.0		0.0		0.0	ns
$t_{EABRE1}$		0.0		0.0		0.0	
$t_{EABRE2}$		0.4		0.6		0.8	
$t_{EABCLK}$		0.0		0.0		0.0	ns
$t_{EABCO}$		0.8		1.1		1.5	ns
$t_{EABYPASS}$		0.0		0.0		0.0	ns
$t_{EABSU}$	0.7		1.0		1.3		ns
$t_{EABH}$	0.4		0.6		0.8		ns
$t_{EABCLR}$	0.8		1.1		1.5		
$t_{AA}$		2.0		2.8		3.8	ns
$t_{WP}$	2.0		2.8		3.8		ns
$t_{RP}$	1.0		1.4		1.9		
$t_{WDSU}$	0.5		0.7		0.9		ns
$t_{WDH}$	0.1		0.1		0.2		ns
$t_{WASU}$	1.0		1.4		1.9		ns
$t_{WAH}$	1.5		2.1		2.9		ns
$t_{RASU}$	1.5		2.1		2.8		
$t_{RAH}$	0.1		0.1		0.2		
$t_{WO}$		2.1		2.9		4.0	ns
$t_{DD}$		2.1		2.9		4.0	ns
$t_{EABOUT}$		0.0		0.0		0.0	ns
$t_{EABCH}$	1.5		2.0		2.5		ns
$t_{EABCL}$	1.5		2.0		2.5		ns

Table 71. EPF10K50S External Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{DRR}}$		8.0		9.5		12.5	ns
$t_{\text{INSU}}^{(2)}$	2.4		2.9		3.9		ns
$t_{\text{INH}}^{(2)}$	0.0		0.0		0.0		ns
$t_{\text{OUTCO}}^{(2)}$	2.0	4.3	2.0	5.2	2.0	7.3	ns
$t_{\text{INSU}}^{(3)}$	2.4		2.9				ns
$t_{\text{INH}}^{(3)}$	0.0		0.0				ns
$t_{\text{OUTCO}}^{(3)}$	0.5	3.3	0.5	4.1			ns
$t_{\text{PCISU}}$	2.4		2.9		—		ns
$t_{\text{PCIH}}$	0.0		0.0		—		ns
$t_{\text{PCICO}}$	2.0	6.0	2.0	7.7	—	—	ns

Table 72. EPF10K50S External Bidirectional Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}^{(2)}$	2.7		3.2		4.3		ns
$t_{\text{INHBIDIR}}^{(2)}$	0.0		0.0		0.0		ns
$t_{\text{INHBIDIR}}^{(3)}$	0.0		0.0		—		ns
$t_{\text{INSUBIDIR}}^{(3)}$	3.7		4.2		—		ns
$t_{\text{OUTCOBIDIR}}^{(2)}$	2.0	4.5	2.0	5.2	2.0	7.3	ns
$t_{\text{XZBIDIR}}^{(2)}$		6.8		7.8		10.1	ns
$t_{\text{ZXBIDIR}}^{(2)}$		6.8		7.8		10.1	ns
$t_{\text{OUTCOBIDIR}}^{(3)}$	0.5	3.5	0.5	4.2	—	—	
$t_{\text{XZBIDIR}}^{(3)}$		6.8		8.4		—	ns
$t_{\text{ZXBIDIR}}^{(3)}$		6.8		8.4		—	ns

**Notes to tables:**

- (1) All timing parameters are described in [Tables 24](#) through [30](#).
- (2) This parameter is measured without use of the ClockLock or ClockBoost circuits.
- (3) This parameter is measured with use of the ClockLock or ClockBoost circuits

Table 73. EPF10K200S Device Internal & External Timing Parameters

Note (1)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{LUT}$		0.7		0.8		1.2	ns
$t_{CLUT}$		0.4		0.5		0.6	ns
$t_{RLUT}$		0.5		0.7		0.9	ns
$t_{PACKED}$		0.4		0.5		0.7	ns
$t_{EN}$		0.6		0.5		0.6	ns
$t_{CICO}$		0.1		0.2		0.3	ns
$t_{CGEN}$		0.3		0.4		0.6	ns
$t_{CGENR}$		0.1		0.2		0.3	ns
$t_{CASC}$		0.7		0.8		1.2	ns
$t_C$		0.5		0.6		0.8	ns
$t_{CO}$		0.5		0.6		0.8	ns
$t_{COMB}$		0.3		0.6		0.8	ns
$t_{SU}$	0.4		0.6		0.7		ns
$t_H$	1.0		1.1		1.5		ns
$t_{PRE}$		0.4		0.6		0.8	ns
$t_{CLR}$		0.5		0.6		0.8	ns
$t_{CH}$	2.0		2.5		3.0		ns
$t_{CL}$	2.0		2.5		3.0		ns

Table 74. EPF10K200S Device IOE Timing Microparameters (Part 1 of 2)

Note (1)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{IOD}$		1.8		1.9		2.6	ns
$t_{IOC}$		0.3		0.3		0.5	ns
$t_{IOCO}$		1.7		1.9		2.6	ns
$t_{IOCOMB}$		0.5		0.6		0.8	ns
$t_{IOSU}$	0.8		0.9		1.2		ns
$t_{IOH}$	0.4		0.8		1.1		ns
$t_{IOCLR}$		0.2		0.2		0.3	ns
$t_{OD1}$		1.3		0.7		0.9	ns
$t_{OD2}$		0.8		0.2		0.4	ns
$t_{OD3}$		2.9		3.0		3.9	ns
$t_{XZ}$		5.0		5.3		7.1	ns
$t_{ZX1}$		5.0		5.3		7.1	ns

# Power Consumption

The supply power (P) for FLEX 10KE devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = (I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC} + P_{IO}$$

The  $I_{CCACTIVE}$  value depends on the switching frequency and the application logic. This value is calculated based on the amount of current that each LE typically consumes. The  $P_{IO}$  value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in [Application Note 74 \(Evaluating Power for Altera Devices\)](#).

Compared to the rest of the device, the embedded array consumes a negligible amount of power. Therefore, the embedded array can be ignored when calculating supply current.

The  $I_{CCACTIVE}$  value can be calculated with the following equation:

$$I_{CCACTIVE} = K \times f_{MAX} \times N \times \text{tog}_{LC} \times \frac{\mu A}{MHz \times LE}$$

Where:

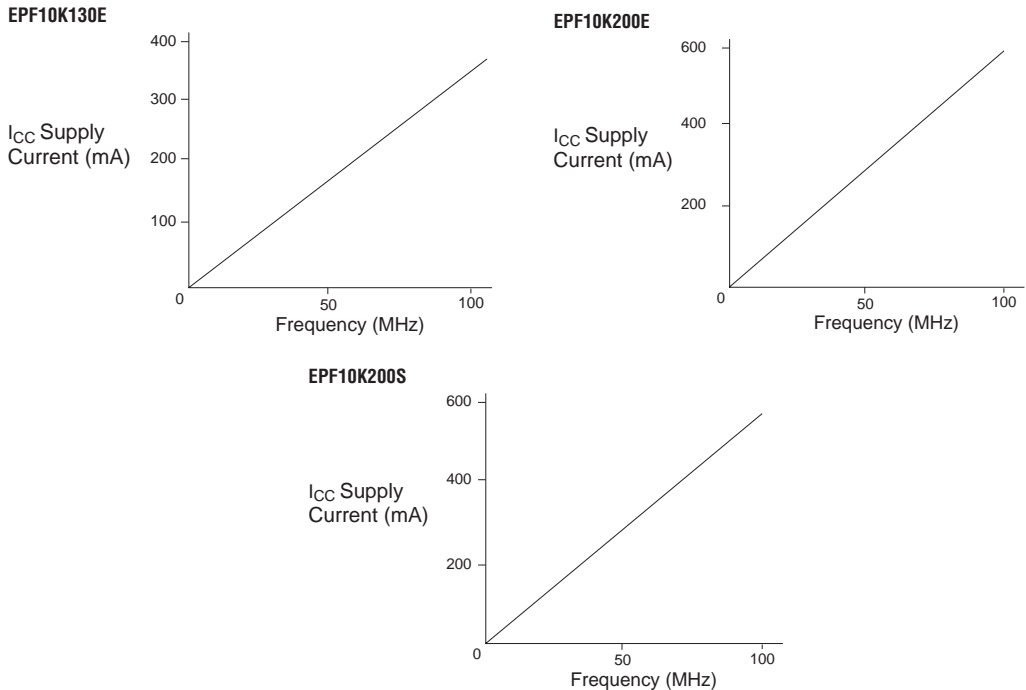
- $f_{MAX}$  = Maximum operating frequency in MHz
- $N$  = Total number of LEs used in the device
- $\text{tog}_{LC}$  = Average percent of LEs toggling at each clock (typically 12.5%)
- $K$  = Constant

**Table 80** provides the constant (K) values for FLEX 10KE devices.

Table 80. FLEX 10KE K Constant Values	
Device	K Value
EPF10K30E	4.5
EPF10K50E	4.8
EPF10K50S	4.5
EPF10K100E	4.5
EPF10K130E	4.6
EPF10K200E	4.8
EPF10K200S	4.6

This calculation provides an  $I_{CC}$  estimate based on typical conditions with no output load. The actual  $I_{CC}$  should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 31. FLEX 10KE  $I_{CCACTIVE}$  vs. Operating Frequency (Part 2 of 2)



## Configuration & Operation

The FLEX 10KE architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

### Operating Modes

The FLEX 10KE architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. The process of physically loading the SRAM data into the device is called *configuration*. Before configuration, as  $V_{CC}$  rises, the device initiates a Power-On Reset (POR). This POR event clears the device and prepares it for configuration. The FLEX 10KE POR time does not exceed 50  $\mu$ s.

When configuring with a configuration device, refer to the respective configuration device data sheet for POR timing information.

## Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the Altera Digital Library for pin-out information.

## Revision History

The information contained in the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.5 supersedes information published in previous versions.

### Version 2.5

The following changes were made to the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.5:

- *Note (1)* added to **Figure 23**.
- Text added to “I/O Element” section on **page 34**.
- Updated **Table 22**.

### Version 2.4

The following changes were made to the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.4: updated text on **page 34** and **page 63**.