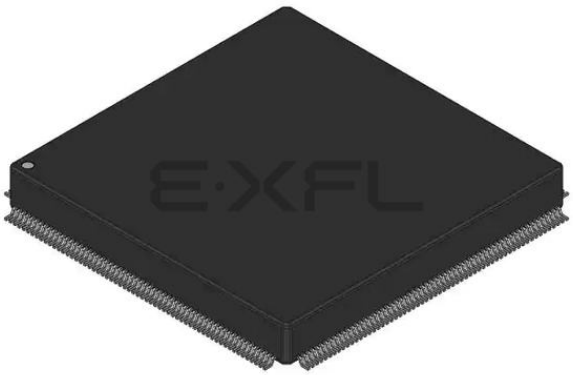

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 832 |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 186 |
| Number of Gates | - |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 240-BQFP |
| Supplier Device Package | 240-PQFP (32x32) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=epf10k130eqc240-1 |

For more information on FLEX device configuration, see the following documents:

- *Configuration Devices for APEX & FLEX Devices Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *MasterBlaster Download Cable Data Sheet*
- *Application Note 116 (Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices)*

FLEX 10KE devices are supported by the Altera development systems, which are integrated packages that offer schematic, text (including AHDL), and waveform design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, and device configuration. The Altera software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The Altera software works easily with common gate array EDA tools for synthesis and simulation. For example, the Altera software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the Altera software contains EDA libraries that use device-specific features such as carry chains, which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the Altera development system includes DesignWare functions that are optimized for the FLEX 10KE architecture.

The Altera development system runs on Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800.

See the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet* for more information.

## Functional Description

Each FLEX 10KE device contains an enhanced embedded array to implement memory and specialized logic functions, and a logic array to implement general logic.

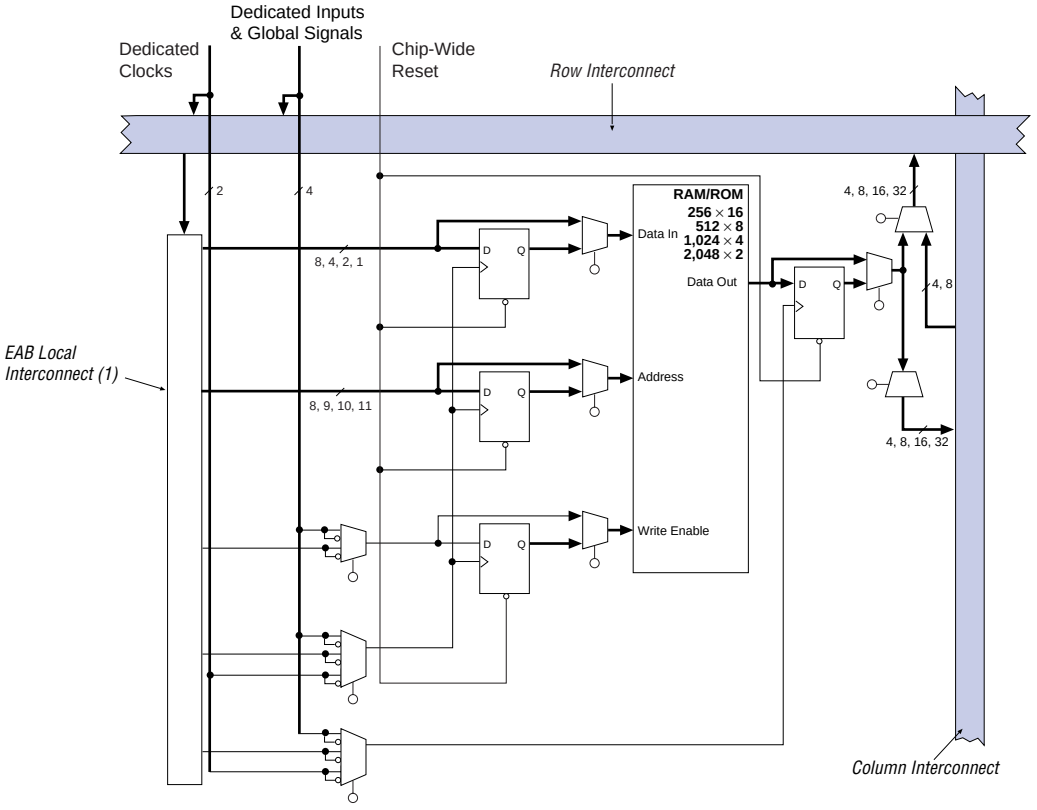
The embedded array consists of a series of EABs. When implementing memory functions, each EAB provides 4,096 bits, which can be used to create RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. When implementing logic, each EAB can contribute 100 to 600 gates towards complex logic functions, such as multipliers, microcontrollers, state machines, and DSP functions. EABs can be used independently, or multiple EABs can be combined to implement larger functions.

The logic array consists of logic array blocks (LABs). Each LAB contains eight LEs and a local interconnect. An LE consists of a four-input look-up table (LUT), a programmable flipflop, and dedicated signal paths for carry and cascade functions. The eight LEs can be used to create medium-sized blocks of logic—such as 8-bit counters, address decoders, or state machines—or combined across LABs to create larger logic blocks. Each LAB represents about 96 usable gates of logic.

Signal interconnections within FLEX 10KE devices (as well as to and from device pins) are provided by the FastTrack Interconnect routing structure, which is a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect routing structure. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an output or input register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. As inputs, they provide setup times as low as 0.9 ns and hold times of 0 ns. As outputs, these registers provide clock-to-output times as low as 3.0 ns. IOEs provide a variety of features, such as JTAG BST support, slew-rate control, tri-state buffers, and open-drain outputs.

*Figure 4. FLEX 10KE Device in Single-Port RAM Mode*




***Note:***

(1) EPF10K30E, EPF10K50E, and EPF10K50S devices have 88 EAB local interconnect channels; EPF10K100E, EPF10K130E, EPF10K200E, and EPF10K200S devices have 104 EAB local interconnect channels.

EABs can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the write enable signal. In contrast, the EAB's synchronous RAM generates its own write enable signal and is self-timed with respect to the input or write clock. A circuit using the EAB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

### *LE Operating Modes*

The FLEX 10KE LE can operate in the following four modes:

- Normal mode
- Arithmetic mode
- Up / down counter mode
- Clearable counter mode

Each of these modes uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. Three inputs to the LE provide clock, clear, and preset control for the register. The Altera software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that use a specific LE operating mode for optimal performance.

The architecture provides a synchronous clock enable to the register in all four modes. The Altera software can set DATA1 to enable the register synchronously, providing easy implementation of fully synchronous designs.

### Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Altera Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. Either the register or the LUT can be used to drive both the local interconnect and the FastTrack Interconnect routing structure at the same time.

The LUT and the register in the LE can be used independently (register packing). To support register packing, the LE has two outputs; one drives the local interconnect, and the other drives the FastTrack Interconnect routing structure. The DATA4 signal can drive the register directly, allowing the LUT to compute a function that is independent of the registered signal; a three-input function can be computed in the LUT, and a fourth independent signal can be registered. Alternatively, a four-input function can be generated, and one of the inputs to this function can be used to drive the register. The register in a packed LE can still use the clock enable, clear, and preset signals in the LE. In a packed LE, the register can drive the FastTrack Interconnect routing structure while the LUT drives the local interconnect, or vice versa.

### Arithmetic Mode

The arithmetic mode offers 2 three-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 11 on page 22, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three signals: a, b, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

### Up/Down Counter Mode

The up / down counter mode offers counter enable, clock enable, synchronous up / down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Use 2 three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the clear and preset register control signals without using the LUT resources.

*Table 9. Peripheral Bus Sources for EPF10K100E, EPF10K130E, EPF10K200E & EPF10K200S Devices*

| Peripheral Control Signal | EPF10K100E | EPF10K130E | EPF10K200E EPF10K200S |
|---|---|---|---|
| OE0 | Row A | Row C | Row G |
| OE1 | Row C | Row E | Row I |
| OE2 | Row E | Row G | Row K |
| OE3 | Row L | Row N | Row R |
| OE4 | Row I | Row K | Row O |
| OE5 | Row K | Row M | Row Q |
| CLKENA0/CLK0/GLOBAL0 | Row F | Row H | Row L |
| CLKENA1/OE6/GLOBAL1 | Row D | Row F | Row J |
| CLKENA2/CLR0 | Row B | Row D | Row H |
| CLKENA3/OE7/GLOBAL2 | Row H | Row J | Row N |
| CLKENA4/CLR1 | Row J | Row L | Row P |
| CLKENA5/CLK1/GLOBAL3 | Row G | Row I | Row M |

Signals on the peripheral control bus can also drive the four global signals, referred to as GLOBAL0 through GLOBAL3 in Tables 8 and 9. An internally generated signal can drive a global signal, providing the same low-skew, low-delay characteristics as a signal driven by an input pin. An LE drives the global signal by driving a row line that drives the peripheral bus, which then drives the global signal. This feature is ideal for internally generated clear or clock signals with high fan-out. However, internally driven global signals offer no advantage over the general-purpose interconnect for routing data signals. The dedicated input pin should be driven to a known logic state (such as ground) and not be allowed to float.

The chip-wide output enable pin is an active-high pin (DEV_OE) that can be used to tri-state all pins on the device. This option can be set in the Altera software. On EPF10K50E and EPF10K200E devices, the built-in I/O pin pull-up resistors (which are active during configuration) are active when the chip-wide output enable pin is asserted. The registers in the IOE can also be reset by the chip-wide reset pin.

*Table 13. ClockLock & ClockBoost Parameters for -2 Speed-Grade Devices*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_R$ | Input rise time | | | | 5 | ns |
| $t_F$ | Input fall time | | | | 5 | ns |
| $t_{INDUTY}$ | Input duty cycle | | 40 | | 60 | % |
| $f_{CLK1}$ | Input clock frequency (ClockBoost clock multiplication factor equals 1) | | 25 | | 75 | MHz |
| $f_{CLK2}$ | Input clock frequency (ClockBoost clock multiplication factor equals 2) | | 16 | | 37.5 | MHz |
| $f_{CLKDEV}$ | Input deviation from user specification in the MAX+PLUS II software *(1)* | | | | 25,000 *(2)* | PPM |
| $t_{INCLKSTB}$ | Input clock stability (measured between adjacent clocks) | | | | 100 | ps |
| $t_{LOCK}$ | Time required for ClockLock or ClockBoost to acquire lock *(3)* | | | | 10 | µs |
| $t_{JITTER}$ | Jitter on ClockLock or ClockBoost-generated clock *(4)* | $t_{INCLKSTB}$ < 100 | | | 250 | ps |
| | | $t_{INCLKSTB}$ < 50 | | | 200 *(4)* | ps |
| $t_{OUTDUTY}$ | Duty cycle for ClockLock or ClockBoost-generated clock | | 40 | 50 | 60 | % |

***Notes to tables:***

(1) To implement the ClockLock and ClockBoost circuitry with the MAX+PLUS II software, designers must specify the input frequency. The Altera software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The $f_{CLKDEV}$ parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.

(2) Twenty-five thousand parts per million (PPM) equates to 2.5% of input clock period.

(3) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration because the $t_{LOCK}$ value is less than the time required for configuration.

(4) The $t_{JITTER}$ specification is measured under long-term observation. The maximum value for $t_{JITTER}$ is 200 ps if $t_{INCLKSTB}$ is lower than 50 ps.

# I/O Configuration

This section discusses the peripheral component interconnect (PCI) pull-up clamping diode option, slew-rate control, open-drain output option, and MultiVolt I/O interface for FLEX 10KE devices. The PCI pull-up clamping diode, slew-rate control, and open-drain output options are controlled pin-by-pin via Altera software logic options. The MultiVolt I/O interface is controlled by connecting $V_{CCIO}$ to a different voltage than $V_{CCINT}$. Its effect can be simulated in the Altera software via the **Global Project Device Options** dialog box (Assign menu).

Figure 20 shows the timing requirements for the JTAG signals.

*Figure 20. FLEX 10KE JTAG Waveforms*

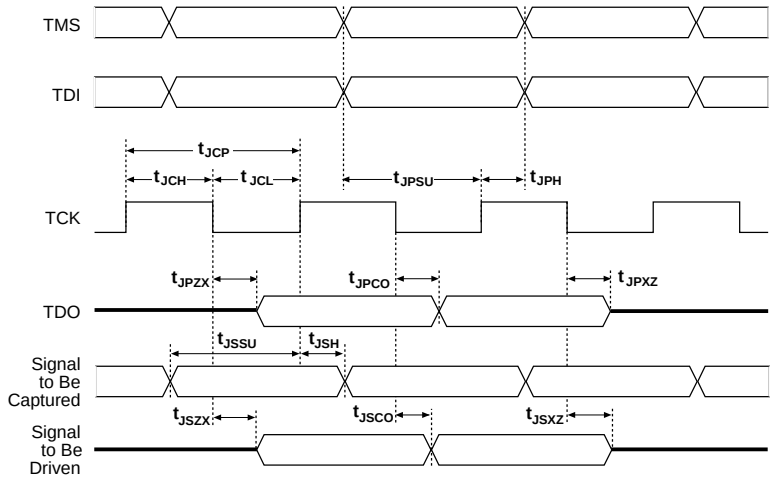



Table 18 shows the timing parameters and values for FLEX 10KE devices.

*Table 18. FLEX 10KE JTAG Timing Parameters & Values*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 100 | | ns |
| $t_{JCH}$ | TCK clock high time | 50 | | ns |
| $t_{JCL}$ | TCK clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock to output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock to output | | 35 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | | 35 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | | 35 | ns |

**Table 22. FLEX 10KE 2.5-V Device DC Operating Conditions** *Notes (6), (7)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 1.7, 0.5 × $V_{CCIO}$ *(8)* | | 5.75 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | 0.8, 0.3 × $V_{CCIO}$ *(8)* | V |
| $V_{OH}$ | 3.3-V high-level TTL output voltage | $I_{OH}$ = –8 mA DC, $V_{CCIO}$ = 3.00 V *(9)* | 2.4 | | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(9)* | $V_{CCIO}$ – 0.2 | | | V |
| | 3.3-V high-level PCI output voltage | $I_{OH}$ = –0.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(9)* | 0.9 × $V_{CCIO}$ | | | V |
| | 2.5-V high-level output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 2.30 V *(9)* | 2.1 | | | V |
| | | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.30 V *(9)* | 2.0 | | | V |
| | | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.30 V *(9)* | 1.7 | | | V |
| $V_{OL}$ | 3.3-V low-level TTL output voltage | $I_{OL}$ = 12 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | | | 0.2 | V |
| | 3.3-V low-level PCI output voltage | $I_{OL}$ = 1.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(10)* | | | 0.1 × $V_{CCIO}$ | V |
| | 2.5-V low-level output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | | | 0.2 | V |
| | | $I_{OL}$ = 1 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | | | 0.4 | V |
| | | $I_{OL}$ = 2 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | | | 0.7 | V |
| $I_I$ | Input pin leakage current | $V_I$ = $V_{CCIOmax}$ to 0 V *(11)* | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current | $V_O$ = $V_{CCIOmax}$ to 0 V *(11)* | –10 | | 10 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) | $V_I$ = ground, no load, no toggling inputs | | 5 | | mA |
| | | $V_I$ = ground, no load, no toggling inputs *(12)* | | 10 | | mA |
| $R_{CONF}$ | Value of I/O pin pull-up resistor before and during configuration | $V_{CCIO}$ = 3.0 V *(13)* | 20 | | 50 | k¾ |
| | | $V_{CCIO}$ = 2.3 V *(13)* | 30 | | 80 | k¾ |

**Table 23. FLEX 10KE Device Capacitance** *Note (14)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 10 | pF |
| $C_{INCLK}$ | Input capacitance on dedicated clock pin | $V_{IN}$ = 0 V, f = 1.0 MHz | | 12 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 10 | pF |

***Notes to tables:***

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum $V_{CC}$ rise time is 100 ms, and $V_{CC}$ must rise monotonically.
(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.
(6) Typical values are for $T_A$ = 25° C, $V_{CCINT}$ = 2.5 V, and $V_{CCIO}$ = 2.5 V or 3.3 V.
(7) These values are specified under the FLEX 10KE Recommended Operating Conditions shown in Tables 20 and 21.
(8) The FLEX 10KE input buffers are compatible with 2.5-V, 3.3-V (LVTTL and LVCMOS), and 5.0-V TTL and CMOS signals. Additionally, the input buffers are 3.3-V PCI compliant when $V_{CCIO}$ and $V_{CCINT}$ meet the relationship shown in Figure 22.
(9) The $I_{OH}$ parameter refers to high-level TTL, PCI, or CMOS output current.
(10) The $I_{OL}$ parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(11) This value is specified for normal device operation. The value may vary during power-up.
(12) This parameter applies to -1 speed-grade commercial-temperature devices and -2 speed-grade-industrial temperature devices.
(13) Pin pull-up resistance values will be lower if the pin is driven higher than $V_{CCIO}$ by an external source.
(14) Capacitance is sample-tested only.

*Figure 25. FLEX 10KE Device LE Timing Model*

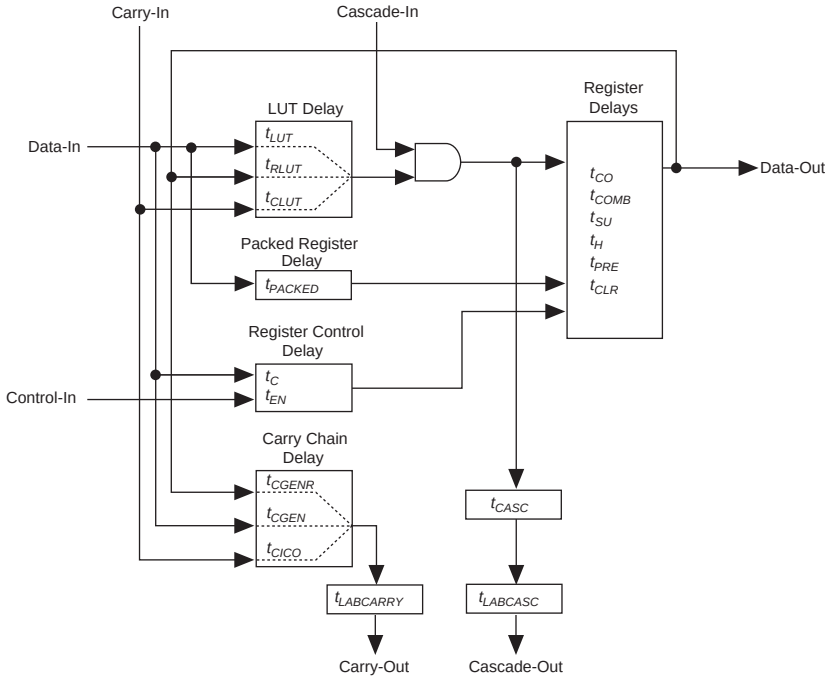
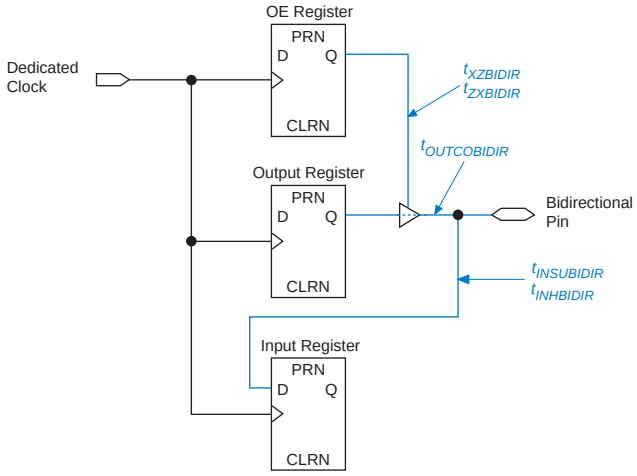


*Figure 28. Synchronous Bidirectional Pin External Timing Model*




Tables 24 through 28 describe the FLEX 10KE device internal timing parameters. Tables 29 through 30 describe the FLEX 10KE external timing parameters and their symbols.

*Table 24. LE Timing Microparameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | Condition |
|---|---|---|
| $t_{LUT}$ | LUT delay for data-in | |
| $t_{CLUT}$ | LUT delay for carry-in | |
| $t_{RLUT}$ | LUT delay for LE register feedback | |
| $t_{PACKED}$ | Data-in to packed register delay | |
| $t_{EN}$ | LE register enable delay | |
| $t_{CICO}$ | Carry-in to carry-out delay | |
| $t_{CGEN}$ | Data-in to carry-out delay | |
| $t_{CGENR}$ | LE register feedback to carry-out delay | |
| $t_{CASC}$ | Cascade-in to cascade-out delay | |
| $t_{C}$ | LE register control signal delay | |
| $t_{CO}$ | LE register clock-to-output delay | |
| $t_{COMB}$ | Combinatorial delay | |
| $t_{SU}$ | LE register setup time for data and enable signals before clock; LE register recovery time after asynchronous clear, preset, or load | |
| $t_{H}$ | LE register hold time for data and enable signals after clock | |
| $t_{PRE}$ | LE register preset delay | |

| *Table 24. LE Timing Microparameters (Part 2 of 2)* *Note (1)* | | |
|---|---|---|
| **Symbol** | **Parameter** | **Condition** |
| $t_{CLR}$ | LE register clear delay | |
| $t_{CH}$ | Minimum clock high time from clock pin | |
| $t_{CL}$ | Minimum clock low time from clock pin | |

| *Table 25. IOE Timing Microparameters* *Note (1)* | | |
|---|---|---|
| **Symbol** | **Parameter** | **Conditions** |
| $t_{IOD}$ | IOE data delay | |
| $t_{IOC}$ | IOE register control signal delay | |
| $t_{IOCO}$ | IOE register clock-to-output delay | |
| $t_{IOCOMB}$ | IOE combinatorial delay | |
| $t_{IOSU}$ | IOE register setup time for data and enable signals before clock; IOE register recovery time after asynchronous clear | |
| $t_{IOH}$ | IOE register hold time for data and enable signals after clock | |
| $t_{IOCLR}$ | IOE register clear time | |
| $t_{OD1}$ | Output buffer and pad delay, slow slew rate = off, $V_{CCIO}$ = 3.3 V | C1 = 35 pF *(2)* |
| $t_{OD2}$ | Output buffer and pad delay, slow slew rate = off, $V_{CCIO}$ = 2.5 V | C1 = 35 pF *(3)* |
| $t_{OD3}$ | Output buffer and pad delay, slow slew rate = on | C1 = 35 pF *(4)* |
| $t_{XZ}$ | IOE output buffer disable delay | |
| $t_{ZX1}$ | IOE output buffer enable delay, slow slew rate = off, $V_{CCIO}$ = 3.3 V | C1 = 35 pF *(2)* |
| $t_{ZX2}$ | IOE output buffer enable delay, slow slew rate = off, $V_{CCIO}$ = 2.5 V | C1 = 35 pF *(3)* |
| $t_{ZX3}$ | IOE output buffer enable delay, slow slew rate = on | C1 = 35 pF *(4)* |
| $t_{INREG}$ | IOE input pad and buffer to IOE register delay | |
| $t_{IOFD}$ | IOE register feedback delay | |
| $t_{INCOMB}$ | IOE input pad and buffer to FastTrack Interconnect delay | |

*Table 43. EPF10K50E External Timing Parameters* *Notes (1), (2)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 8.5 | | 10.0 | | 13.5 | ns |
| $t_{INSU}$ | 2.7 | | 3.2 | | 4.3 | | ns |
| $t_{INH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ | 2.0 | 4.5 | 2.0 | 5.2 | 2.0 | 7.3 | ns |
| $t_{PCISU}$ | 3.0 | | 4.2 | | - | | ns |
| $t_{PCIH}$ | 0.0 | | 0.0 | | - | | ns |
| $t_{PCICO}$ | 2.0 | 6.0 | 2.0 | 7.7 | - | - | ns |

*Table 44. EPF10K50E External Bidirectional Timing Parameters* *Notes (1), (2)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.7 | | 3.2 | | 4.3 | | ns |
| $t_{INHBIDIR}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCOBIDIR}$ | 2.0 | 4.5 | 2.0 | 5.2 | 2.0 | 7.3 | ns |
| $t_{XZBIDIR}$ | | 6.8 | | 7.8 | | 10.1 | ns |
| $t_{ZXBIDIR}$ | | 6.8 | | 7.8 | | 10.1 | ns |

***Notes to tables:***
(1) All timing parameters are described in Tables 24 through 30 in this data sheet.
(2) These parameters are specified by characterization.

Tables 45 through 51 show EPF10K100E device internal and external timing parameters.

*Table 45. EPF10K100E Device LE Timing Microparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 0.7 | | 1.0 | | 1.5 | ns |
| $t_{CLUT}$ | | 0.5 | | 0.7 | | 0.9 | ns |
| $t_{RLUT}$ | | 0.6 | | 0.8 | | 1.1 | ns |
| $t_{PACKED}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{EN}$ | | 0.2 | | 0.3 | | 0.3 | ns |
| $t_{CICO}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.5 | | 0.7 | ns |

Tables 52 through 58 show EPF10K130E device internal and external timing parameters.

**Table 52. EPF10K130E Device LE Timing Microparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 0.6 | | 0.9 | | 1.3 | ns |
| $t_{CLUT}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{RLUT}$ | | 0.7 | | 0.9 | | 0.2 | ns |
| $t_{PACKED}$ | | 0.3 | | 0.5 | | 0.6 | ns |
| $t_{EN}$ | | 0.2 | | 0.3 | | 0.4 | ns |
| $t_{CICO}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.6 | | 0.8 | ns |
| $t_{CGENR}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CASC}$ | | 0.6 | | 0.9 | | 1.2 | ns |
| $t_{C}$ | | 0.3 | | 0.5 | | 0.6 | ns |
| $t_{CO}$ | | 0.5 | | 0.7 | | 0.8 | ns |
| $t_{COMB}$ | | 0.3 | | 0.5 | | 0.6 | ns |
| $t_{SU}$ | 0.5 | | 0.7 | | 0.8 | | ns |
| $t_{H}$ | 0.6 | | 0.7 | | 1.0 | | ns |
| $t_{PRE}$ | | 0.9 | | 1.2 | | 1.6 | ns |
| $t_{CLR}$ | | 0.9 | | 1.2 | | 1.6 | ns |
| $t_{CH}$ | 1.5 | | 1.5 | | 2.5 | | ns |
| $t_{CL}$ | 1.5 | | 1.5 | | 2.5 | | ns |

**Table 53. EPF10K130E Device IOE Timing Microparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 1.3 | | 1.5 | | 2.0 | ns |
| $t_{IOC}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{IOCO}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{IOCOMB}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{IOSU}$ | 1.0 | | 1.2 | | 1.6 | | ns |
| $t_{IOH}$ | 0.9 | | 0.9 | | 1.4 | | ns |
| $t_{IOCLR}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{OD1}$ | | 2.8 | | 4.1 | | 5.5 | ns |
| $t_{OD2}$ | | 2.8 | | 4.1 | | 5.5 | ns |

**Table 53. EPF10K130E Device IOE Timing Microparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{OD3}$ | | 4.0 | | 5.6 | | 7.5 | ns |
| $t_{XZ}$ | | 2.8 | | 4.1 | | 5.5 | ns |
| $t_{ZX1}$ | | 2.8 | | 4.1 | | 5.5 | ns |
| $t_{ZX2}$ | | 2.8 | | 4.1 | | 5.5 | ns |
| $t_{ZX3}$ | | 4.0 | | 5.6 | | 7.5 | ns |
| $t_{INREG}$ | | 2.5 | | 3.0 | | 4.1 | ns |
| $t_{IOFD}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{INCOMB}$ | | 0.4 | | 0.5 | | 0.6 | ns |

**Table 54. EPF10K130E Device EAB Internal Microparameters** *(Part 1 of 2)* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 1.5 | | 2.0 | | 2.6 | ns |
| $t_{EABDATA2}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABWE1}$ | | 1.5 | | 2.0 | | 2.6 | ns |
| $t_{EABWE2}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{EABRE1}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{EABRE2}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCLK}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCO}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{EABBYPASS}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{EABSU}$ | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{EABH}$ | 0.1 | | 0.2 | | 0.2 | | ns |
| $t_{EABCLR}$ | 0.3 | | 0.4 | | 0.5 | | ns |
| $t_{AA}$ | | 4.0 | | 5.0 | | 6.6 | ns |
| $t_{WP}$ | 2.7 | | 3.5 | | 4.7 | | ns |
| $t_{RP}$ | 1.0 | | 1.3 | | 1.7 | | ns |
| $t_{WDSU}$ | 1.0 | | 1.3 | | 1.7 | | ns |
| $t_{WDH}$ | 0.2 | | 0.2 | | 0.3 | | ns |
| $t_{WASU}$ | 1.6 | | 2.1 | | 2.8 | | ns |
| $t_{WAH}$ | 1.6 | | 2.1 | | 2.8 | | ns |
| $t_{RASU}$ | 3.0 | | 3.9 | | 5.2 | | ns |
| $t_{RAH}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{WO}$ | | 1.5 | | 2.0 | | 2.6 | ns |

**Table 54. EPF10K130E Device EAB Internal Microparameters** *(Part 2 of 2)* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DD}$ | | 1.5 | | 2.0 | | 2.6 | ns |
| $t_{EABOUT}$ | | 0.2 | | 0.3 | | 0.3 | ns |
| $t_{EABCH}$ | 1.5 | | 2.0 | | 2.5 | | ns |
| $t_{EABCL}$ | 2.7 | | 3.5 | | 4.7 | | ns |

**Table 55. EPF10K130E Device EAB Internal Timing Macroparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABAA}$ | | 5.9 | | 7.5 | | 9.9 | ns |
| $t_{EABRCOMB}$ | 5.9 | | 7.5 | | 9.9 | | ns |
| $t_{EABRCREG}$ | 5.1 | | 6.4 | | 8.5 | | ns |
| $t_{EABWP}$ | 2.7 | | 3.5 | | 4.7 | | ns |
| $t_{EABWCOMB}$ | 5.9 | | 7.7 | | 10.3 | | ns |
| $t_{EABWCREG}$ | 5.4 | | 7.0 | | 9.4 | | ns |
| $t_{EABDD}$ | | 3.4 | | 4.5 | | 5.9 | ns |
| $t_{EABDATACO}$ | | 0.5 | | 0.7 | | 0.8 | ns |
| $t_{EABDATASU}$ | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{EABDATAH}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{EABWESU}$ | 1.1 | | 1.4 | | 1.9 | | ns |
| $t_{EABWEH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWDSU}$ | 1.0 | | 1.3 | | 1.7 | | ns |
| $t_{EABWDH}$ | 0.2 | | 0.2 | | 0.3 | | ns |
| $t_{EABWASU}$ | 4.1 | | 5.1 | | 6.8 | | ns |
| $t_{EABWAH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWO}$ | | 3.4 | | 4.5 | | 5.9 | ns |

*Table 71. EPF10K50S External Timing Parameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 8.0 | | 9.5 | | 12.5 | ns |
| $t_{INSU}$ *(2)* | 2.4 | | 2.9 | | 3.9 | | ns |
| $t_{INH}$ *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(2)* | 2.0 | 4.3 | 2.0 | 5.2 | 2.0 | 7.3 | ns |
| $t_{INSU}$ *(3)* | 2.4 | | 2.9 | | | | ns |
| $t_{INH}$ *(3)* | 0.0 | | 0.0 | | | | ns |
| $t_{OUTCO}$ *(3)* | 0.5 | 3.3 | 0.5 | 4.1 | | | ns |
| $t_{PCISU}$ | 2.4 | | 2.9 | | – | | ns |
| $t_{PCIH}$ | 0.0 | | 0.0 | | – | | ns |
| $t_{PCICO}$ | 2.0 | 6.0 | 2.0 | 7.7 | – | – | ns |

*Table 72. EPF10K50S External Bidirectional Timing Parameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ *(2)* | 2.7 | | 3.2 | | 4.3 | | ns |
| $t_{INHBIDIR}$ *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INHBIDIR}$ *(3)* | 0.0 | | 0.0 | | – | | ns |
| $t_{INSUBIDIR}$ *(3)* | 3.7 | | 4.2 | | – | | ns |
| $t_{OUTCOBIDIR}$ *(2)* | 2.0 | 4.5 | 2.0 | 5.2 | 2.0 | 7.3 | ns |
| $t_{XZBIDIR}$ *(2)* | | 6.8 | | 7.8 | | 10.1 | ns |
| $t_{ZXBIDIR}$ *(2)* | | 6.8 | | 7.8 | | 10.1 | ns |
| $t_{OUTCOBIDIR}$ *(3)* | 0.5 | 3.5 | 0.5 | 4.2 | – | – | |
| $t_{XZBIDIR}$ *(3)* | | 6.8 | | 8.4 | | – | ns |
| $t_{ZXBIDIR}$ *(3)* | | 6.8 | | 8.4 | | – | ns |

***Notes to tables:***

(1) All timing parameters are described in Tables 24 through 30.
(2) This parameter is measured without use of the ClockLock or ClockBoost circuits.
(3) This parameter is measured with use of the ClockLock or ClockBoost circuits

**Table 77. EPF10K200S Device Interconnect Timing Microparameters (Part 2 of 2)** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{LABCASC}$ | | 0.5 | | 1.0 | | 1.4 | ns |

**Table 78. EPF10K200S External Timing Parameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 9.0 | | 12.0 | | 16.0 | ns |
| $t_{INSU}$ *(2)* | 3.1 | | 3.7 | | 4.7 | | ns |
| $t_{INH}$ *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(2)* | 2.0 | 3.7 | 2.0 | 4.4 | 2.0 | 6.3 | ns |
| $t_{INSU}$*(3)* | 2.1 | | 2.7 | | – | | ns |
| $t_{INH}$ *(3)* | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCO}$*(3)* | 0.5 | 2.7 | 0.5 | 3.4 | – | – | ns |
| $t_{PCISU}$ | 3.0 | | 4.2 | | – | | ns |
| $t_{PCIH}$ | 0.0 | | 0.0 | | – | | ns |
| $t_{PCICO}$ | 2.0 | 6.0 | 2.0 | 8.9 | – | – | ns |

**Table 79. EPF10K200S External Bidirectional Timing Parameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ *(2)* | 2.3 | | 3.4 | | 4.4 | | ns |
| $t_{INHBIDIR}$ *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSUBIDIR}$ *(3)* | 3.3 | | 4.4 | | – | | ns |
| $t_{INHBIDIR}$ *(3)* | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCOBIDIR}$ *(2)* | 2.0 | 3.7 | 2.0 | 4.4 | 2.0 | 6.3 | ns |
| $t_{XZBIDIR}$ *(2)* | | 6.9 | | 7.6 | | 9.2 | ns |
| $t_{ZXBIDIR}$ *(2)* | | 5.9 | | 6.6 | | – | ns |
| $t_{OUTCOBIDIR}$ *(3)* | 0.5 | 2.7 | 0.5 | 3.4 | – | – | ns |
| $t_{XZBIDIR}$ *(3)* | | 6.9 | | 7.6 | | 9.2 | ns |
| $t_{ZXBIDIR}$ *(3)* | | 5.9 | | 6.6 | | – | ns |

***Notes to tables:***

(1) All timing parameters are described in Tables 24 through 30 in this data sheet.
(2) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(3) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

SRAM configuration elements allow FLEX 10KE devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 85 ms and can be used to reconfigure an entire system dynamically. In-field upgrades can be performed by distributing new configuration files.

Before and during configuration, all I/O pins (except dedicated inputs, clock, or configuration pins) are pulled high by a weak pull-up resistor.

## Programming Files

Despite being function- and pin-compatible, FLEX 10KE devices are not programming- or configuration file-compatible with FLEX 10K or FLEX 10KA devices. A design therefore must be recompiled before it is transferred from a FLEX 10K or FLEX 10KA device to an equivalent FLEX 10KE device. This recompilation should be performed both to create a new programming or configuration file and to check design timing in FLEX 10KE devices, which has different timing characteristics than FLEX 10K or FLEX 10KA devices.

FLEX 10KE devices are generally pin-compatible with equivalent FLEX 10KA devices. In some cases, FLEX 10KE devices have fewer I/O pins than the equivalent FLEX 10KA devices. Table 81 shows which FLEX 10KE devices have fewer I/O pins than equivalent FLEX 10KA devices. However, power, ground, JTAG, and configuration pins are the same on FLEX 10KA and FLEX 10KE devices, enabling migration from a FLEX 10KA design to a FLEX 10KE design.