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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	832
Number of Logic Elements/Cells	6656
Total RAM Bits	65536
Number of I/O	186
Number of Gates	342000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k130eqc240-3n

Table 5. FLEX 10KE Performance

Application	Resources Used		Performance			Units
	LEs	EABs	-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	
16-bit loadable counter	16	0	285	250	200	MHz
16-bit accumulator	16	0	285	250	200	MHz
16-to-1 multiplexer (1)	10	0	3.5	4.9	7.0	ns
16-bit multiplier with 3-stage pipeline (2)	592	0	156	131	93	MHz
256 × 16 RAM read cycle speed (2)	0	1	196	154	118	MHz
256 × 16 RAM write cycle speed (2)	0	1	185	143	106	MHz

Notes:

- (1) This application uses combinatorial inputs and outputs.
 (2) This application uses registered inputs and outputs.

Table 6 shows FLEX 10KE performance for more complex designs. These designs are available as Altera MegaCore® functions.

Table 6. FLEX 10KE Performance for Complex Designs

Application	LEs Used	Performance			Units
		-1 Speed Grade	-2 Speed Grade	-3 Speed Grade	
8-bit, 16-tap parallel finite impulse response (FIR) filter	597	192	156	116	MSPS
8-bit, 512-point fast Fourier transform (FFT) function	1,854	23.4	28.7	38.9	μs (1)
		113	92	68	MHz
a16450 universal asynchronous receiver/transmitter (UART)	342	36	28	20.5	MHz

Note:

- (1) These values are for calculation time. Calculation time = number of clocks required / $f_{\max}$. Number of clocks required = ceiling $[\log_2 (\text{points})/2] \times [\text{points} + 14 + \text{ceiling}]$



For more information on FLEX device configuration, see the following documents:

- *Configuration Devices for APEX & FLEX Devices Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *MasterBlaster Download Cable Data Sheet*
- *Application Note 116 (Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices)*

FLEX 10KE devices are supported by the Altera development systems, which are integrated packages that offer schematic, text (including AHDL), and waveform design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, and device configuration. The Altera software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The Altera software works easily with common gate array EDA tools for synthesis and simulation. For example, the Altera software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the Altera software contains EDA libraries that use device-specific features such as carry chains, which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the Altera development system includes DesignWare functions that are optimized for the FLEX 10KE architecture.

The Altera development system runs on Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800.

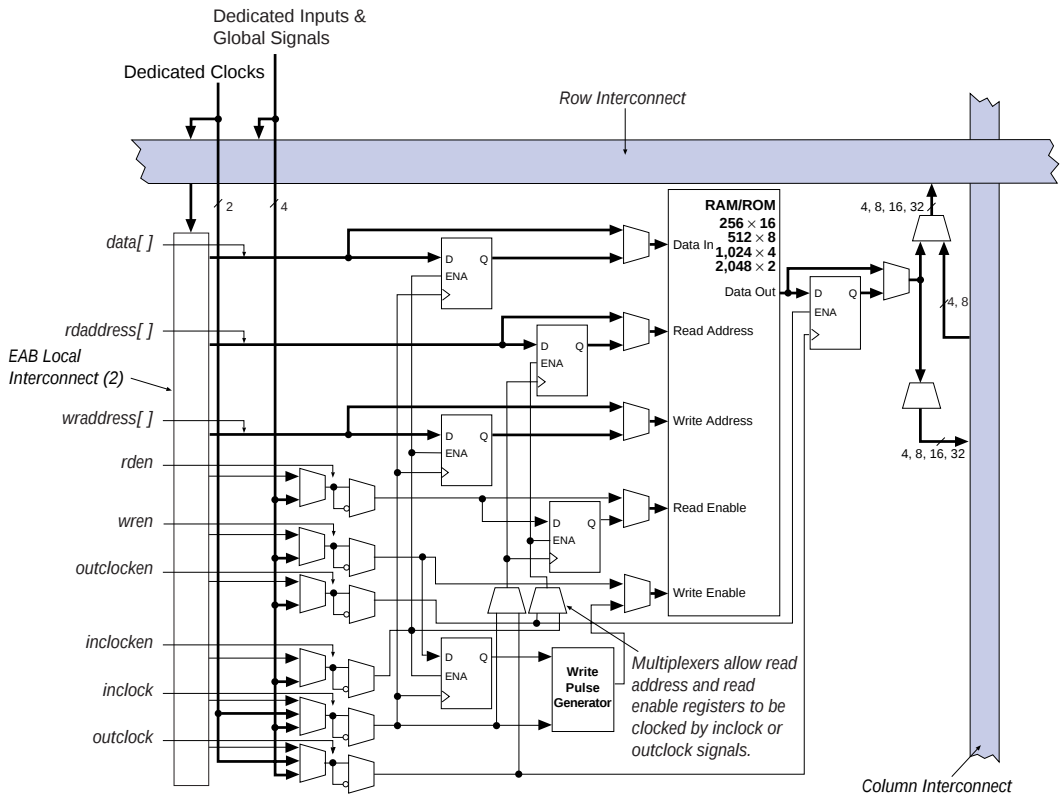


See the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet* for more information.

The EAB can also be used for bidirectional, dual-port memory applications where two ports read or write simultaneously. To implement this type of dual-port memory, two EABs are used to support two simultaneous read or writes.

Alternatively, one clock and clock enable can be used to control the input registers of the EAB, while a different clock and clock enable control the output registers (see Figure 2).

Figure 2. FLEX 10KE Device in Dual-Port RAM Mode Notes (1)



Notes:

- (1) All registers can be asynchronously cleared by EAB local interconnect signals, global signals, or the chip-wide reset.
- (2) EPF10K30E and EPF10K50E devices have 88 EAB local interconnect channels; EPF10K100E, EPF10K130E, and EPF10K200E devices have 104 EAB local interconnect channels.

EABs provide flexible options for driving and controlling clock signals. Different clocks and clock enables can be used for reading and writing to the EAB. Registers can be independently inserted on the data input, EAB output, write address, write enable signals, read address, and read enable signals. The global signals and the EAB local interconnect can drive write enable, read enable, and clock enable signals. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control write enable, read enable, clear, clock, and clock enable signals.

An EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs (see [Figures 2 and 4](#)). The column interconnect, which is adjacent to the EAB, has twice as many channels as other columns in the device.

Logic Array Block

An LAB consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure to the FLEX 10KE architecture, facilitating efficient routing with optimum device utilization and high performance (see [Figure 7](#)).

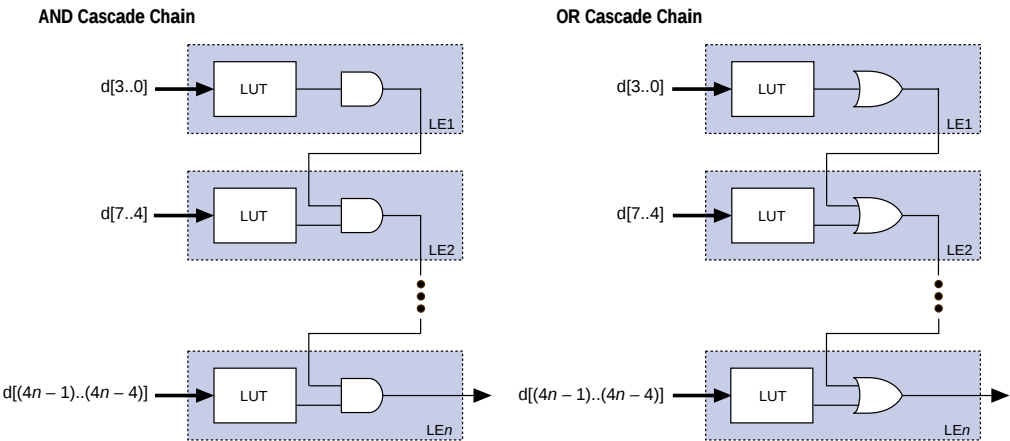
Cascade Chain

With the cascade chain, the FLEX 10KE architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. An a delay as low as 0.6 ns per LE, each additional LE provides four more inputs to the effective width of a function. Cascade chain logic can be created automatically by the Altera Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than eight bits are implemented automatically by linking several LABs together. For easier routing, a long cascade chain skips every other LAB in a row. A cascade chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB (e.g., the last LE of the first LAB in a row cascades to the first LE of the third LAB). The cascade chain does not cross the center of the row (e.g., in the EPF10K50E device, the cascade chain stops at the eighteenth LAB and a new one begins at the nineteenth LAB). This break is due to the EAB's placement in the middle of the row.

Figure 10 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of $4n$ variables implemented with n LEs. The LE delay is 0.9 ns; the cascade chain delay is 0.6 ns. With the cascade chain, 2.7 ns are needed to decode a 16-bit address.

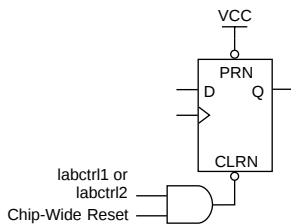
Figure 10. FLEX 10KE Cascade Chain Operation



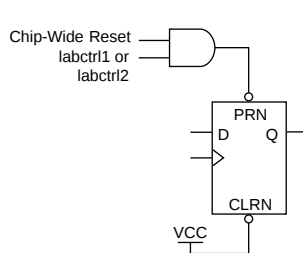
In addition to the six clear and preset modes, FLEX 10KE devices provide a chip-wide reset pin that can reset all registers in the device. Use of this feature is set during design entry. In any of the clear and preset modes, the chip-wide reset overrides all other signals. Registers with asynchronous presets may be preset when the chip-wide reset is asserted. Inversion can be used to implement the asynchronous preset. Figure 12 shows examples of how to setup the preset and clear inputs for the desired functionality.

Figure 12. FLEX 10KE LE Clear & Preset Modes

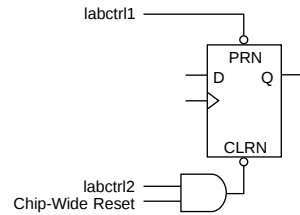
Asynchronous Clear



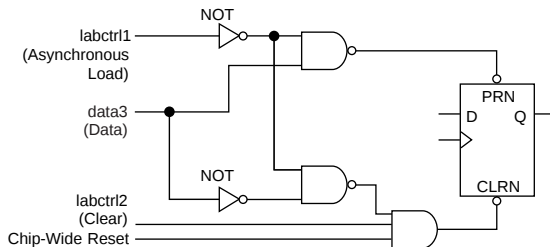
Asynchronous Preset



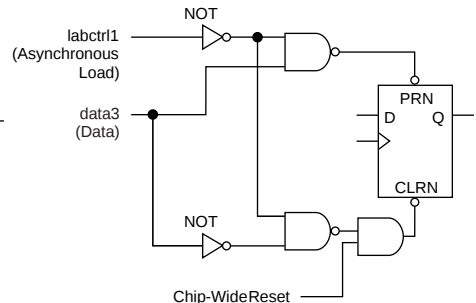
Asynchronous Preset & Clear



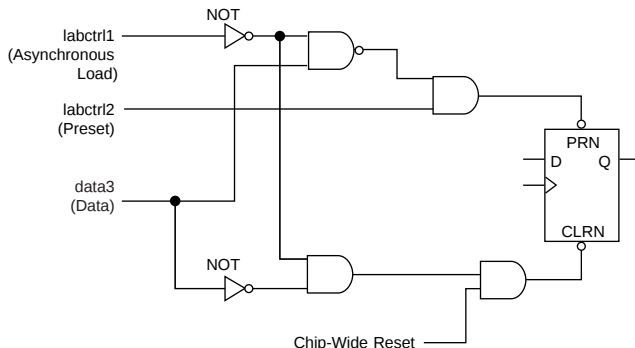
Asynchronous Load with Clear



Asynchronous Load without Clear or Preset



Asynchronous Load with Preset



FastTrack Interconnect Routing Structure

In the FLEX 10KE architecture, connections between LEs, EABs, and device I/O pins are provided by the FastTrack Interconnect routing structure, which is a series of continuous horizontal and vertical routing channels that traverses the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

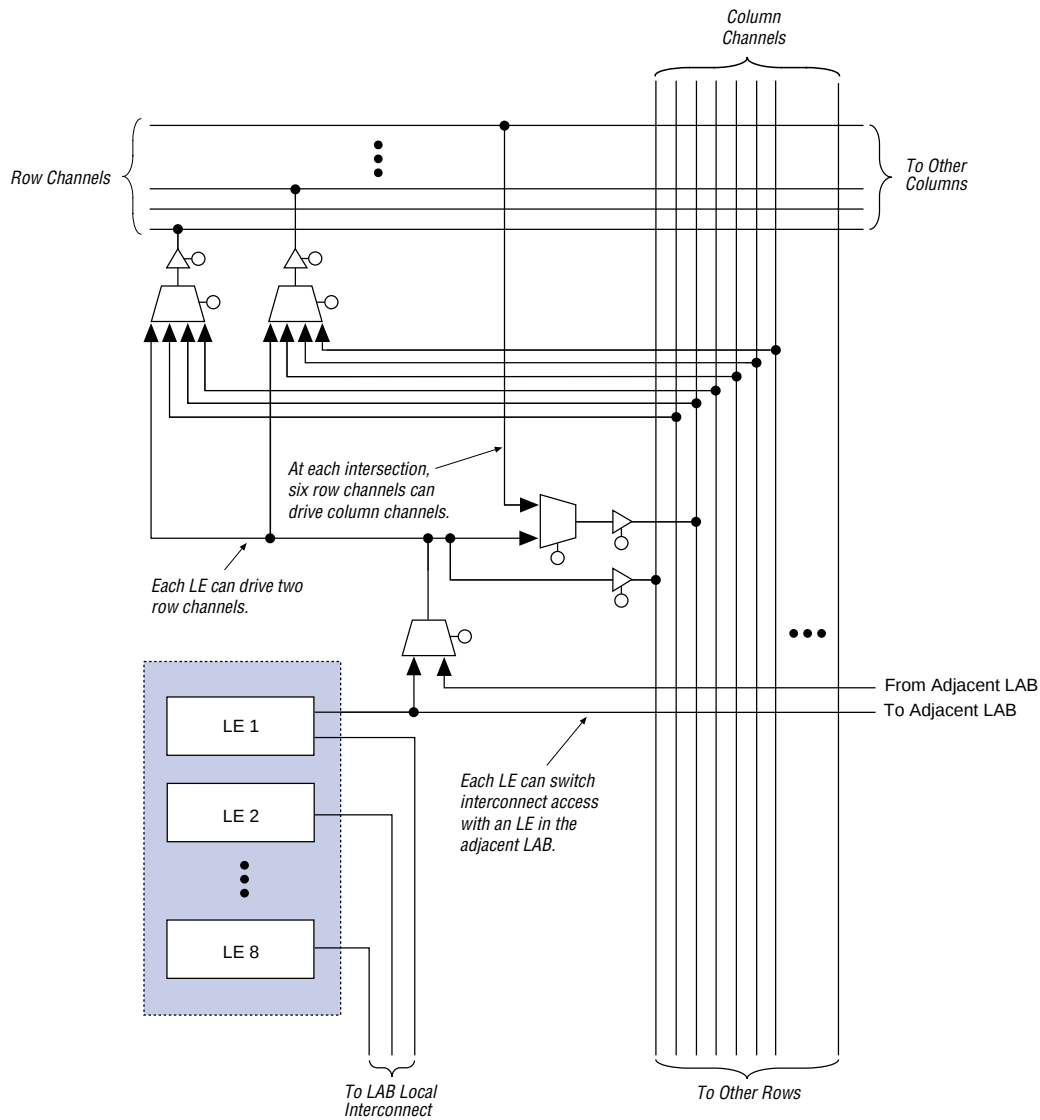
The FastTrack Interconnect routing structure consists of row and column interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect. The row interconnect can drive I/O pins and feed other LABs in the row. The column interconnect routes signals between rows and can drive I/O pins.

Row channels drive into the LAB or EAB local interconnect. The row signal is buffered at every LAB or EAB to reduce the effect of fan-out on delay. A row channel can be driven by an LE or by one of three column channels. These four signals feed dual 4-to-1 multiplexers that connect to two specific row channels. These multiplexers, which are connected to each LE, allow column channels to drive row channels even when all eight LEs in a LAB drive the row interconnect.

Each column of LABs or EABs is served by a dedicated column interconnect. The column interconnect that serves the EABs has twice as many channels as other column interconnects. The column interconnect can then drive I/O pins or another row's interconnect to route the signals to other LABs or EABs in the device. A signal from the column interconnect, which can be either the output of a LE or an input from an I/O pin, must be routed to the row interconnect before it can enter a LAB or EAB. Each row channel that is driven by an IOE or EAB can drive one specific column channel.

Access to row and column channels can be switched between LEs in adjacent pairs of LABs. For example, a LE in one LAB can drive the row and column channels normally driven by a particular LE in the adjacent LAB in the same row, and vice versa. This flexibility enables routing resources to be used more efficiently (see [Figure 13](#)).

Figure 13. FLEX 10KE LAB Connections to Row & Column Interconnect



Tables 12 and 13 summarize the ClockLock and ClockBoost parameters for -1 and -2 speed-grade devices, respectively.

Table 12. ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)		25		180	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)		16		90	MHz
f_{CLKDEV}	Input deviation from user specification in the MAX+PLUS II software (1)				25,000 (2)	PPM
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)				100	ps
t_{LOCK}	Time required for ClockLock or ClockBoost to acquire lock (3)				10	μs
t_{JITTER}	Jitter on ClockLock or ClockBoost-generated clock (4)	$t_{INCLKSTB} < 100$			250	ps
		$t_{INCLKSTB} < 50$			200 (4)	ps
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		40	50	60	%

Figure 20 shows the timing requirements for the JTAG signals.

Figure 20. FLEX 10KE JTAG Waveforms

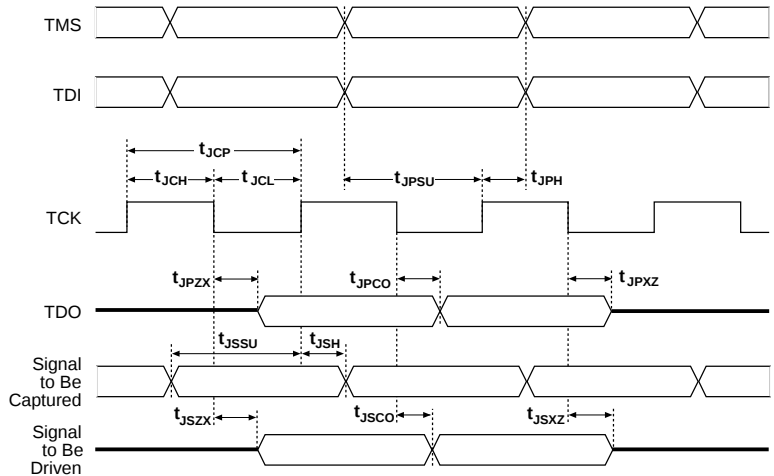


Table 18 shows the timing parameters and values for FLEX 10KE devices.

Table 18. FLEX 10KE JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

Table 20. 2.5-V EPF10K50E & EPF10K200E Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CCINT}	Supply voltage for internal logic and input buffers	(3), (4)	2.30 (2.30)	2.70 (2.70)	V
V _{CCIO}	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(3), (4)	2.30 (2.30)	2.70 (2.70)	V
V _I	Input voltage	(5)	−0.5	5.75	V
V _O	Output voltage		0	V _{CCIO}	V
T _A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	−40	85	° C
T _J	Operating temperature	For commercial use	0	85	° C
		For industrial use	−40	100	° C
t _R	Input rise time			40	ns
t _F	Input fall time			40	ns

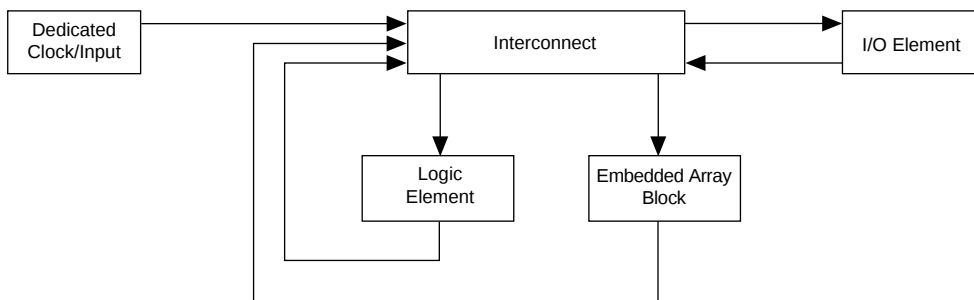
Table 21. 2.5-V EPF10K30E, EPF10K50S, EPF10K100E, EPF10K130E & EPF10K200S Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CCINT}	Supply voltage for internal logic and input buffers	(3), (4)	2.375 (2.375)	2.625 (2.625)	V
V _{CCIO}	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(3), (4)	2.375 (2.375)	2.625 (2.625)	V
V _I	Input voltage	(5)	−0.5	5.75	V
V _O	Output voltage		0	V _{CCIO}	V
T _A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	−40	85	° C
T _J	Operating temperature	For commercial use	0	85	° C
		For industrial use	−40	100	° C
t _R	Input rise time			40	ns
t _F	Input fall time			40	ns

Timing simulation and delay prediction are available with the Altera Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

Figure 24 shows the overall timing model, which maps the possible paths to and from the various elements of the FLEX 10KE device.

Figure 24. FLEX 10KE Device Timing Model



Figures 25 through 28 show the delays that correspond to various paths and functions within the LE, IOE, EAB, and bidirectional timing models.

Figure 26. FLEX 10KE Device IOE Timing Model

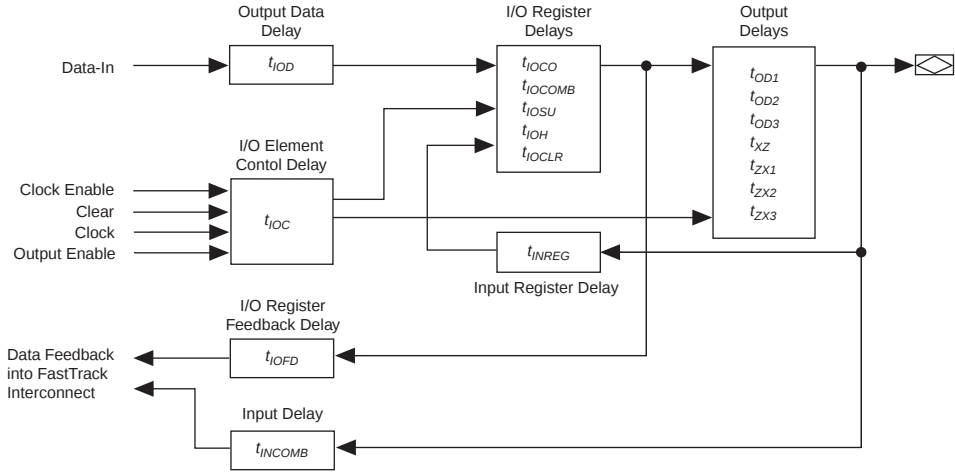


Figure 27. FLEX 10KE Device EAB Timing Model

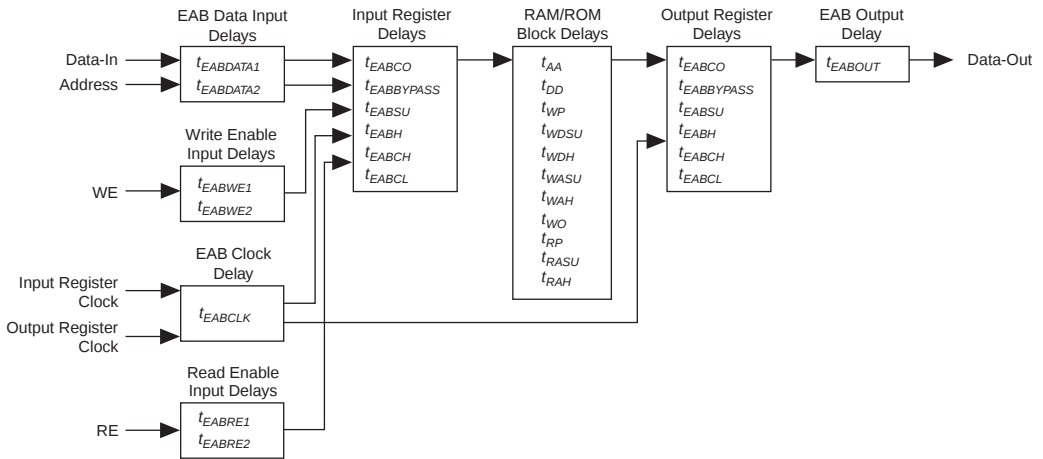


Table 27. EAB Timing Macroparameters *Note (1), (6)*

Symbol	Parameter	Conditions
t_{EABAA}	EAB address access delay	
$t_{EABRCCOMB}$	EAB asynchronous read cycle time	
$t_{EABRCREG}$	EAB synchronous read cycle time	
t_{EABWP}	EAB write pulse width	
$t_{EABWCCOMB}$	EAB asynchronous write cycle time	
$t_{EABWCREG}$	EAB synchronous write cycle time	
t_{EABDD}	EAB data-in to data-out valid delay	
$t_{EABDATAO}$	EAB clock-to-output delay when using output registers	
$t_{EABDATASU}$	EAB data/address setup time before clock when using input register	
$t_{EABDATAH}$	EAB data/address hold time after clock when using input register	
$t_{EABWESU}$	EAB WE setup time before clock when using input register	
t_{EABWEH}	EAB WE hold time after clock when using input register	
$t_{EABWDSU}$	EAB data setup time before falling edge of write pulse when not using input registers	
t_{EABWDH}	EAB data hold time after falling edge of write pulse when not using input registers	
$t_{EABWASU}$	EAB address setup time before rising edge of write pulse when not using input registers	
t_{EABWAH}	EAB address hold time after falling edge of write pulse when not using input registers	
t_{EABWO}	EAB write enable to data output valid delay	

Table 30. External Bidirectional Timing Parameters *Note (9)*

Symbol	Parameter	Conditions
$t_{\text{INSUBIDIR}}$	Setup time for bi-directional pins with global clock at same-row or same-column LE register	
t_{INHBIDIR}	Hold time for bidirectional pins with global clock at same-row or same-column LE register	
t_{INH}	Hold time with global clock at IOE register	
$t_{\text{OUTCOBIDIR}}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	C1 = 35 pF
t_{XZBIDIR}	Synchronous IOE output buffer disable delay	C1 = 35 pF
t_{ZXBIDIR}	Synchronous IOE output buffer enable delay, slow slew rate= off	C1 = 35 pF

Notes to tables:

- (1) Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.
- (2) Operating conditions: VCCIO = 3.3 V $\pm$ 10% for commercial or industrial use.
- (3) Operating conditions: VCCIO = 2.5 V $\pm$ 5% for commercial or industrial use in EPF10K30E, EPF10K50S, EPF10K100E, EPF10K130E, and EPF10K200S devices.
- (4) Operating conditions: VCCIO = 3.3 V.
- (5) Because the RAM in the EAB is self-timed, this parameter can be ignored when the WE signal is registered.
- (6) EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.
- (7) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.
- (8) Contact Altera Applications for test circuit specifications and test conditions.
- (9) This timing parameter is sample-tested only.
- (10) This parameter is measured with the measurement and test conditions, including load, specified in the PCI Local Bus Specification, revision 2.2.

Table 35. EPF10K30E Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		1.8		2.4		2.9	ns
t_{DIN2LE}		1.5		1.8		2.4	ns
$t_{DIN2DATA}$		1.5		1.8		2.2	ns
$t_{DCLK2IOE}$		2.2		2.6		3.0	ns
$t_{DCLK2LE}$		1.5		1.8		2.4	ns
$t_{SAMELAB}$		0.1		0.2		0.3	ns
$t_{SAMEROW}$		2.0		2.4		2.7	ns
$t_{SAMECOLUMN}$		0.7		1.0		0.8	ns
$t_{DIFFROW}$		2.7		3.4		3.5	ns
$t_{TWOROWS}$		4.7		5.8		6.2	ns
$t_{LEPERIPH}$		2.7		3.4		3.8	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.8		0.8		1.1	ns

Table 36. EPF10K30E External Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DDR}		8.0		9.5		12.5	ns
$t_{INSU}^{(3)}$	2.1		2.5		3.9		ns
$t_{INH}^{(3)}$	0.0		0.0		0.0		ns
$t_{OUTCO}^{(3)}$	2.0	4.9	2.0	5.9	2.0	7.6	ns
$t_{INSU}^{(4)}$	1.1		1.5		—		ns
$t_{INH}^{(4)}$	0.0		0.0		—		ns
$t_{OUTCO}^{(4)}$	0.5	3.9	0.5	4.9	—	—	ns
t_{PCISU}	3.0		4.2		—		ns
t_{PCIH}	0.0		0.0		—		ns
t_{PCICO}	2.0	6.0	2.0	7.5	—	—	ns

Table 56. EPF10K130E Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		2.8		3.5		4.4	ns
t_{DIN2LE}		0.7		1.2		1.6	ns
$t_{DIN2DATA}$		1.6		1.9		2.2	ns
$t_{DCLK2IOE}$		1.6		2.1		2.7	ns
$t_{DCLK2LE}$		0.7		1.2		1.6	ns
$t_{SAMELAB}$		0.1		0.2		0.2	ns
$t_{SAMEROW}$		1.9		3.4		5.1	ns
$t_{SAMECOLUMN}$		0.9		2.6		4.4	ns
$t_{DIFFROW}$		2.8		6.0		9.5	ns
$t_{TWOROWS}$		4.7		9.4		14.6	ns
$t_{LEPERIPH}$		3.1		4.7		6.9	ns
$t_{LABCARRY}$		0.6		0.8		1.0	ns
$t_{LABCASC}$		0.9		1.2		1.6	ns

Table 57. EPF10K130E External Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		9.0		12.0		16.0	ns
$t_{INSU}^{(3)}$	1.9		2.1		3.0		ns
$t_{INH}^{(3)}$	0.0		0.0		0.0		ns
$t_{OUTCO}^{(3)}$	2.0	5.0	2.0	7.0	2.0	9.2	ns
$t_{INSU}^{(4)}$	0.9		1.1		—		ns
$t_{INH}^{(4)}$	0.0		0.0		—		ns
$t_{OUTCO}^{(4)}$	0.5	4.0	0.5	6.0	—	—	ns
t_{PCISU}	3.0		6.2		—		ns
t_{PCIH}	0.0		0.0		—		ns
t_{PCICO}	2.0	6.0	2.0	6.9	—	—	ns

Table 74. EPF10K200S Device IOE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ZX2}		4.5		4.8		6.6	ns
t_{ZX3}		6.6		7.6		10.1	ns
t_{INREG}		3.7		5.7		7.7	ns
t_{IOFD}		1.8		3.4		4.0	ns
t_{INCOMB}		1.8		3.4		4.0	ns

Table 75. EPF10K200S Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.8		2.4		3.2	ns
$t_{EABDATA1}$		0.4		0.5		0.6	ns
t_{EABWE1}		1.1		1.7		2.3	ns
t_{EABWE2}		0.0		0.0		0.0	ns
t_{EABRE1}		0		0		0	ns
t_{EABRE2}		0.4		0.5		0.6	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.8		0.9		1.2	ns
$t_{EABYPASS}$		0.0		0.1		0.1	ns
t_{EABSU}	0.7		1.1		1.5		ns
t_{EABH}	0.4		0.5		0.6		ns
t_{EABCLR}	0.8		0.9		1.2		ns
t_{AA}		2.1		3.7		4.9	ns
t_{WP}	2.1		4.0		5.3		ns
t_{RP}	1.1		1.1		1.5		ns
t_{WDSU}	0.5		1.1		1.5		ns
t_{WDH}	0.1		0.1		0.1		ns
t_{WASU}	1.1		1.6		2.1		ns
t_{WAH}	1.6		2.5		3.3		ns
t_{RASU}	1.6		2.6		3.5		ns
t_{RAH}	0.1		0.1		0.2		ns
t_{WO}		2.0		2.4		3.2	ns
t_{DD}		2.0		2.4		3.2	ns
t_{EABOUT}		0.0		0.1		0.1	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	2.1		2.8		3.8		ns

Additionally, the Altera software offers several features that help plan for future device migration by preventing the use of conflicting I/O pins.

Table 81. I/O Counts for FLEX 10KA & FLEX 10KE Devices

FLEX 10KA		FLEX 10KE	
Device	I/O Count	Device	I/O Count
EPF10K30AF256	191	EPF10K30EF256	176
EPF10K30AF484	246	EPF10K30EF484	220
EPF10K50VB356	274	EPF10K50SB356	220
EPF10K50VF484	291	EPF10K50EF484	254
EPF10K50VF484	291	EPF10K50SF484	254
EPF10K100AF484	369	EPF10K100EF484	338

Configuration Schemes

The configuration data for a FLEX 10KE device can be loaded with one of five configuration schemes (see [Table 82](#)), chosen on the basis of the target application. An EPC1, EPC2, or EPC16 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of a FLEX 10KE device, allowing automatic configuration on system power-up.

Multiple FLEX 10KE devices can be configured in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device. Additional FLEX 10K, FLEX 10KA, FLEX 10KE, and FLEX 6000 devices can be configured in the same serial chain.

Table 82. Data Sources for FLEX 10KE Configuration

Configuration Scheme	Data Source
Configuration device	EPC1, EPC2, or EPC16 configuration device
Passive serial (PS)	BitBlaster, ByteBlasterMV, or MasterBlaster download cables, or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	BitBlaster or ByteBlasterMV download cables, or microprocessor with a Jam STAPL file or JBC file

Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the Altera Digital Library for pin-out information.

Revision History

The information contained in the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.5 supersedes information published in previous versions.

Version 2.5

The following changes were made to the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.5:

- *Note (1)* added to *Figure 23*.
- Text added to “I/O Element” section on *page 34*.
- Updated *Table 22*.

Version 2.4

The following changes were made to the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.4: updated text on *page 34* and *page 63*.