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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	1248
Number of Logic Elements/Cells	9984
Total RAM Bits	98304
Number of I/O	274
Number of Gates	513000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	356-LBGA
Supplier Device Package	356-BGA (35x35)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=epf10k200sbc356-1

- Software design support and automatic place-and-route provided by Altera’s development systems for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800
- Flexible package options
 - Available in a variety of packages with 144 to 672 pins, including the innovative FineLine BGA™ packages (see [Tables 3 and 4](#))
 - SameFrame™ pin-out compatibility between FLEX 10KA and FLEX 10KE devices across a range of device densities and pin counts
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), DesignWare components, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, VeriBest, and Viewlogic

Table 3. FLEX 10KE Package Options & I/O Pin Count *Notes (1), (2)*

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP RQFP	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA	599-Pin PGA	600-Pin BGA	672-Pin FineLine BGA
EPF10K30E	102	147		176		220			220 (3)
EPF10K50E	102	147	189	191		254			254 (3)
EPF10K50S	102	147	189	191	220	254			254 (3)
EPF10K100E		147	189	191	274	338			338 (3)
EPF10K130E			186		274	369		424	413
EPF10K200E							470	470	470
EPF10K200S			182		274	369	470	470	470

Notes:

- (1) FLEX 10KE device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), pin-grid array (PGA), and ball-grid array (BGA) packages.
- (2) Devices in the same package are pin-compatible, although some devices have more I/O pins than others. When planning device migration, use the I/O pins that are common to all devices.
- (3) This option is supported with a 484-pin FineLine BGA package. By using SameFrame pin migration, all FineLine BGA packages are pin-compatible. For example, a board can be designed to support 256-pin, 484-pin, and 672-pin FineLine BGA packages. The Altera software automatically avoids conflicting pins when future migration is set.

Table 4. FLEX 10KE Package Sizes

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP RQFP	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA	599-Pin PGA	600-Pin BGA	672-Pin FineLine BGA
Pitch (mm)	0.50	0.50	0.50	1.0	1.27	1.0	–	1.27	1.0
Area (mm ²)	484	936	1,197	289	1,225	529	3,904	2,025	729
Length × width (mm × mm)	22 × 22	30.6 × 30.6	34.6 × 34.6	17 × 17	35 × 35	23 × 23	62.5 × 62.5	45 × 45	27 × 27

General Description

Altera FLEX 10KE devices are enhanced versions of FLEX 10K devices. Based on reconfigurable CMOS SRAM elements, the FLEX architecture incorporates all features necessary to implement common gate array megafunctions. With up to 200,000 typical gates, FLEX 10KE devices provide the density, speed, and features to integrate entire systems, including multiple 32-bit buses, into a single device.

The ability to reconfigure FLEX 10KE devices enables 100% testing prior to shipment and allows the designer to focus on simulation and design verification. FLEX 10KE reconfigurability eliminates inventory management for gate array designs and generation of test vectors for fault coverage.

Table 5 shows FLEX 10KE performance for some common designs. All performance values were obtained with Synopsys DesignWare or LPM functions. Special design techniques are not required to implement the applications; the designer simply infers or instantiates a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.



For more information on FLEX device configuration, see the following documents:

- [*Configuration Devices for APEX & FLEX Devices Data Sheet*](#)
- [*BitBlaster Serial Download Cable Data Sheet*](#)
- [*ByteBlasterMV Parallel Port Download Cable Data Sheet*](#)
- [*MasterBlaster Download Cable Data Sheet*](#)
- [*Application Note 116 \(Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices\)*](#)

FLEX 10KE devices are supported by the Altera development systems, which are integrated packages that offer schematic, text (including AHDL), and waveform design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, and device configuration. The Altera software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The Altera software works easily with common gate array EDA tools for synthesis and simulation. For example, the Altera software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the Altera software contains EDA libraries that use device-specific features such as carry chains, which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the Altera development system includes DesignWare functions that are optimized for the FLEX 10KE architecture.

The Altera development system runs on Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800.



See the [*MAX+PLUS II Programmable Logic Development System & Software Data Sheet*](#) and the [*Quartus Programmable Logic Development System & Software Data Sheet*](#) for more information.

LE Operating Modes

The FLEX 10KE LE can operate in the following four modes:

- Normal mode
- Arithmetic mode
- Up/down counter mode
- Clearable counter mode

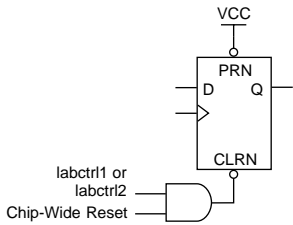
Each of these modes uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. Three inputs to the LE provide clock, clear, and preset control for the register. The Altera software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that use a specific LE operating mode for optimal performance.

The architecture provides a synchronous clock enable to the register in all four modes. The Altera software can set `DATA1` to enable the register synchronously, providing easy implementation of fully synchronous designs.

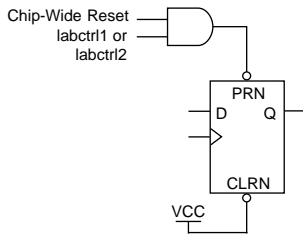
In addition to the six clear and preset modes, FLEX 10KE devices provide a chip-wide reset pin that can reset all registers in the device. Use of this feature is set during design entry. In any of the clear and preset modes, the chip-wide reset overrides all other signals. Registers with asynchronous presets may be preset when the chip-wide reset is asserted. Inversion can be used to implement the asynchronous preset. Figure 12 shows examples of how to setup the preset and clear inputs for the desired functionality.

Figure 12. FLEX 10KE LE Clear & Preset Modes

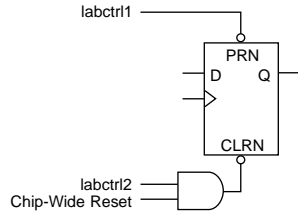
Asynchronous Clear



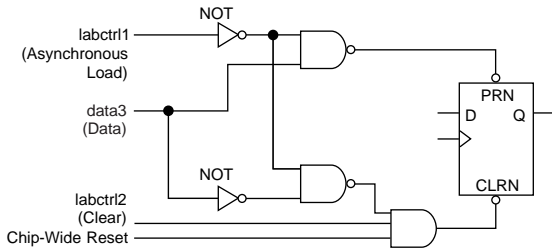
Asynchronous Preset



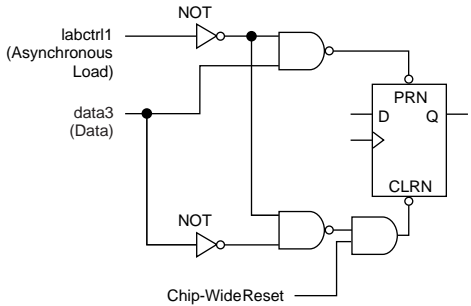
Asynchronous Preset & Clear



Asynchronous Load with Clear



Asynchronous Load without Clear or Preset



Asynchronous Load with Preset

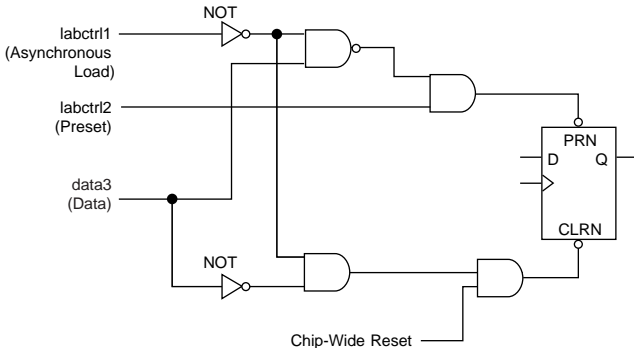
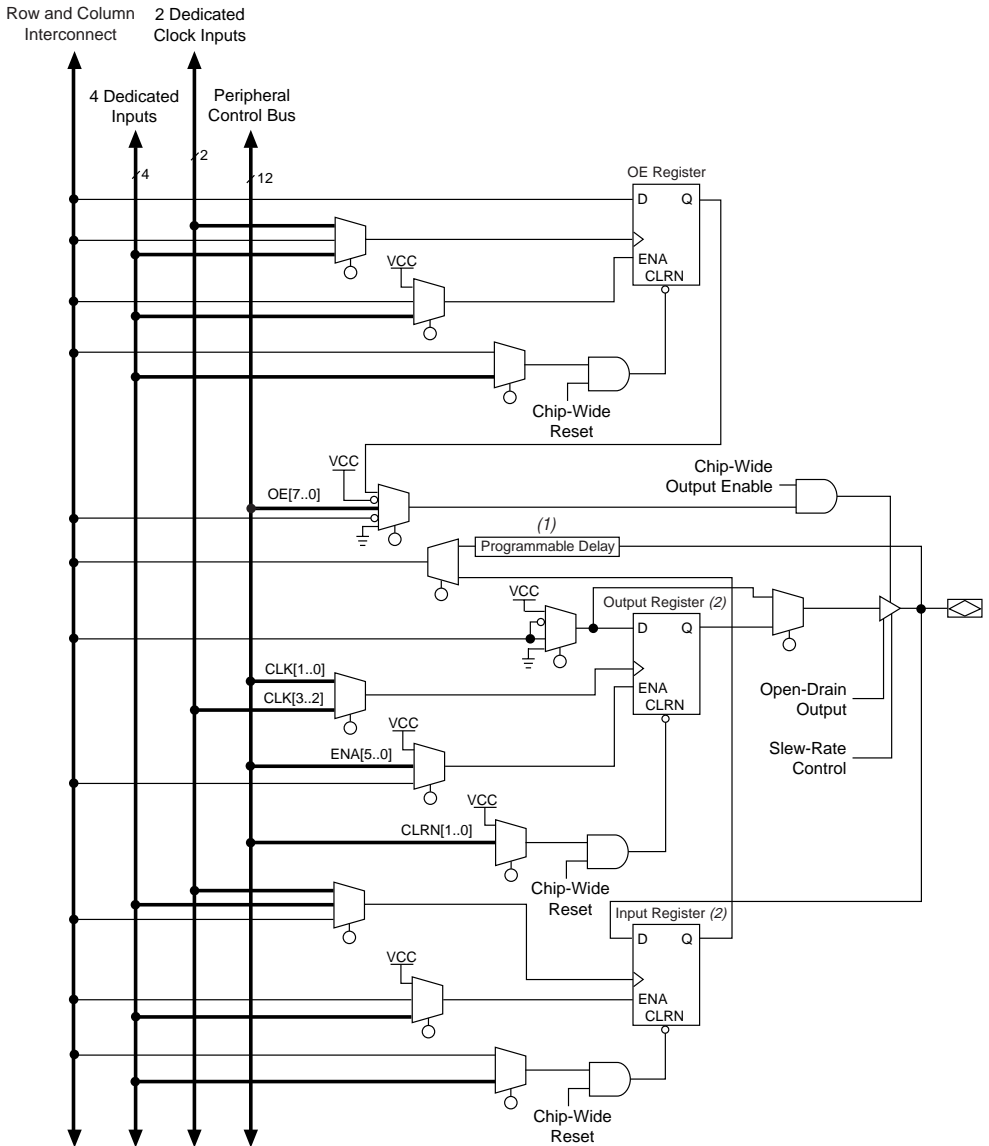


Figure 15. FLEX 10KE Bidirectional I/O Registers



Note:

- (1) All FLEX 10KE devices (except the EPF10K50E and EPF10K200E devices) have a programmable input delay buffer on the input path.

When dedicated inputs drive non-inverted and inverted peripheral clears, clock enables, and output enables, two signals on the peripheral control bus will be used.

Tables 8 and 9 list the sources for each peripheral control signal, and show how the output enable, clock enable, clock, and clear signals share 12 peripheral control signals. The tables also show the rows that can drive global signals.

Table 8. Peripheral Bus Sources for EPF10K30E, EPF10K50E & EPF10K50S Devices

Peripheral Control Signal	EPF10K30E	EPF10K50E EPF10K50S
OE0	Row A	Row A
OE1	Row B	Row B
OE2	Row C	Row D
OE3	Row D	Row F
OE4	Row E	Row H
OE5	Row F	Row J
CLKENA0 / CLK0 / GLOBAL0	Row A	Row A
CLKENA1 / OE6 / GLOBAL1	Row B	Row C
CLKENA2 / CLR0	Row C	Row E
CLKENA3 / OE7 / GLOBAL2	Row D	Row G
CLKENA4 / CLR1	Row E	Row I
CLKENA5 / CLK1 / GLOBAL3	Row F	Row J

Table 9. Peripheral Bus Sources for EPF10K100E, EPF10K130E, EPF10K200E & EPF10K200S Devices

Peripheral Control Signal	EPF10K100E	EPF10K130E	EPF10K200E EPF10K200S
OE0	Row A	Row C	Row G
OE1	Row C	Row E	Row I
OE2	Row E	Row G	Row K
OE3	Row L	Row N	Row R
OE4	Row I	Row K	Row O
OE5	Row K	Row M	Row Q
CLKENA0/CLK0/GLOBAL0	Row F	Row H	Row L
CLKENA1/OE6/GLOBAL1	Row D	Row F	Row J
CLKENA2/CLR0	Row B	Row D	Row H
CLKENA3/OE7/GLOBAL2	Row H	Row J	Row N
CLKENA4/CLR1	Row J	Row L	Row P
CLKENA5/CLK1/GLOBAL3	Row G	Row I	Row M

Signals on the peripheral control bus can also drive the four global signals, referred to as GLOBAL0 through GLOBAL3 in [Tables 8 and 9](#). An internally generated signal can drive a global signal, providing the same low-skew, low-delay characteristics as a signal driven by an input pin. An LE drives the global signal by driving a row line that drives the peripheral bus, which then drives the global signal. This feature is ideal for internally generated clear or clock signals with high fan-out. However, internally driven global signals offer no advantage over the general-purpose interconnect for routing data signals. The dedicated input pin should be driven to a known logic state (such as ground) and not be allowed to float.

The chip-wide output enable pin is an active-high pin (DEV_OE) that can be used to tri-state all pins on the device. This option can be set in the Altera software. On EPF10K50E and EPF10K200E devices, the built-in I/O pin pull-up resistors (which are active during configuration) are active when the chip-wide output enable pin is asserted. The registers in the IOE can also be reset by the chip-wide reset pin.

Table 13. ClockLock & ClockBoost Parameters for -2 Speed-Grade Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)		25		75	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)		16		37.5	MHz
f_{CLKDEV}	Input deviation from user specification in the MAX+PLUS II software (1)				25,000 (2)	PPM
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)				100	ps
t_{LOCK}	Time required for ClockLock or ClockBoost to acquire lock (3)				10	μ s
t_{JITTER}	Jitter on ClockLock or ClockBoost-generated clock (4)	$t_{INCLKSTB} < 100$			250	ps
		$t_{INCLKSTB} < 50$			200 (4)	ps
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		40	50	60	%

Notes to tables:

- (1) To implement the ClockLock and ClockBoost circuitry with the MAX+PLUS II software, designers must specify the input frequency. The Altera software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The f_{CLKDEV} parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.
- (2) Twenty-five thousand parts per million (PPM) equates to 2.5% of input clock period.
- (3) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration because the t_{LOCK} value is less than the time required for configuration.
- (4) The t_{JITTER} specification is measured under long-term observation. The maximum value for t_{JITTER} is 200 ps if $t_{INCLKSTB}$ is lower than 50 ps.

I/O Configuration

This section discusses the peripheral component interconnect (PCI) pull-up clamping diode option, slew-rate control, open-drain output option, and MultiVolt I/O interface for FLEX 10KE devices. The PCI pull-up clamping diode, slew-rate control, and open-drain output options are controlled pin-by-pin via Altera software logic options. The MultiVolt I/O interface is controlled by connecting V_{CCIO} to a different voltage than V_{CCINT} . Its effect can be simulated in the Altera software via the **Global Project Device Options** dialog box (Assign menu).

Table 17. 32-Bit IDCODE for FLEX 10KE Devices Note (1)

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) (2)
EPF10K30E	0001	0001 0000 0011 0000	00001101110	1
EPF10K50E EPF10K50S	0001	0001 0000 0101 0000	00001101110	1
EPF10K100E	0010	0000 0001 0000 0000	00001101110	1
EPF10K130E	0001	0000 0001 0011 0000	00001101110	1
EPF10K200E EPF10K200S	0001	0000 0010 0000 0000	00001101110	1

Notes:

- (1) The most significant bit (MSB) is on the left.
- (2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

FLEX 10KE devices include weak pull-up resistors on the JTAG pins.



For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Jam Programming & Test Language Specification*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V_{IH}	High-level input voltage		1.7, $0.5 \times V_{CCIO}$ (8)		5.75	V	
V_{IL}	Low-level input voltage		-0.5		0.8, $0.3 \times V_{CCIO}$ (8)	V	
V_{OH}	3.3-V high-level TTL output voltage	$I_{OH} = -8$ mA DC, $V_{CCIO} = 3.00$ V (9)	2.4			V	
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (9)	$V_{CCIO} - 0.2$			V	
	3.3-V high-level PCI output voltage	$I_{OH} = -0.5$ mA DC, $V_{CCIO} = 3.00$ to 3.60 V (9)	$0.9 \times V_{CCIO}$			V	
	2.5-V high-level output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 2.30$ V (9)	2.1			V	
		$I_{OH} = -1$ mA DC, $V_{CCIO} = 2.30$ V (9)	2.0			V	
		$I_{OH} = -2$ mA DC, $V_{CCIO} = 2.30$ V (9)	1.7			V	
V_{OL}	3.3-V low-level TTL output voltage	$I_{OL} = 12$ mA DC, $V_{CCIO} = 3.00$ V (10)			0.45	V	
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.00$ V (10)			0.2	V	
	3.3-V low-level PCI output voltage	$I_{OL} = 1.5$ mA DC, $V_{CCIO} = 3.00$ to 3.60 V (10)			$0.1 \times V_{CCIO}$	V	
	2.5-V low-level output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 2.30$ V (10)				0.2	V
		$I_{OL} = 1$ mA DC, $V_{CCIO} = 2.30$ V (10)				0.4	V
		$I_{OL} = 2$ mA DC, $V_{CCIO} = 2.30$ V (10)				0.7	V
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V (11)	-10		10	μ A	
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V (11)	-10		10	μ A	
I_{CC0}	V_{CC} supply current (standby)	$V_I =$ ground, no load, no toggling inputs		5		mA	
		$V_I =$ ground, no load, no toggling inputs (12)		10		mA	
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	$V_{CCIO} = 3.0$ V (13)	20		50	$k\frac{3}{4}$	
		$V_{CCIO} = 2.3$ V (13)	30		80	$k\frac{3}{4}$	

Table 23. FLEX 10KE Device Capacitance *Note (14)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	$V_{IN} = 0\text{ V}$, $f = 1.0\text{ MHz}$		10	pF
C_{INCLK}	Input capacitance on dedicated clock pin	$V_{IN} = 0\text{ V}$, $f = 1.0\text{ MHz}$		12	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0\text{ V}$, $f = 1.0\text{ MHz}$		10	pF

Notes to tables:

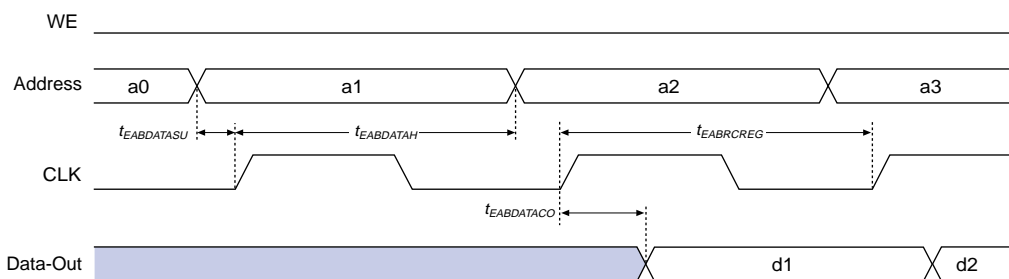
- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input voltage is -0.5 V . During transitions, the inputs may undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns .
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum V_{CC} rise time is 100 ms , and V_{CC} must rise monotonically.
- (5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
- (6) Typical values are for $T_A = 25^\circ\text{ C}$, $V_{CCINT} = 2.5\text{ V}$, and $V_{CCIO} = 2.5\text{ V}$ or 3.3 V .
- (7) These values are specified under the FLEX 10KE Recommended Operating Conditions shown in [Tables 20 and 21](#).
- (8) The FLEX 10KE input buffers are compatible with 2.5-V , 3.3-V (LVTTTL and LVCMOS), and 5.0-V TTL and CMOS signals. Additionally, the input buffers are 3.3-V PCI compliant when V_{CCIO} and V_{CCINT} meet the relationship shown in [Figure 22](#).
- (9) The I_{OH} parameter refers to high-level TTL, PCI, or CMOS output current.
- (10) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (11) This value is specified for normal device operation. The value may vary during power-up.
- (12) This parameter applies to -1 speed-grade commercial-temperature devices and -2 speed-grade-industrial temperature devices.
- (13) Pin pull-up resistance values will be lower if the pin is driven higher than V_{CCIO} by an external source.
- (14) Capacitance is sample-tested only.

Table 27. EAB Timing Macroparameters *Note (1), (6)*

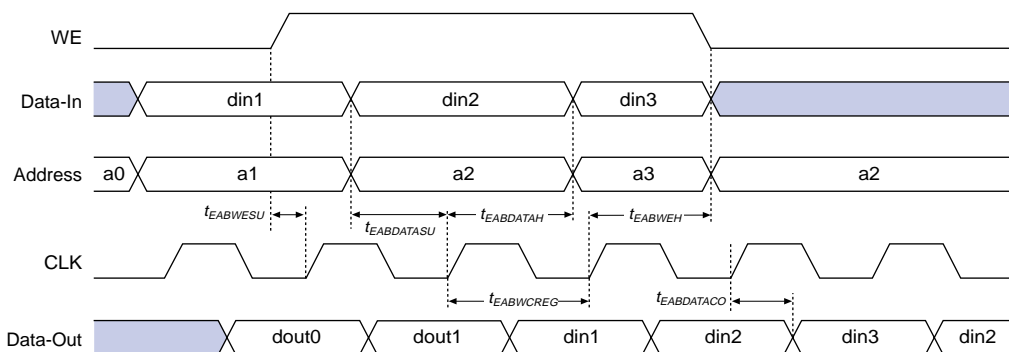
Symbol	Parameter	Conditions
t_{EABAA}	EAB address access delay	
$t_{EABRCCOMB}$	EAB asynchronous read cycle time	
$t_{EABRCREG}$	EAB synchronous read cycle time	
t_{EABWP}	EAB write pulse width	
$t_{EABWCCOMB}$	EAB asynchronous write cycle time	
$t_{EABWCREG}$	EAB synchronous write cycle time	
t_{EABDD}	EAB data-in to data-out valid delay	
$t_{EABDATACO}$	EAB clock-to-output delay when using output registers	
$t_{EABDATASU}$	EAB data/address setup time before clock when using input register	
$t_{EABDATAH}$	EAB data/address hold time after clock when using input register	
$t_{EABWESU}$	EAB \overline{WE} setup time before clock when using input register	
t_{EABWEH}	EAB \overline{WE} hold time after clock when using input register	
$t_{EABWDSU}$	EAB data setup time before falling edge of write pulse when not using input registers	
t_{EABWDH}	EAB data hold time after falling edge of write pulse when not using input registers	
$t_{EABWASU}$	EAB address setup time before rising edge of write pulse when not using input registers	
t_{EABWAH}	EAB address hold time after falling edge of write pulse when not using input registers	
t_{EABWO}	EAB write enable to data output valid delay	

Figure 30. EAB Synchronous Timing Waveforms

EAB Synchronous Read



EAB Synchronous Write (EAB Output Registers Used)



Tables 31 through 37 show EPF10K30E device internal and external timing parameters.

Table 31. EPF10K30E Device LE Timing Microparameters (Part 1 of 2) Note (1)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.7		0.8		1.1	ns
t_{CLUT}		0.5		0.6		0.8	ns
t_{RLUT}		0.6		0.7		1.0	ns
t_{PACKED}		0.3		0.4		0.5	ns
t_{EN}		0.6		0.8		1.0	ns
t_{CICO}		0.1		0.1		0.2	ns
t_{CGEN}		0.4		0.5		0.7	ns

Table 48. EPF10K100E Device EAB Internal Timing Macroparameters (Part 2 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABWCOMB}$	5.9		7.7		10.3		ns
$t_{EABWCREG}$	5.4		7.0		9.4		ns
t_{EABDD}		3.4		4.5		5.9	ns
$t_{EABDATACO}$		0.5		0.7		0.8	ns
$t_{EABDATASU}$	0.8		1.0		1.4		ns
$t_{EABDATAH}$	0.1		0.1		0.2		ns
$t_{EABWESU}$	1.1		1.4		1.9		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.0		1.3		1.7		ns
t_{EABWDH}	0.2		0.2		0.3		ns
$t_{EABWASU}$	4.1		5.2		6.8		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		3.4		4.5		5.9	ns

Table 49. EPF10K100E Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		3.1		3.6		4.4	ns
t_{DIN2LE}		0.3		0.4		0.5	ns
$t_{DIN2DATA}$		1.6		1.8		2.0	ns
$t_{DCLK2IOE}$		0.8		1.1		1.4	ns
$t_{DCLK2LE}$		0.3		0.4		0.5	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		1.5		2.5		3.4	ns
$t_{SAMECOLUMN}$		0.4		1.0		1.6	ns
$t_{DIFFROW}$		1.9		3.5		5.0	ns
$t_{TWOROWS}$		3.4		6.0		8.4	ns
$t_{LEPERIPH}$		4.3		5.4		6.5	ns
$t_{LABCARRY}$		0.5		0.7		0.9	ns
$t_{LABCASC}$		0.8		1.0		1.4	ns

Table 54. EPF10K130E Device EAB Internal Microparameters (Part 2 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DD}		1.5		2.0		2.6	ns
t_{EABOUT}		0.2		0.3		0.3	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	2.7		3.5		4.7		ns

Table 55. EPF10K130E Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		5.9		7.5		9.9	ns
$t_{EABRCOMB}$	5.9		7.5		9.9		ns
$t_{EABRCREG}$	5.1		6.4		8.5		ns
t_{EABWP}	2.7		3.5		4.7		ns
$t_{EABWCOMB}$	5.9		7.7		10.3		ns
$t_{EABWCREG}$	5.4		7.0		9.4		ns
t_{EABDD}		3.4		4.5		5.9	ns
$t_{EABDATACO}$		0.5		0.7		0.8	ns
$t_{EABDATASU}$	0.8		1.0		1.4		ns
$t_{EABDATAH}$	0.1		0.1		0.2		ns
$t_{EABWESU}$	1.1		1.4		1.9		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.0		1.3		1.7		ns
t_{EABWDH}	0.2		0.2		0.3		ns
$t_{EABWASU}$	4.1		5.1		6.8		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		3.4		4.5		5.9	ns

Table 76. EPF10K200S Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		3.9		6.4		8.4	ns
$t_{EABRCOMB}$	3.9		6.4		8.4		ns
$t_{EABRCREG}$	3.6		5.7		7.6		ns
t_{EABWP}	2.1		4.0		5.3		ns
$t_{EABWCOMB}$	4.8		8.1		10.7		ns
$t_{EABWCREG}$	5.4		8.0		10.6		ns
t_{EABDD}		3.8		5.1		6.7	ns
$t_{EABDATACO}$		0.8		1.0		1.3	ns
$t_{EABDATASU}$	1.1		1.6		2.1		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	0.7		1.1		1.5		ns
t_{EABWEH}	0.4		0.5		0.6		ns
$t_{EABWDSU}$	1.2		1.8		2.4		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	1.9		3.6		4.7		ns
t_{EABWAH}	0.8		0.5		0.7		ns
t_{EABWO}		3.1		4.4		5.8	ns

Table 77. EPF10K200S Device Interconnect Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		4.4		4.8		5.5	ns
t_{DIN2LE}		0.6		0.6		0.9	ns
$t_{DIN2DATA}$		1.8		2.1		2.8	ns
$t_{DCLK2IOE}$		1.7		2.0		2.8	ns
$t_{DCLK2LE}$		0.6		0.6		0.9	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		3.0		4.6		5.7	ns
$t_{SAMECOLUMN}$		3.5		4.9		6.4	ns
$t_{DIFFROW}$		6.5		9.5		12.1	ns
$t_{TROWROWS}$		9.5		14.1		17.8	ns
$t_{LEPERIPH}$		5.5		6.2		7.2	ns
$t_{LABCARRY}$		0.3		0.1		0.2	ns

Table 77. EPF10K200S Device Interconnect Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.5		1.0		1.4	ns

 Table 78. EPF10K200S External Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		9.0		12.0		16.0	ns
$t_{INSU}^{(2)}$	3.1		3.7		4.7		ns
$t_{INH}^{(2)}$	0.0		0.0		0.0		ns
$t_{OUTCO}^{(2)}$	2.0	3.7	2.0	4.4	2.0	6.3	ns
$t_{INSU}^{(3)}$	2.1		2.7		–		ns
$t_{INH}^{(3)}$	0.0		0.0		–		ns
$t_{OUTCO}^{(3)}$	0.5	2.7	0.5	3.4	–	–	ns
t_{PCISU}	3.0		4.2		–		ns
t_{PCIH}	0.0		0.0		–		ns
t_{PCICO}	2.0	6.0	2.0	8.9	–	–	ns

 Table 79. EPF10K200S External Bidirectional Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}^{(2)}$	2.3		3.4		4.4		ns
$t_{INHBIDIR}^{(2)}$	0.0		0.0		0.0		ns
$t_{INSUBIDIR}^{(3)}$	3.3		4.4		–		ns
$t_{INHBIDIR}^{(3)}$	0.0		0.0		–		ns
$t_{OUTCOBIDIR}^{(2)}$	2.0	3.7	2.0	4.4	2.0	6.3	ns
$t_{XZBIDIR}^{(2)}$		6.9		7.6		9.2	ns
$t_{ZXBIDIR}^{(2)}$		5.9		6.6		–	ns
$t_{OUTCOBIDIR}^{(3)}$	0.5	2.7	0.5	3.4	–	–	ns
$t_{XZBIDIR}^{(3)}$		6.9		7.6		9.2	ns
$t_{ZXBIDIR}^{(3)}$		5.9		6.6		–	ns

Notes to tables:

- (1) All timing parameters are described in Tables 24 through 30 in this data sheet.
- (2) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
- (3) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Power Consumption

The supply power (P) for FLEX 10KE devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = (I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC} + P_{IO}$$

The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value is calculated based on the amount of current that each LE typically consumes. The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in [Application Note 74 \(Evaluating Power for Altera Devices\)](#).

Compared to the rest of the device, the embedded array consumes a negligible amount of power. Therefore, the embedded array can be ignored when calculating supply current.

The $I_{CCACTIVE}$ value can be calculated with the following equation:

$$I_{CCACTIVE} = K \times f_{MAX} \times N \times \mathbf{togLC} \times \frac{\mu A}{MHz \times LE}$$

Where:

- f_{MAX} = Maximum operating frequency in MHz
- N = Total number of LEs used in the device
- \mathbf{togLC} = Average percent of LEs toggling at each clock (typically 12.5%)
- K = Constant

Table 80 provides the constant (K) values for FLEX 10KE devices.

<i>Table 80. FLEX 10KE K Constant Values</i>	
Device	K Value
EPF10K30E	4.5
EPF10K50E	4.8
EPF10K50S	4.5
EPF10K100E	4.5
EPF10K130E	4.6
EPF10K200E	4.8
EPF10K200S	4.6

This calculation provides an I_{CC} estimate based on typical conditions with no output load. The actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

To better reflect actual designs, the power model (and the constant K in the power calculation equations) for continuous interconnect FLEX devices assumes that LEs drive FastTrack Interconnect channels. In contrast, the power model of segmented FPGAs assumes that all LEs drive only one short interconnect segment. This assumption may lead to inaccurate results when compared to measured power consumption for actual designs in segmented FPGAs.

Figure 31 shows the relationship between the current and operating frequency of FLEX 10KE devices.

Figure 31. FLEX 10KE $I_{CCACTIVE}$ vs. Operating Frequency (Part 1 of 2)

