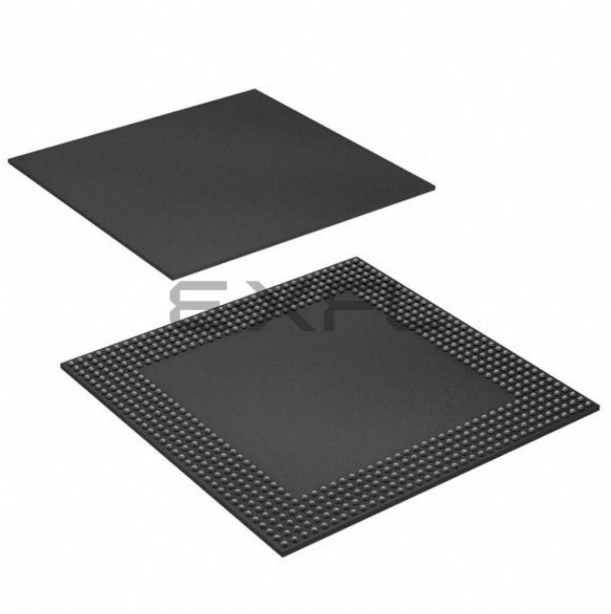
Intel - EPF10K200SBC600-3B Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	1248
Number of Logic Elements/Cells	9984
Total RAM Bits	98304
Number of I/O	470
Number of Gates	513000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	600-BGA
Supplier Device Package	600-BGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k200sbc600-3b

- Software design support and automatic place-and-route provided by Altera's development systems for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800
- Flexible package options
  - Available in a variety of packages with 144 to 672 pins, including the innovative FineLine BGA™ packages (see Tables 3 and 4)
  - SameFrame™ pin-out compatibility between FLEX 10KA and FLEX 10KE devices across a range of device densities and pin counts
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), DesignWare components, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, VeriBest, and Viewlogic

Table 3. FLEX 10KE Package Options & I/O Pin Count *Notes (1), (2)*

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP RQFP	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA	599-Pin PGA	600-Pin BGA	672-Pin FineLine BGA
EPF10K30E	102	147		176		220			220 *(3)*
EPF10K50E	102	147	189	191		254			254 *(3)*
EPF10K50S	102	147	189	191	220	254			254 *(3)*
EPF10K100E		147	189	191	274	338			338 *(3)*
EPF10K130E			186		274	369		424	413
EPF10K200E							470	470	470
EPF10K200S			182		274	369	470	470	470

Notes:

(1) FLEX 10KE device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), pin-grid array (PGA), and ball-grid array (BGA) packages.

(2) Devices in the same package are pin-compatible, although some devices have more I/O pins than others. When planning device migration, use the I/O pins that are common to all devices.

(3) This option is supported with a 484-pin FineLine BGA package. By using SameFrame pin migration, all FineLine BGA packages are pin-compatible. For example, a board can be designed to support 256-pin, 484-pin, and 672-pin FineLine BGA packages. The Altera software automatically avoids conflicting pins when future migration is set.

Table 4. FLEX 10KE Package Sizes

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP RQFP	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA	599-Pin PGA	600-Pin BGA	672-Pin FineLine BGA
Pitch (mm)	0.50	0.50	0.50	1.0	1.27	1.0	–	1.27	1.0
Area (mm^2)	484	936	1,197	289	1,225	529	3,904	2,025	729
Length × width (mm × mm)	22 × 22	30.6 × 30.6	34.6 × 34.6	17 × 17	35 × 35	23 × 23	62.5 × 62.5	45 × 45	27 × 27

General Description

Altera FLEX 10KE devices are enhanced versions of FLEX 10K devices. Based on reconfigurable CMOS SRAM elements, the FLEX architecture incorporates all features necessary to implement common gate array megafunctions. With up to 200,000 typical gates, FLEX 10KE devices provide the density, speed, and features to integrate entire systems, including multiple 32-bit buses, into a single device.

The ability to reconfigure FLEX 10KE devices enables 100% testing prior to shipment and allows the designer to focus on simulation and design verification. FLEX 10KE reconfigurability eliminates inventory management for gate array designs and generation of test vectors for fault coverage.

Table 5 shows FLEX 10KE performance for some common designs. All performance values were obtained with Synopsys DesignWare or LPM functions. Special design techniques are not required to implement the applications; the designer simply infers or instantiates a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

EABs provide flexible options for driving and controlling clock signals. Different clocks and clock enables can be used for reading and writing to the EAB. Registers can be independently inserted on the data input, EAB output, write address, write enable signals, read address, and read enable signals. The global signals and the EAB local interconnect can drive write enable, read enable, and clock enable signals. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control write enable, read enable, clear, clock, and clock enable signals.

An EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs (see Figures 2 and 4). The column interconnect, which is adjacent to the EAB, has twice as many channels as other columns in the device.

Logic Array Block

An LAB consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure to the FLEX 10KE architecture, facilitating efficient routing with optimum device utilization and high performance (see Figure 7).

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks, the other two can be used for clear / preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I / O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I / O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LE in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated from LE outputs.

Logic Element

The LE, the smallest unit of logic in the FLEX 10KE architecture, has a compact size that provides efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous clock enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect routing structure (see Figure 8).

Figure 8. FLEX 10KE Logic Element

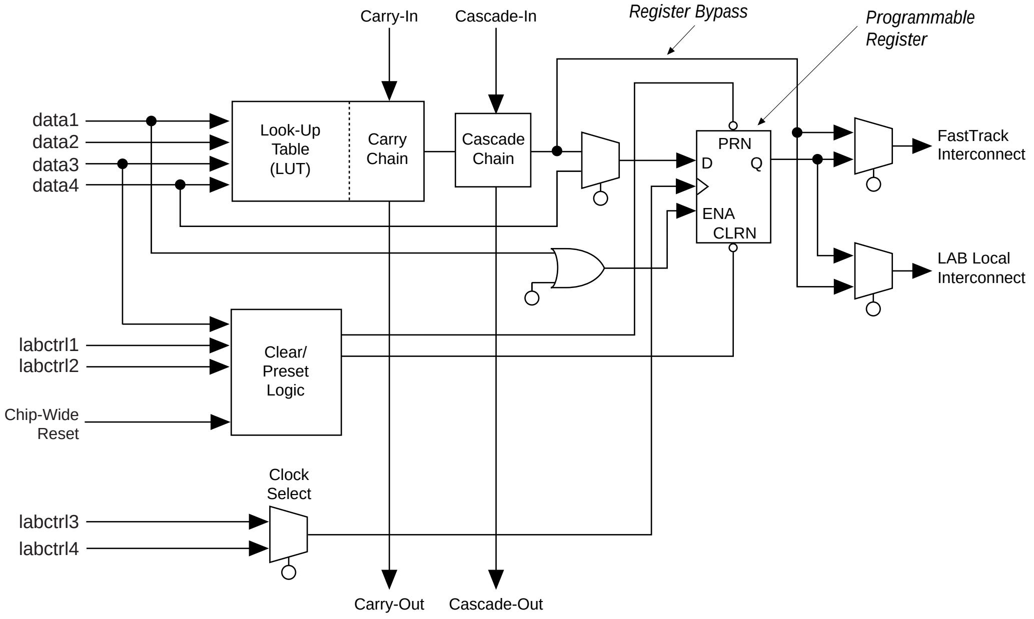
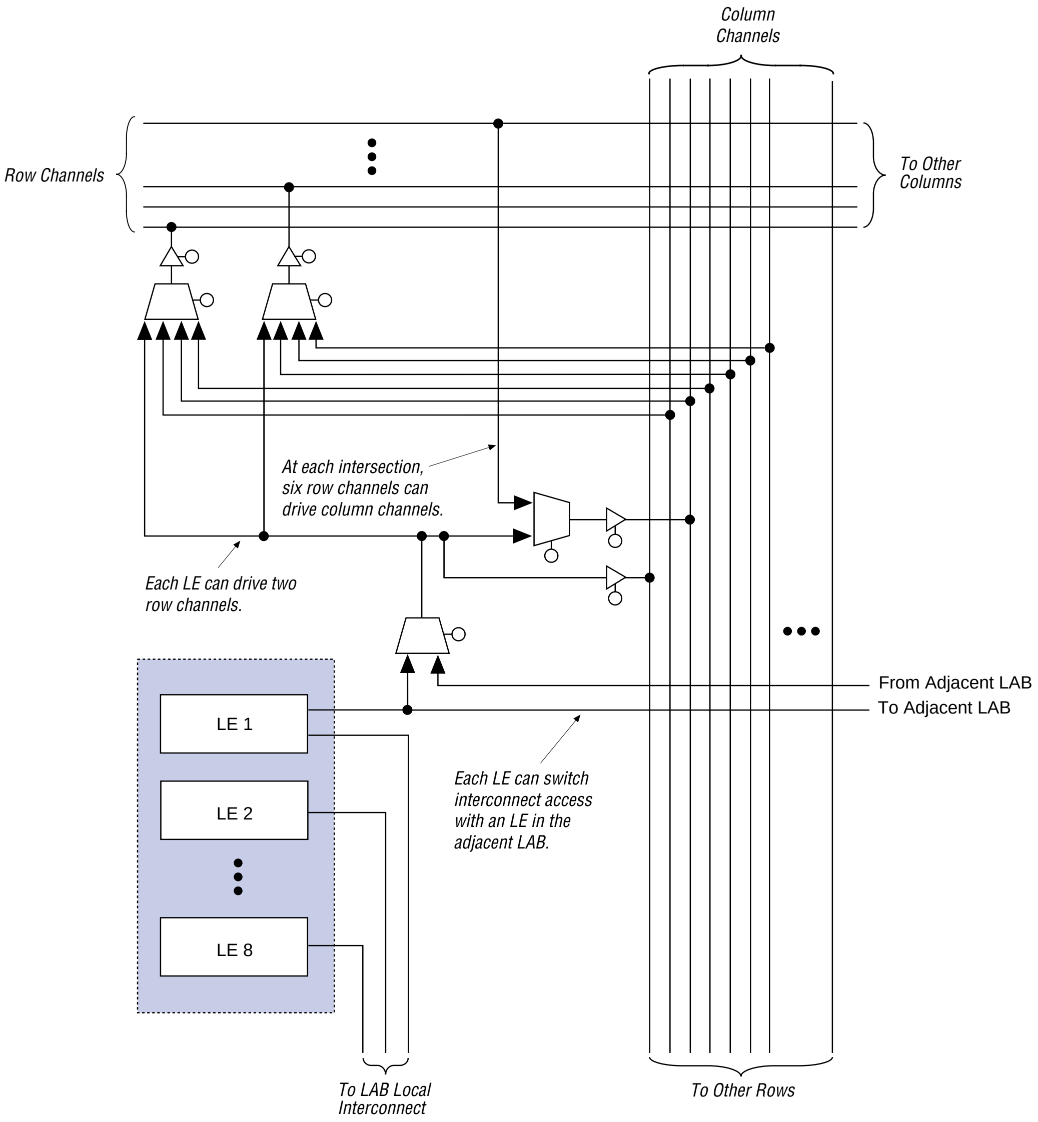


Figure 13. FLEX 10KE LAB Connections to Row & Column Interconnect



Tables 12 and 13 summarize the ClockLock and ClockBoost parameters for -1 and -2 speed-grade devices, respectively.

Table 12. ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)		25		180	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)		16		90	MHz
f_{CLKDEV}	Input deviation from user specification in the MAX+PLUS II software *(1)*				25,000 *(2)*	PPM
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)				100	ps
t_{LOCK}	Time required for ClockLock or ClockBoost to acquire lock *(3)*				10	µs
t_{JITTER}	Jitter on ClockLock or ClockBoost-generated clock *(4)*	$t_{INCLKSTB} < 100$			250	ps
		$t_{INCLKSTB} < 50$			200 *(4)*	ps
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		40	50	60	%

Table 17. 32-Bit IDCODE for FLEX 10KE Devices *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) *(2)*
EPF10K30E	`0001`	`0001 0000 0011 0000`	`00001101110`	`1`
EPF10K50E EPF10K50S	`0001`	`0001 0000 0101 0000`	`00001101110`	`1`
EPF10K100E	`0010`	`0000 0001 0000 0000`	`00001101110`	`1`
EPF10K130E	`0001`	`0000 0001 0011 0000`	`00001101110`	`1`
EPF10K200E EPF10K200S	`0001`	`0000 0010 0000 0000`	`00001101110`	`1`

Notes:

(1) The most significant bit (MSB) is on the left.

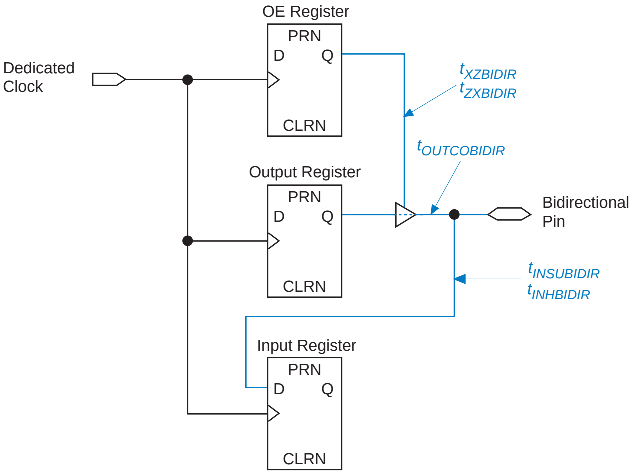
(2) The least significant bit (LSB) for all JTAG IDCODEs is `1`.

FLEX 10KE devices include weak pull-up resistors on the JTAG pins.

For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Jam Programming & Test Language Specification*

Figure 28. Synchronous Bidirectional Pin External Timing Model



Tables 24 through 28 describe the FLEX 10KE device internal timing parameters. Tables 29 through 30 describe the FLEX 10KE external timing parameters and their symbols.

Table 24. LE Timing Microparameters (Part 1 of 2) Note (1)

Symbol	Parameter	Condition
t_{LUT}	LUT delay for data-in	
t_{CLUT}	LUT delay for carry-in	
t_{RLUT}	LUT delay for LE register feedback	
t_{PACKED}	Data-in to packed register delay	
t_{EN}	LE register enable delay	
t_{CICO}	Carry-in to carry-out delay	
t_{CGEN}	Data-in to carry-out delay	
t_{CGENR}	LE register feedback to carry-out delay	
t_{CASC}	Cascade-in to cascade-out delay	
t_C	LE register control signal delay	
t_{CO}	LE register clock-to-output delay	
t_{COMB}	Combinatorial delay	
t_{SU}	LE register setup time for data and enable signals before clock; LE register recovery time after asynchronous clear, preset, or load	
t_H	LE register hold time for data and enable signals after clock	
t_{PRE}	LE register preset delay	

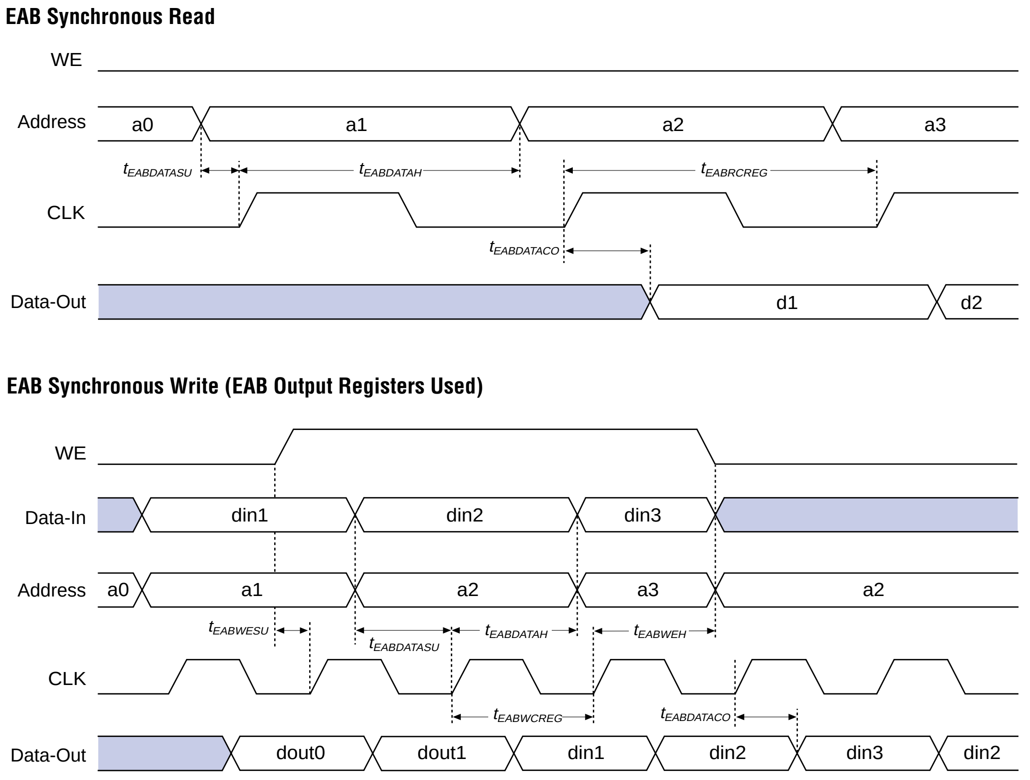
Table 30. External Bidirectional Timing Parameters *Note (9)*

Symbol	Parameter	Conditions
$t_{INSUBIDIR}$	Setup time for bi-directional pins with global clock at same-row or same-column LE register	
$t_{INHBIDIR}$	Hold time for bidirectional pins with global clock at same-row or same-column LE register	
t_{INH}	Hold time with global clock at IOE register	
$t_{OUTCOBIDIR}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	C1 = 35 pF
$t_{XZBIDIR}$	Synchronous IOE output buffer disable delay	C1 = 35 pF
$t_{ZXBIDIR}$	Synchronous IOE output buffer enable delay, slow slew rate= off	C1 = 35 pF

Notes to tables:

(1) Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.
(2) Operating conditions: VCCIO = 3.3 V ±10% for commercial or industrial use.
(3) Operating conditions: VCCIO = 2.5 V ±5% for commercial or industrial use in EPF10K30E, EPF10K50S, EPF10K100E, EPF10K130E, and EPF10K200S devices.
(4) Operating conditions: VCCIO = 3.3 V.
(5) Because the RAM in the EAB is self-timed, this parameter can be ignored when the `WE` signal is registered.
(6) EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.
(7) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.
(8) Contact Altera Applications for test circuit specifications and test conditions.
(9) This timing parameter is sample-tested only.
(10) This parameter is measured with the measurement and test conditions, including load, specified in the PCI Local Bus Specification, revision 2.2.

Figure 30. EAB Synchronous Timing Waveforms



Tables 31 through 37 show EPF10K30E device internal and external timing parameters.

Table 31. EPF10K30E Device LE Timing Microparameters (Part 1 of 2) Note (1)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.7		0.8		1.1	ns
t_{CLUT}		0.5		0.6		0.8	ns
t_{RLUT}		0.6		0.7		1.0	ns
t_{PACKED}		0.3		0.4		0.5	ns
t_{EN}		0.6		0.8		1.0	ns
t_{CICO}		0.1		0.1		0.2	ns
t_{CGEN}		0.4		0.5		0.7	ns

Table 35. EPF10K30E Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		1.8		2.4		2.9	ns
t_{DIN2LE}		1.5		1.8		2.4	ns
$t_{DIN2DATA}$		1.5		1.8		2.2	ns
$t_{DCLK2IOE}$		2.2		2.6		3.0	ns
$t_{DCLK2LE}$		1.5		1.8		2.4	ns
$t_{SAMELAB}$		0.1		0.2		0.3	ns
$t_{SAMEROW}$		2.0		2.4		2.7	ns
$t_{SAMECOLUMN}$		0.7		1.0		0.8	ns
$t_{DIFFROW}$		2.7		3.4		3.5	ns
$t_{TWOROWS}$		4.7		5.8		6.2	ns
$t_{LEPERIPH}$		2.7		3.4		3.8	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.8		0.8		1.1	ns

Table 36. EPF10K30E External Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		8.0		9.5		12.5	ns
t_{INSU} *(3)*	2.1		2.5		3.9		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	4.9	2.0	5.9	2.0	7.6	ns
t_{INSU} *(4)*	1.1		1.5		–		ns
t_{INH} *(4)*	0.0		0.0		–		ns
t_{OUTCO} *(4)*	0.5	3.9	0.5	4.9	–	–	ns
t_{PCISU}	3.0		4.2		–		ns
t_{PCIH}	0.0		0.0		–		ns
t_{PCICO}	2.0	6.0	2.0	7.5	–	–	ns

Table 38. EPF10K50E Device LE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{H}	0.9		1.0		1.4		ns
t_{PRE}		0.5		0.6		0.8	ns
t_{CLR}		0.5		0.6		0.8	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns

Table 39. EPF10K50E Device IOE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{IOD}		2.2		2.4		3.3	ns
t_{IOC}		0.3		0.3		0.5	ns
t_{IOCO}		1.0		1.0		1.4	ns
t_{IOCOMB}		0.0		0.0		0.2	ns
t_{IOSU}	1.0		1.2		1.7		ns
t_{IOH}	0.3		0.3		0.5		ns
t_{IOCLR}		0.9		1.0		1.4	ns
t_{OD1}		0.8		0.9		1.2	ns
t_{OD2}		0.3		0.4		0.7	ns
t_{OD3}		3.0		3.5		3.5	ns
t_{XZ}		1.4		1.7		2.3	ns
t_{ZX1}		1.4		1.7		2.3	ns
t_{ZX2}		0.9		1.2		1.8	ns
t_{ZX3}		3.6		4.3		4.6	ns
t_{INREG}		4.9		5.8		7.8	ns
t_{IOFD}		2.8		3.3		4.5	ns
t_{INCOMB}		2.8		3.3		4.5	ns

Table 40. EPF10K50E Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.7		2.0		2.7	ns
$t_{EABDATA1}$		0.6		0.7		0.9	ns
t_{EABWE1}		1.1		1.3		1.8	ns
t_{EABWE2}		0.4		0.4		0.6	ns
t_{EABRE1}		0.8		0.9		1.2	ns
t_{EABRE2}		0.4		0.4		0.6	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.3		0.3		0.5	ns
$t_{EABBYPASS}$		0.5		0.6		0.8	ns
t_{EABSU}	0.9		1.0		1.4		ns
t_{EABH}	0.4		0.4		0.6		ns
t_{EABCLR}	0.3		0.3		0.5		ns
t_{AA}		3.2		3.8		5.1	ns
t_{WP}	2.5		2.9		3.9		ns
t_{RP}	0.9		1.1		1.5		ns
t_{WDSU}	0.9		1.0		1.4		ns
t_{WDH}	0.1		0.1		0.2		ns
t_{WASU}	1.7		2.0		2.7		ns
t_{WAH}	1.8		2.1		2.9		ns
t_{RASU}	3.1		3.7		5.0		ns
t_{RAH}	0.2		0.2		0.3		ns
t_{WO}		2.5		2.9		3.9	ns
t_{DD}		2.5		2.9		3.9	ns
t_{EABOUT}		0.5		0.6		0.8	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	2.5		2.9		3.9		ns

Table 58. EPF10K130E External Bidirectional Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (3)	2.2		2.4		3.2		ns
$t_{INHBIDIR}$ (3)	0.0		0.0		0.0		ns
$t_{INSUBIDIR}$ (4)	2.8		3.0		–		ns
$t_{INHBIDIR}$ (4)	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ (3)	2.0	5.0	2.0	7.0	2.0	9.2	ns
$t_{XZBIDIR}$ (3)		5.6		8.1		10.8	ns
$t_{ZXBIDIR}$ (3)		5.6		8.1		10.8	ns
$t_{OUTCOBIDIR}$ (4)	0.5	4.0	0.5	6.0	–	–	ns
$t_{XZBIDIR}$ (4)		4.6		7.1		–	ns
$t_{ZXBIDIR}$ (4)		4.6		7.1		–	ns

Notes to tables:

(1) All timing parameters are described in Tables 24 through 30 in this data sheet.
(2) These parameters are specified by characterization.
(3) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 59 through 65 show EPF10K200E device internal and external timing parameters.

Table 59. EPF10K200E Device LE Timing Microparameters *(Part 1 of 2)* *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.7		0.8		1.2	ns
t_{CLUT}		0.4		0.5		0.6	ns
t_{RLUT}		0.6		0.7		0.9	ns
t_{PACKED}		0.3		0.5		0.7	ns
t_{EN}		0.4		0.5		0.6	ns
t_{CICO}		0.2		0.2		0.3	ns
t_{CGEN}		0.4		0.4		0.6	ns
t_{CGENR}		0.2		0.2		0.3	ns
t_{CASC}		0.7		0.8		1.2	ns
t_C		0.5		0.6		0.8	ns
t_{CO}		0.5		0.6		0.8	ns
t_{COMB}		0.4		0.6		0.8	ns
t_{SU}	0.4		0.6		0.7		ns

Table 59. EPF10K200E Device LE Timing Microparameters *(Part 2 of 2)* *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{H}	0.9		1.1		1.5		ns
t_{PRE}		0.5		0.6		0.8	ns
t_{CLR}		0.5		0.6		0.8	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns

Table 60. EPF10K200E Device IOE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IOD}		1.6		1.9		2.6	ns
t_{IOC}		0.3		0.3		0.5	ns
t_{IOCO}		1.6		1.9		2.6	ns
t_{IOCOMB}		0.5		0.6		0.8	ns
t_{IOSU}	0.8		0.9		1.2		ns
t_{IOH}	0.7		0.8		1.1		ns
t_{IOCLR}		0.2		0.2		0.3	ns
t_{OD1}		0.6		0.7		0.9	ns
t_{OD2}		0.1		0.2		0.7	ns
t_{OD3}		2.5		3.0		3.9	ns
t_{XZ}		4.4		5.3		7.1	ns
t_{ZX1}		4.4		5.3		7.1	ns
t_{ZX2}		3.9		4.8		6.9	ns
t_{ZX3}		6.3		7.6		10.1	ns
t_{INREG}		4.8		5.7		7.7	ns
t_{IOFD}		1.5		1.8		2.4	ns
t_{INCOMB}		1.5		1.8		2.4	ns

Table 61. EPF10K200E Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		2.0		2.4		3.2	ns
$t_{EABDATA1}$		0.4		0.5		0.6	ns
t_{EABWE1}		1.4		1.7		2.3	ns
t_{EABWE2}		0.0		0.0		0.0	ns
t_{EABRE1}		0		0		0	ns
t_{EABRE2}		0.4		0.5		0.6	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.8		0.9		1.2	ns
$t_{EABBYPASS}$		0.0		0.1		0.1	ns
t_{EABSU}	0.9		1.1		1.5		ns
t_{EABH}	0.4		0.5		0.6		ns
t_{EABCLR}	0.8		0.9		1.2		ns
t_{AA}		3.1		3.7		4.9	ns
t_{WP}	3.3		4.0		5.3		ns
t_{RP}	0.9		1.1		1.5		ns
t_{WDSU}	0.9		1.1		1.5		ns
t_{WDH}	0.1		0.1		0.1		ns
t_{WASU}	1.3		1.6		2.1		ns
t_{WAH}	2.1		2.5		3.3		ns
t_{RASU}	2.2		2.6		3.5		ns
t_{RAH}	0.1		0.1		0.2		ns
t_{WO}		2.0		2.4		3.2	ns
t_{DD}		2.0		2.4		3.2	ns
t_{EABOUT}		0.0		0.1		0.1	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	3.3		4.0		5.3		ns

Table 62. EPF10K200E Device EAB Internal Timing Macroparameters (Part 1 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		5.1		6.4		8.4	ns
$t_{EABRCOMB}$	5.1		6.4		8.4		ns
$t_{EABRCREG}$	4.8		5.7		7.6		ns
t_{EABWP}	3.3		4.0		5.3		ns

Table 64. EPF10K200E External Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		10.0		12.0		16.0	ns
t_{INSU}	2.8		3.4		4.4		ns
t_{INH}	0.0		0.0		0.0		ns
t_{OUTCO}	2.0	4.5	2.0	5.3	2.0	7.8	ns
t_{PCISU}	3.0		6.2		-		ns
t_{PCIH}	0.0		0.0		-		ns
t_{PCICO}	2.0	6.0	2.0	8.9	-	-	ns

Table 65. EPF10K200E External Bidirectional Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	3.0		4.0		5.5		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	4.5	2.0	5.3	2.0	7.8	ns
$t_{XZBIDIR}$		8.1		9.5		13.0	ns
$t_{ZXBIDIR}$		8.1		9.5		13.0	ns

Notes to tables:

(1) All timing parameters are described in Tables 24 through 30 in this data sheet.

(2) These parameters are specified by characterization.

Tables 66 through 79 show EPF10K50S and EPF10K200S device external timing parameters.

Table 66. EPF10K50S Device LE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.6		0.8		1.1	ns
t_{CLUT}		0.5		0.6		0.8	ns
t_{RLUT}		0.6		0.7		0.9	ns
t_{PACKED}		0.2		0.3		0.4	ns
t_{EN}		0.6		0.7		0.9	ns
t_{CICO}		0.1		0.1		0.1	ns
t_{CGEN}		0.4		0.5		0.6	ns

Table 74. EPF10K200S Device IOE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ZX2}		4.5		4.8		6.6	ns
t_{ZX3}		6.6		7.6		10.1	ns
t_{INREG}		3.7		5.7		7.7	ns
t_{IOFD}		1.8		3.4		4.0	ns
t_{INCOMB}		1.8		3.4		4.0	ns

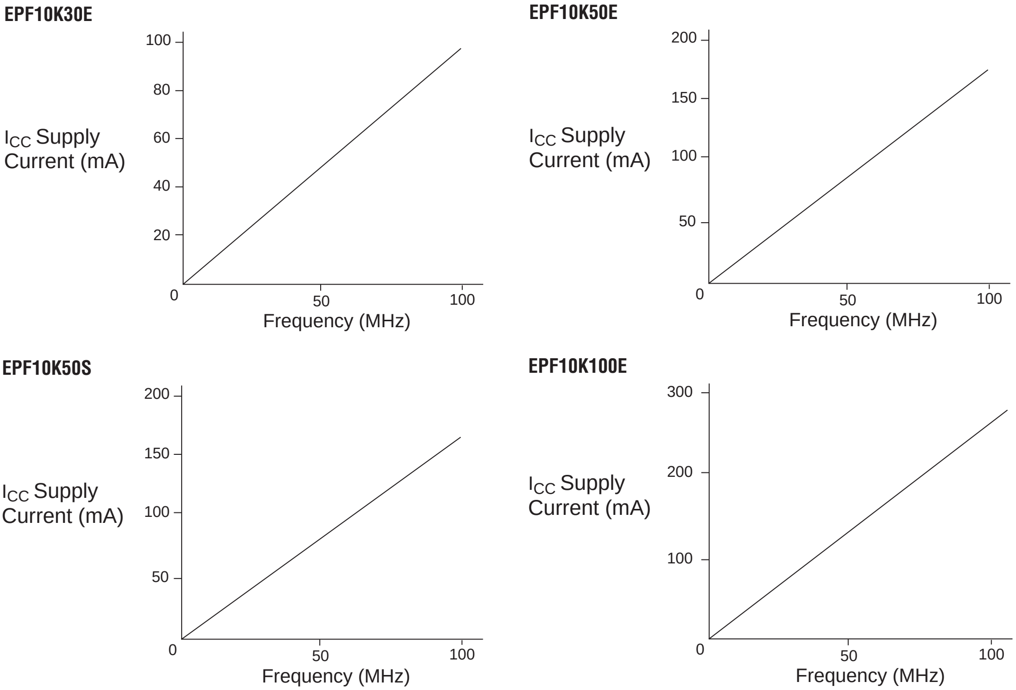
Table 75. EPF10K200S Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.8		2.4		3.2	ns
$t_{EABDATA1}$		0.4		0.5		0.6	ns
t_{EABWE1}		1.1		1.7		2.3	ns
t_{EABWE2}		0.0		0.0		0.0	ns
t_{EABRE1}		0		0		0	ns
t_{EABRE2}		0.4		0.5		0.6	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.8		0.9		1.2	ns
$t_{EABBYPASS}$		0.0		0.1		0.1	ns
t_{EABSU}	0.7		1.1		1.5		ns
t_{EABH}	0.4		0.5		0.6		ns
t_{EABCLR}	0.8		0.9		1.2		ns
t_{AA}		2.1		3.7		4.9	ns
t_{WP}	2.1		4.0		5.3		ns
t_{RP}	1.1		1.1		1.5		ns
t_{WDSU}	0.5		1.1		1.5		ns
t_{WDH}	0.1		0.1		0.1		ns
t_{WASU}	1.1		1.6		2.1		ns
t_{WAH}	1.6		2.5		3.3		ns
t_{RASU}	1.6		2.6		3.5		ns
t_{RAH}	0.1		0.1		0.2		ns
t_{WO}		2.0		2.4		3.2	ns
t_{DD}		2.0		2.4		3.2	ns
t_{EABOUT}		0.0		0.1		0.1	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	2.1		2.8		3.8		ns

To better reflect actual designs, the power model (and the constant K in the power calculation equations) for continuous interconnect FLEX devices assumes that LEs drive FastTrack Interconnect channels. In contrast, the power model of segmented FPGAs assumes that all LEs drive only one short interconnect segment. This assumption may lead to inaccurate results when compared to measured power consumption for actual designs in segmented FPGAs.

Figure 31 shows the relationship between the current and operating frequency of FLEX 10KE devices.

Figure 31. FLEX 10KE $I_{CCACTIVE}$ vs. Operating Frequency (Part 1 of 2)



EPF10K30E

EPF10K50E

EPF10K50S

EPF10K100E

Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the Altera Digital Library for pin-out information.

Revision History

The information contained in the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.5 supersedes information published in previous versions.

Version 2.5

The following changes were made to the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.5:

- *Note (1)* added to Figure 23.
- Text added to "I/O Element" section on page 34.
- Updated Table 22.

Version 2.4

The following changes were made to the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.4: updated text on page 34 and page 63.