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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	1248
Number of Logic Elements/Cells	9984
Total RAM Bits	98304
Number of I/O	470
Number of Gates	513000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	672-BBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epf10k200sbc672-2x">https://www.e-xfl.com/product-detail/intel/epf10k200sbc672-2x</a>

Table 2. FLEX 10KE Device Features

Feature	EPF10K100E (2)	EPF10K130E	EPF10K200E EPF10K200S
Typical gates (1)	100,000	130,000	200,000
Maximum system gates	257,000	342,000	513,000
Logic elements (LEs)	4,992	6,656	9,984
EABs	12	16	24
Total RAM bits	49,152	65,536	98,304
Maximum user I/O pins	338	413	470

**Note to tables:**

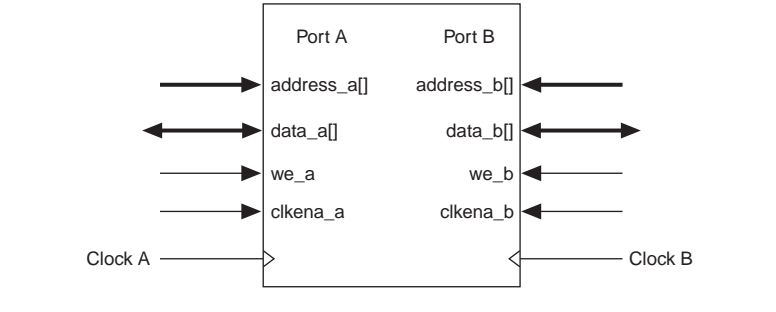
- (1) The embedded IEEE Std. 1149.1 JTAG circuitry adds up to 31,250 gates in addition to the listed typical or maximum system gates.
- (2) New EPF10K100B designs should use EPF10K100E devices.

## ...and More Features

- Fabricated on an advanced process and operate with a 2.5-V internal supply voltage
- In-circuit reconfigurability (ICR) via external configuration devices, intelligent controller, or JTAG port
- ClockLock™ and ClockBoost™ options for reduced clock delay/skew and clock multiplication
- Built-in low-skew clock distribution trees
- 100% functional testing of all devices; test vectors or scan chains are not required
- Pull-up on I/O pins before and during configuration
- Flexible interconnect
  - FastTrack® Interconnect continuous routing structure for fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Tri-state emulation that implements internal tri-state buses
  - Up to six global clock signals and four global clear signals
- Powerful I/O pins
  - Individual tri-state output enable control for each pin
  - Open-drain option on each I/O pin
  - Programmable output slew-rate control to reduce switching noise
  - Clamp to V<sub>CCIO</sub> user-selectable on a pin-by-pin basis
  - Supports hot-socketing

The EAB can also use Altera megafunctions to implement dual-port RAM applications where both ports can read or write, as shown in [Figure 3](#).

Figure 3. FLEX 10KE EAB in Dual-Port RAM Mode



The FLEX 10KE EAB can be used in a single-port mode, which is useful for backward-compatibility with FLEX 10K designs (see [Figure 4](#)).



EABs provide flexible options for driving and controlling clock signals. Different clocks and clock enables can be used for reading and writing to the EAB. Registers can be independently inserted on the data input, EAB output, write address, write enable signals, read address, and read enable signals. The global signals and the EAB local interconnect can drive write enable, read enable, and clock enable signals. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control write enable, read enable, clear, clock, and clock enable signals.

An EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs (see [Figures 2 and 4](#)). The column interconnect, which is adjacent to the EAB, has twice as many channels as other columns in the device.

### Logic Array Block

An LAB consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure to the FLEX 10KE architecture, facilitating efficient routing with optimum device utilization and high performance (see [Figure 7](#)).

### Clearable Counter Mode

The clearable counter mode is similar to the up/down counter mode, but supports a synchronous clear instead of the up/down control. The clear function is substituted for the cascade-in signal in the up/down counter mode. Use 2 three-input LUTs: one generates the counter data, and the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer. The output of this multiplexer is ANDed with a synchronous clear signal.

### *Internal Tri-State Emulation*

Internal tri-state emulation provides internal tri-states without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable (OE) signals select which signal drives the bus. However, if multiple OE signals are active, contending signals can be driven onto the bus. Conversely, if no OE signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The Altera software automatically implements tri-state bus functionality with a multiplexer.

### *Clear & Preset Logic Control*

Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. The clear and preset control structure of the LE asynchronously loads signals into a register. Either LABCTRL1 or LABCTRL2 can control the asynchronous clear. Alternatively, the register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

During compilation, the Altera Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six modes chosen during design entry:

- Asynchronous clear
- Asynchronous preset
- Asynchronous clear and preset
- Asynchronous load with clear
- Asynchronous load with preset
- Asynchronous load without clear or preset

## FastTrack Interconnect Routing Structure

In the FLEX 10KE architecture, connections between LEs, EABs, and device I/O pins are provided by the FastTrack Interconnect routing structure, which is a series of continuous horizontal and vertical routing channels that traverses the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect routing structure consists of row and column interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect. The row interconnect can drive I/O pins and feed other LABs in the row. The column interconnect routes signals between rows and can drive I/O pins.

Row channels drive into the LAB or EAB local interconnect. The row signal is buffered at every LAB or EAB to reduce the effect of fan-out on delay. A row channel can be driven by an LE or by one of three column channels. These four signals feed dual 4-to-1 multiplexers that connect to two specific row channels. These multiplexers, which are connected to each LE, allow column channels to drive row channels even when all eight LEs in a LAB drive the row interconnect.

Each column of LABs or EABs is served by a dedicated column interconnect. The column interconnect that serves the EABs has twice as many channels as other column interconnects. The column interconnect can then drive I/O pins or another row's interconnect to route the signals to other LABs or EABs in the device. A signal from the column interconnect, which can be either the output of a LE or an input from an I/O pin, must be routed to the row interconnect before it can enter a LAB or EAB. Each row channel that is driven by an IOE or EAB can drive one specific column channel.

Access to row and column channels can be switched between LEs in adjacent pairs of LABs. For example, a LE in one LAB can drive the row and column channels normally driven by a particular LE in the adjacent LAB in the same row, and vice versa. This flexibility enables routing resources to be used more efficiently (see [Figure 13](#)).

When dedicated inputs drive non-inverted and inverted peripheral clears, clock enables, and output enables, two signals on the peripheral control bus will be used.

Tables 8 and 9 list the sources for each peripheral control signal, and show how the output enable, clock enable, clock, and clear signals share 12 peripheral control signals. The tables also show the rows that can drive global signals.

*Table 8. Peripheral Bus Sources for EPF10K30E, EPF10K50E & EPF10K50S Devices*

Peripheral Control Signal	EPF10K30E	EPF10K50E EPF10K50S
OE0	Row A	Row A
OE1	Row B	Row B
OE2	Row C	Row D
OE3	Row D	Row F
OE4	Row E	Row H
OE5	Row F	Row J
CLKENA0/CLK0/GLOBAL0	Row A	Row A
CLKENA1/OE6/GLOBAL1	Row B	Row C
CLKENA2/CLR0	Row C	Row E
CLKENA3/OE7/GLOBAL2	Row D	Row G
CLKENA4/CLR1	Row E	Row I
CLKENA5/CLK1/GLOBAL3	Row F	Row J

## ClockLock & ClockBoost Features

To support high-speed designs, FLEX 10KE devices offer optional ClockLock and ClockBoost circuitry containing a phase-locked loop (PLL) used to increase design speed and reduce resource usage. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by resource sharing within the device. The ClockBoost feature allows the designer to distribute a low-speed clock and multiply that clock on-device. Combined, the ClockLock and ClockBoost features provide significant improvements in system performance and bandwidth.

All FLEX 10KE devices, except EPF10K50E and EPF10K200E devices, support ClockLock and ClockBoost circuitry. EPF10K50S and EPF10K200S devices support this circuitry. Devices that support ClockLock and ClockBoost circuitry are distinguished with an "X" suffix in the ordering code; for instance, the EPF10K200SFC672-1X device supports this circuit.

The ClockLock and ClockBoost features in FLEX 10KE devices are enabled through the Altera software. External devices are not required to use these features. The output of the ClockLock and ClockBoost circuits is not available at any of the device pins.

The ClockLock and ClockBoost circuitry locks onto the rising edge of the incoming clock. The circuit output can drive the clock inputs of registers only; the generated clock cannot be gated or inverted.

The dedicated clock pin (`GCLK1`) supplies the clock to the ClockLock and ClockBoost circuitry. When the dedicated clock pin is driving the ClockLock or ClockBoost circuitry, it cannot drive elsewhere in the device.

For designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to the `GCLK1` pin. In the Altera software, the `GCLK1` pin can feed both the ClockLock and ClockBoost circuitry in the FLEX 10KE device. However, when both circuits are used, the other clock pin cannot be used.

Tables 12 and 13 summarize the ClockLock and ClockBoost parameters for -1 and -2 speed-grade devices, respectively.

**Table 12. ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_R$	Input rise time				5	ns
$t_F$	Input fall time				5	ns
$t_{INDUTY}$	Input duty cycle		40		60	%
$f_{CLK1}$	Input clock frequency (ClockBoost clock multiplication factor equals 1)		25		180	MHz
$f_{CLK2}$	Input clock frequency (ClockBoost clock multiplication factor equals 2)		16		90	MHz
$f_{CLKDEV}$	Input deviation from user specification in the MAX+PLUS II software (1)				25,000 (2)	PPM
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)				100	ps
$t_{LOCK}$	Time required for ClockLock or ClockBoost to acquire lock (3)				10	μs
$t_{JITTER}$	Jitter on ClockLock or ClockBoost-generated clock (4)	$t_{INCLKSTB} < 100$			250	ps
		$t_{INCLKSTB} < 50$			200 (4)	ps
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		40	50	60	%

The  $V_{CCINT}$  pins must always be connected to a 2.5-V power supply. With a 2.5-V  $V_{CCINT}$  level, input voltages are compatible with 2.5-V, 3.3-V, and 5.0-V inputs. The  $V_{CCIO}$  pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When the  $V_{CCIO}$  pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the  $V_{CCIO}$  pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with  $V_{CCIO}$  levels higher than 3.0 V achieve a faster timing delay of  $t_{OD2}$  instead of  $t_{OD1}$ .

Table 14 summarizes FLEX 10KE MultiVolt I/O support.

Table 14. FLEX 10KE MultiVolt I/O Support						
$V_{CCIO}$ (V)	Input Signal (V)			Output Signal (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓ (1)	✓ (1)	✓		
3.3	✓	✓	✓ (1)	✓ (2)	✓	✓

**Notes:**

- (1) The PCI clamping diode must be disabled to drive an input with voltages higher than  $V_{CCIO}$ .
- (2) When  $V_{CCIO} = 3.3$  V, a FLEX 10KE device can drive a 2.5-V device that has 3.3-V tolerant inputs.

Open-drain output pins on FLEX 10KE devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a  $V_{IH}$  of 3.5 V. When the open-drain pin is active, it will drive low. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The  $I_{OL}$  current specification should be considered when selecting a pull-up resistor.

## Power Sequencing & Hot-Socketing

Because FLEX 10KE devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The  $V_{CCIO}$  and  $V_{CCINT}$  power planes can be powered in any order.

Signals can be driven into FLEX 10KE devices before and during power up without damaging the device. Additionally, FLEX 10KE devices do not drive out during power up. Once operating conditions are reached, FLEX 10KE devices operate as specified by the user.

*Table 17. 32-Bit IDCODE for FLEX 10KE Devices* *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) (2)
EPF10K30E	0001	0001 0000 0011 0000	00001101110	1
EPF10K50E EPF10K50S	0001	0001 0000 0101 0000	00001101110	1
EPF10K100E	0010	0000 0001 0000 0000	00001101110	1
EPF10K130E	0001	0000 0001 0011 0000	00001101110	1
EPF10K200E EPF10K200S	0001	0000 0010 0000 0000	00001101110	1

**Notes:**

(1) The most significant bit (MSB) is on the left.

(2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

FLEX 10KE devices include weak pull-up resistors on the JTAG pins.



For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Jam Programming & Test Language Specification*

Table 22. FLEX 10KE 2.5-V Device DC Operating Conditions

Notes (6), (7)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IH}$	High-level input voltage		1.7, $0.5 \times V_{CCIO}$ (8)		5.75	V
$V_{IL}$	Low-level input voltage		-0.5		0.8, $0.3 \times V_{CCIO}$ (8)	V
$V_{OH}$	3.3-V high-level TTL output voltage	$I_{OH} = -8$ mA DC, $V_{CCIO} = 3.00$ V (9)	2.4			V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (9)	$V_{CCIO} - 0.2$			V
	3.3-V high-level PCI output voltage	$I_{OH} = -0.5$ mA DC, $V_{CCIO} = 3.00$ to $3.60$ V (9)	$0.9 \times V_{CCIO}$			V
	2.5-V high-level output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 2.30$ V (9)	2.1			V
		$I_{OH} = -1$ mA DC, $V_{CCIO} = 2.30$ V (9)	2.0			V
		$I_{OH} = -2$ mA DC, $V_{CCIO} = 2.30$ V (9)	1.7			V
$V_{OL}$	3.3-V low-level TTL output voltage	$I_{OL} = 12$ mA DC, $V_{CCIO} = 3.00$ V (10)			0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.00$ V (10)			0.2	V
	3.3-V low-level PCI output voltage	$I_{OL} = 1.5$ mA DC, $V_{CCIO} = 3.00$ to $3.60$ V (10)			$0.1 \times V_{CCIO}$	V
	2.5-V low-level output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 2.30$ V (10)			0.2	V
		$I_{OL} = 1$ mA DC, $V_{CCIO} = 2.30$ V (10)			0.4	V
		$I_{OL} = 2$ mA DC, $V_{CCIO} = 2.30$ V (10)			0.7	V
$I_I$	Input pin leakage current	$V_I = V_{CCIOmax}$ to $0$ V (11)	-10		10	$\mu$ A
$I_{OZ}$	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to $0$ V (11)	-10		10	$\mu$ A
$I_{CC0}$	$V_{CC}$ supply current (standby)	$V_I =$ ground, no load, no toggling inputs		5		mA
		$V_I =$ ground, no load, no toggling inputs (12)		10		mA
$R_{CONF}$	Value of I/O pin pull-up resistor before and during configuration	$V_{CCIO} = 3.0$ V (13)	20		50	$k\frac{3}{4}$
		$V_{CCIO} = 2.3$ V (13)	30		80	$k\frac{3}{4}$

Table 23. FLEX 10KE Device Capacitance *Note (14)*

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input capacitance	$V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		10	pF
$C_{INCLK}$	Input capacitance on dedicated clock pin	$V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		12	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		10	pF

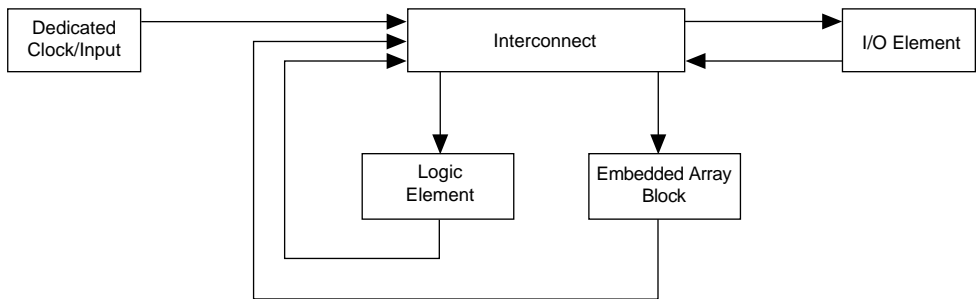
**Notes to tables:**

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input voltage is  $-0.5\text{ V}$ . During transitions, the inputs may undershoot to  $-2.0\text{ V}$  for input currents less than  $100\text{ mA}$  and periods shorter than  $20\text{ ns}$ .
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum  $V_{CC}$  rise time is  $100\text{ ms}$ , and  $V_{CC}$  must rise monotonically.
- (5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before  $V_{CCINT}$  and  $V_{CCIO}$  are powered.
- (6) Typical values are for  $T_A = 25^\circ\text{ C}$ ,  $V_{CCINT} = 2.5\text{ V}$ , and  $V_{CCIO} = 2.5\text{ V}$  or  $3.3\text{ V}$ .
- (7) These values are specified under the FLEX 10KE Recommended Operating Conditions shown in [Tables 20 and 21](#).
- (8) The FLEX 10KE input buffers are compatible with  $2.5\text{-V}$ ,  $3.3\text{-V}$  (LVTTTL and LVCMOS), and  $5.0\text{-V}$  TTL and CMOS signals. Additionally, the input buffers are  $3.3\text{-V}$  PCI compliant when  $V_{CCIO}$  and  $V_{CCINT}$  meet the relationship shown in [Figure 22](#).
- (9) The  $I_{OH}$  parameter refers to high-level TTL, PCI, or CMOS output current.
- (10) The  $I_{OL}$  parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (11) This value is specified for normal device operation. The value may vary during power-up.
- (12) This parameter applies to -1 speed-grade commercial-temperature devices and -2 speed-grade-industrial temperature devices.
- (13) Pin pull-up resistance values will be lower if the pin is driven higher than  $V_{CCIO}$  by an external source.
- (14) Capacitance is sample-tested only.

Timing simulation and delay prediction are available with the Altera Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

Figure 24 shows the overall timing model, which maps the possible paths to and from the various elements of the FLEX 10KE device.

Figure 24. FLEX 10KE Device Timing Model



Figures 25 through 28 show the delays that correspond to various paths and functions within the LE, IOE, EAB, and bidirectional timing models.

Table 34. EPF10K30E Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABAA}$		6.4		7.6		8.8	ns
$t_{EABRCOMB}$	6.4		7.6		8.8		ns
$t_{EABRCREG}$	4.4		5.1		6.0		ns
$t_{EABWP}$	2.5		2.9		3.3		ns
$t_{EABWCOMB}$	6.0		7.0		8.0		ns
$t_{EABWCREG}$	6.8		7.8		9.0		ns
$t_{EABDD}$		5.7		6.7		7.7	ns
$t_{EABDATACO}$		0.8		0.9		1.1	ns
$t_{EABDATASU}$	1.5		1.7		2.0		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	1.3		1.4		1.7		ns
$t_{EABWEH}$	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.5		1.7		2.0		ns
$t_{EABWDH}$	0.0		0.0		0.0		ns
$t_{EABWASU}$	3.0		3.6		4.3		ns
$t_{EABWAH}$	0.5		0.5		0.4		ns
$t_{EABWO}$		5.1		6.0		6.8	ns

Table 35. EPF10K30E Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		1.8		2.4		2.9	ns
$t_{DIN2LE}$		1.5		1.8		2.4	ns
$t_{DIN2DATA}$		1.5		1.8		2.2	ns
$t_{DCLK2IOE}$		2.2		2.6		3.0	ns
$t_{DCLK2LE}$		1.5		1.8		2.4	ns
$t_{SAMELAB}$		0.1		0.2		0.3	ns
$t_{SAMEROW}$		2.0		2.4		2.7	ns
$t_{SAMECOLUMN}$		0.7		1.0		0.8	ns
$t_{DIFFROW}$		2.7		3.4		3.5	ns
$t_{TWOROWS}$		4.7		5.8		6.2	ns
$t_{LEPERIPH}$		2.7		3.4		3.8	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.8		0.8		1.1	ns

Table 36. EPF10K30E External Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DDR}$		8.0		9.5		12.5	ns
$t_{INSU}$ (3)	2.1		2.5		3.9		ns
$t_{INH}$ (3)	0.0		0.0		0.0		ns
$t_{OUTCO}$ (3)	2.0	4.9	2.0	5.9	2.0	7.6	ns
$t_{INSU}$ (4)	1.1		1.5		—		ns
$t_{INH}$ (4)	0.0		0.0		—		ns
$t_{OUTCO}$ (4)	0.5	3.9	0.5	4.9	—	—	ns
$t_{PCISU}$	3.0		4.2		—		ns
$t_{PCIH}$	0.0		0.0		—		ns
$t_{PCICO}$	2.0	6.0	2.0	7.5	—	—	ns

Table 40. EPF10K50E Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.7		2.0		2.7	ns
$t_{EABDATA1}$		0.6		0.7		0.9	ns
$t_{EABWE1}$		1.1		1.3		1.8	ns
$t_{EABWE2}$		0.4		0.4		0.6	ns
$t_{EABRE1}$		0.8		0.9		1.2	ns
$t_{EABRE2}$		0.4		0.4		0.6	ns
$t_{EABCLK}$		0.0		0.0		0.0	ns
$t_{EABCO}$		0.3		0.3		0.5	ns
$t_{EABYPASS}$		0.5		0.6		0.8	ns
$t_{EABSU}$	0.9		1.0		1.4		ns
$t_{EABH}$	0.4		0.4		0.6		ns
$t_{EABCLR}$	0.3		0.3		0.5		ns
$t_{AA}$		3.2		3.8		5.1	ns
$t_{WP}$	2.5		2.9		3.9		ns
$t_{RP}$	0.9		1.1		1.5		ns
$t_{WDSU}$	0.9		1.0		1.4		ns
$t_{WDH}$	0.1		0.1		0.2		ns
$t_{WASU}$	1.7		2.0		2.7		ns
$t_{WAH}$	1.8		2.1		2.9		ns
$t_{RASU}$	3.1		3.7		5.0		ns
$t_{RAH}$	0.2		0.2		0.3		ns
$t_{WO}$		2.5		2.9		3.9	ns
$t_{DD}$		2.5		2.9		3.9	ns
$t_{EABOUT}$		0.5		0.6		0.8	ns
$t_{EABCH}$	1.5		2.0		2.5		ns
$t_{EABCL}$	2.5		2.9		3.9		ns

Table 56. EPF10K130E Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		2.8		3.5		4.4	ns
$t_{DIN2LE}$		0.7		1.2		1.6	ns
$t_{DIN2DATA}$		1.6		1.9		2.2	ns
$t_{DCLK2IOE}$		1.6		2.1		2.7	ns
$t_{DCLK2LE}$		0.7		1.2		1.6	ns
$t_{SAMELAB}$		0.1		0.2		0.2	ns
$t_{SAMEROW}$		1.9		3.4		5.1	ns
$t_{SAMECOLUMN}$		0.9		2.6		4.4	ns
$t_{DIFFROW}$		2.8		6.0		9.5	ns
$t_{TWOROWS}$		4.7		9.4		14.6	ns
$t_{LEPERIPH}$		3.1		4.7		6.9	ns
$t_{LABCARRY}$		0.6		0.8		1.0	ns
$t_{LABCASC}$		0.9		1.2		1.6	ns

Table 57. EPF10K130E External Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DRR}$		9.0		12.0		16.0	ns
$t_{INSU}^{(3)}$	1.9		2.1		3.0		ns
$t_{INH}^{(3)}$	0.0		0.0		0.0		ns
$t_{OUTCO}^{(3)}$	2.0	5.0	2.0	7.0	2.0	9.2	ns
$t_{INSU}^{(4)}$	0.9		1.1		—		ns
$t_{INH}^{(4)}$	0.0		0.0		—		ns
$t_{OUTCO}^{(4)}$	0.5	4.0	0.5	6.0	—	—	ns
$t_{PCISU}$	3.0		6.2		—		ns
$t_{PCIH}$	0.0		0.0		—		ns
$t_{PCICO}$	2.0	6.0	2.0	6.9	—	—	ns

Table 61. EPF10K200E Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		2.0		2.4		3.2	ns
$t_{EABDATA1}$		0.4		0.5		0.6	ns
$t_{EABWE1}$		1.4		1.7		2.3	ns
$t_{EABWE2}$		0.0		0.0		0.0	ns
$t_{EABRE1}$		0		0		0	ns
$t_{EABRE2}$		0.4		0.5		0.6	ns
$t_{EABCLK}$		0.0		0.0		0.0	ns
$t_{EABCO}$		0.8		0.9		1.2	ns
$t_{EABYPASS}$		0.0		0.1		0.1	ns
$t_{EABSU}$	0.9		1.1		1.5		ns
$t_{EABH}$	0.4		0.5		0.6		ns
$t_{EABCLR}$	0.8		0.9		1.2		ns
$t_{AA}$		3.1		3.7		4.9	ns
$t_{WP}$	3.3		4.0		5.3		ns
$t_{RP}$	0.9		1.1		1.5		ns
$t_{WDSU}$	0.9		1.1		1.5		ns
$t_{WDH}$	0.1		0.1		0.1		ns
$t_{WASU}$	1.3		1.6		2.1		ns
$t_{WAH}$	2.1		2.5		3.3		ns
$t_{RASU}$	2.2		2.6		3.5		ns
$t_{RAH}$	0.1		0.1		0.2		ns
$t_{WO}$		2.0		2.4		3.2	ns
$t_{DD}$		2.0		2.4		3.2	ns
$t_{EABOUT}$		0.0		0.1		0.1	ns
$t_{EABCH}$	1.5		2.0		2.5		ns
$t_{EABCL}$	3.3		4.0		5.3		ns

Table 62. EPF10K200E Device EAB Internal Timing Macroparameters (Part 1 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABAA}$		5.1		6.4		8.4	ns
$t_{EABRCOMB}$	5.1		6.4		8.4		ns
$t_{EABRCREG}$	4.8		5.7		7.6		ns
$t_{EABWP}$	3.3		4.0		5.3		ns

Additionally, the Altera software offers several features that help plan for future device migration by preventing the use of conflicting I/O pins.

*Table 81. I/O Counts for FLEX 10KA & FLEX 10KE Devices*

FLEX 10KA		FLEX 10KE	
Device	I/O Count	Device	I/O Count
EPF10K30AF256	191	EPF10K30EF256	176
EPF10K30AF484	246	EPF10K30EF484	220
EPF10K50VB356	274	EPF10K50SB356	220
EPF10K50VF484	291	EPF10K50EF484	254
EPF10K50VF484	291	EPF10K50SF484	254
EPF10K100AF484	369	EPF10K100EF484	338

## Configuration Schemes

The configuration data for a FLEX 10KE device can be loaded with one of five configuration schemes (see [Table 82](#)), chosen on the basis of the target application. An EPC1, EPC2, or EPC16 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of a FLEX 10KE device, allowing automatic configuration on system power-up.

Multiple FLEX 10KE devices can be configured in any of the five configuration schemes by connecting the configuration enable ( $\overline{nCE}$ ) and configuration enable output ( $\overline{nCEO}$ ) pins on each device. Additional FLEX 10K, FLEX 10KA, FLEX 10KE, and FLEX 6000 devices can be configured in the same serial chain.

*Table 82. Data Sources for FLEX 10KE Configuration*

Configuration Scheme	Data Source
Configuration device	EPC1, EPC2, or EPC16 configuration device
Passive serial (PS)	BitBlaster, ByteBlasterMV, or MasterBlaster download cables, or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	BitBlaster or ByteBlasterMV download cables, or microprocessor with a Jam STAPL file or JBC file