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**Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

**Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 1248 |
| Number of Logic Elements/Cells | 9984 |
| Total RAM Bits | 98304 |
| Number of I/O | 369 |
| Number of Gates | 513000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 484-BBGA |
| Supplier Device Package | 484-FBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=epf10k200sfc484-1x |

Table 5. FLEX 10KE Performance

| Application | Resources Used | | Performance | | | Units |
|---|---|---|---|---|---|---|
| | LEs | EABs | -1 Speed Grade | -2 Speed Grade | -3 Speed Grade | |
| 16-bit loadable counter | 16 | 0 | 285 | 250 | 200 | MHz |
| 16-bit accumulator | 16 | 0 | 285 | 250 | 200 | MHz |
| 16-to-1 multiplexer (1) | 10 | 0 | 3.5 | 4.9 | 7.0 | ns |
| 16-bit multiplier with 3-stage pipeline (2) | 592 | 0 | 156 | 131 | 93 | MHz |
| 256 × 16 RAM read cycle speed (2) | 0 | 1 | 196 | 154 | 118 | MHz |
| 256 × 16 RAM write cycle speed (2) | 0 | 1 | 185 | 143 | 106 | MHz |

*Notes:*

(1)    This application uses combinatorial inputs and outputs.

(2)    This application uses registered inputs and outputs.

Table 6 shows FLEX 10KE performance for more complex designs. These designs are available as Altera MegaCore® functions.

Table 6. FLEX 10KE Performance for Complex Designs

| Application | LEs Used | Performance | | | Units |
|---|---|---|---|---|---|
| | | -1 Speed Grade | -2 Speed Grade | -3 Speed Grade | |
| 8-bit, 16-tap parallel finite impulse response (FIR) filter | 597 | 192 | 156 | 116 | MSPS |
| 8-bit, 512-point fast Fourier transform (FFT) function | 1,854 | 23.4 | 28.7 | 38.9 | µs (1) |
| | | 113 | 92 | 68 | MHz |
| a16450 universal asynchronous receiver/transmitter (UART) | 342 | 36 | 28 | 20.5 | MHz |

*Note:*

(1)    These values are for calculation time. Calculation time = number of clocks required/$f_{max}$. Number of clocks required = ceiling [log 2 (points)/2] × [points +14 + ceiling]

The EAB can also be used for bidirectional, dual-port memory applications where two ports read or write simultaneously. To implement this type of dual-port memory, two EABs are used to support two simultaneous read or writes.

Alternatively, one clock and clock enable can be used to control the input registers of the EAB, while a different clock and clock enable control the output registers (see Figure 2).

*Figure 2. FLEX 10KE Device in Dual-Port RAM Mode*    *Notes (1)*
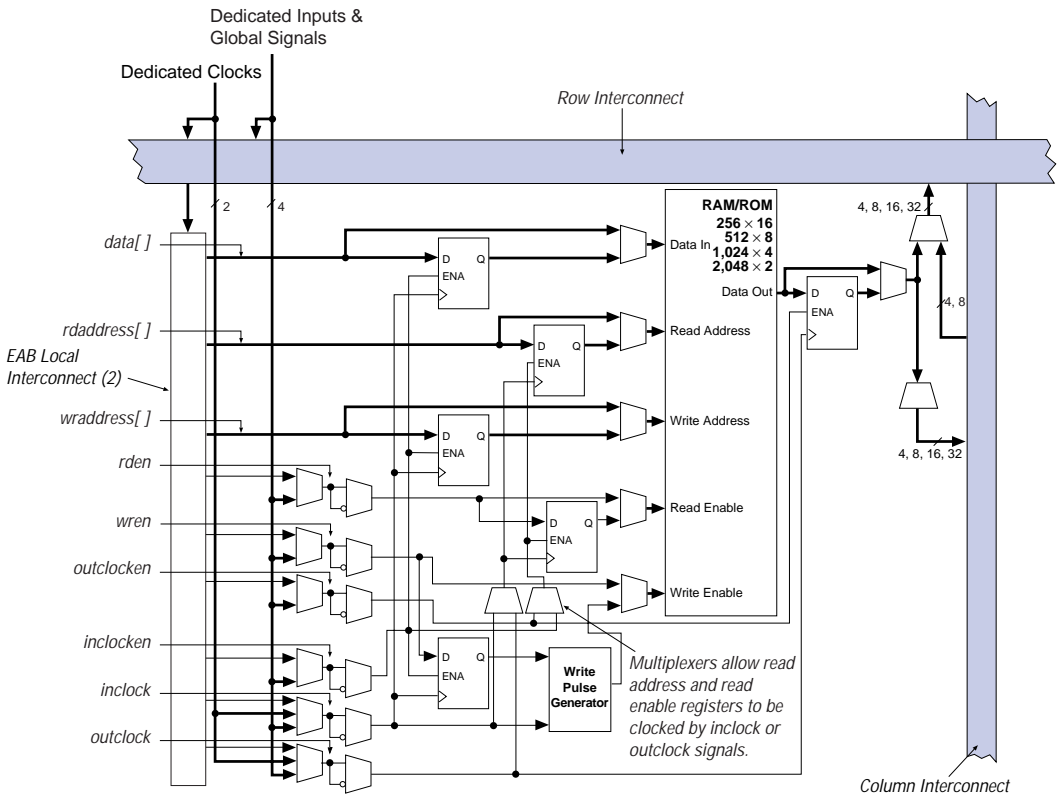


*Notes:*
(1)  All registers can be asynchronously cleared by EAB local interconnect signals, global signals, or the chip-wide reset.
(2)  EPF10K30E and EPF10K50E devices have 88 EAB local interconnect channels; EPF10K100E, EPF10K130E, and EPF10K200E devices have 104 EAB local interconnect channels.

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When used as RAM, each EAB can be configured in any of the following sizes: $256 \times 16$, $512 \times 8$, $1,024 \times 4$, or $2,048 \times 2$ (see Figure 5).

*Figure 5. FLEX 10KE EAB Memory Configurations*



256 × 16          512 × 8          1,024 × 4          2,048 × 2
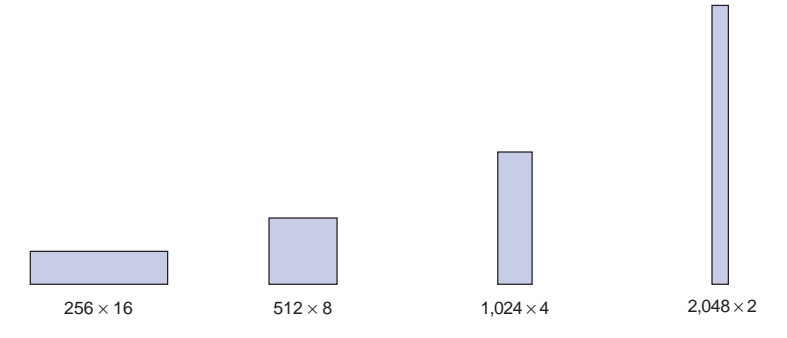
Larger blocks of RAM are created by combining multiple EABs. For example, two $256 \times 16$ RAM blocks can be combined to form a $256 \times 32$ block; two $512 \times 8$ RAM blocks can be combined to form a $512 \times 16$ block (see Figure 6).

*Figure 6. Examples of Combining FLEX 10KE EABs*



256 × 32

256 × 16

256 × 16

512 × 16

512 × 8

512 × 8
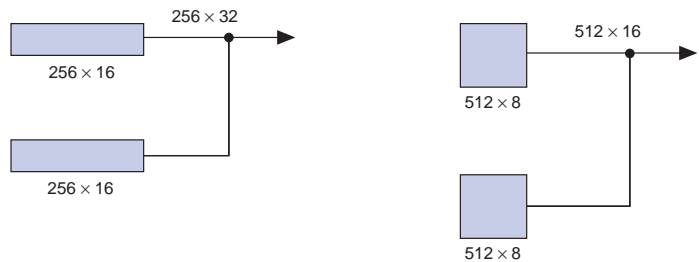
If necessary, all EABs in a device can be cascaded to form a single RAM block. EABs can be cascaded to form RAM blocks of up to 2,048 words without impacting timing. The Altera software automatically combines EABs to meet a designer's RAM specifications.

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks, the other two can be used for clear/preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I/O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I/O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LE in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated from LE outputs.

## Logic Element

The LE, the smallest unit of logic in the FLEX 10KE architecture, has a compact size that provides efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous clock enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect routing structure (see Figure 8).

*Figure 8. FLEX 10KE Logic Element*
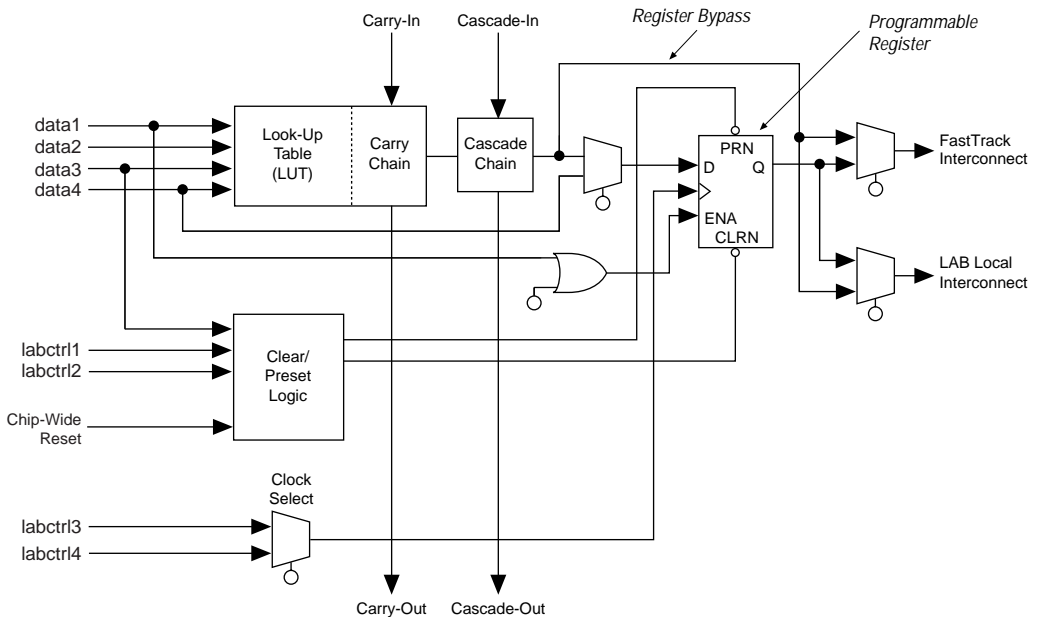
Figure 9 shows how an *n*-bit full adder can be implemented in *n* + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for an accumulator function. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal.

*Figure 9. FLEX 10KE Carry Chain Operation (n-Bit Full Adder)*
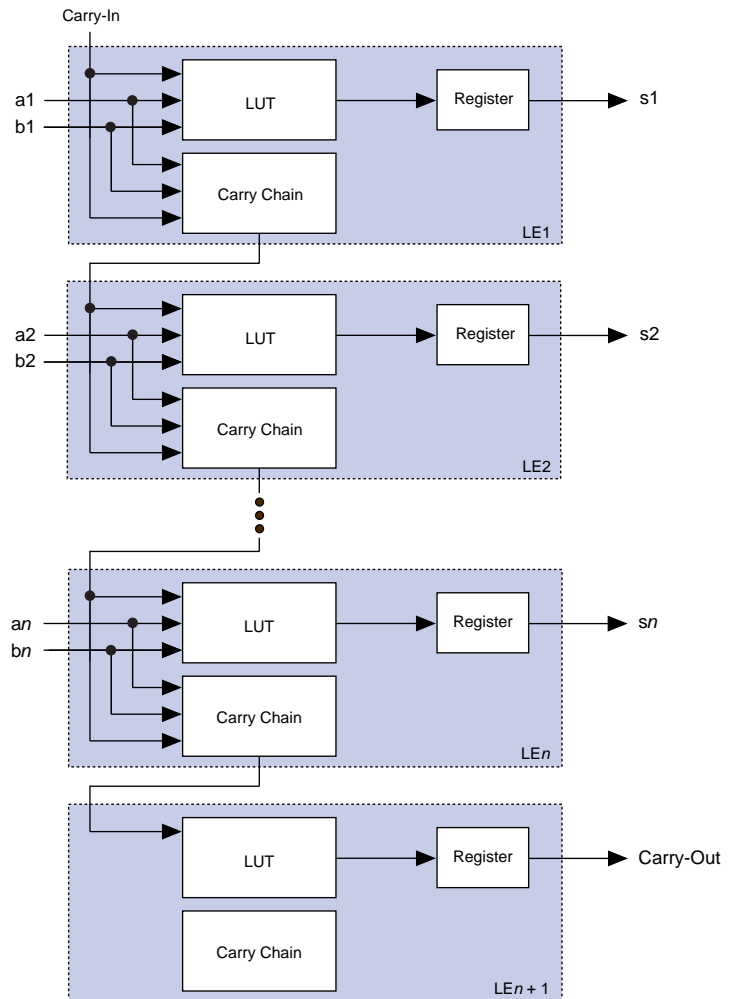
*Cascade Chain*

With the cascade chain, the FLEX 10KE architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. An a delay as low as 0.6 ns per LE, each additional LE provides four more inputs to the effective width of a function. Cascade chain logic can be created automatically by the Altera Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than eight bits are implemented automatically by linking several LABs together. For easier routing, a long cascade chain skips every other LAB in a row. A cascade chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB (e.g., the last LE of the first LAB in a row cascades to the first LE of the third LAB). The cascade chain does not cross the center of the row (e.g., in the EPF10K50E device, the cascade chain stops at the eighteenth LAB and a new one begins at the nineteenth LAB). This break is due to the EAB's placement in the middle of the row.

Figure 10 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of $4n$ variables implemented with $n$ LEs. The LE delay is 0.9 ns; the cascade chain delay is 0.6 ns. With the cascade chain, 2.7 ns are needed to decode a 16-bit address.

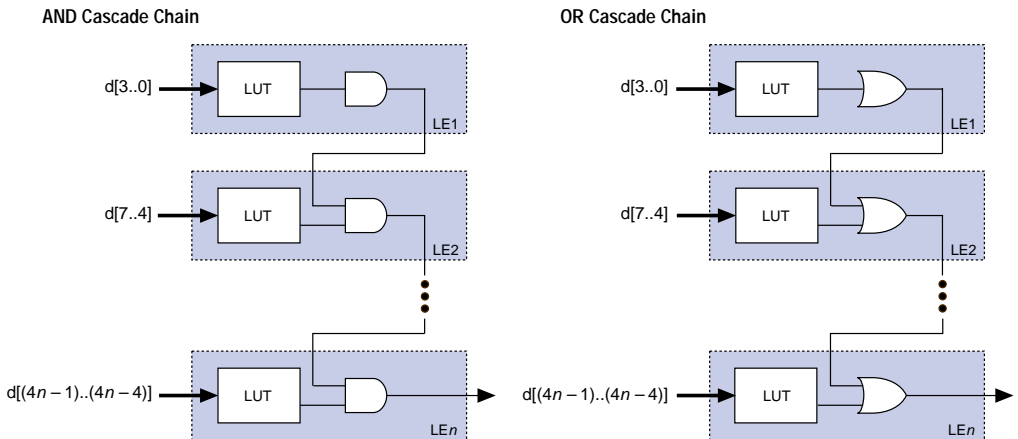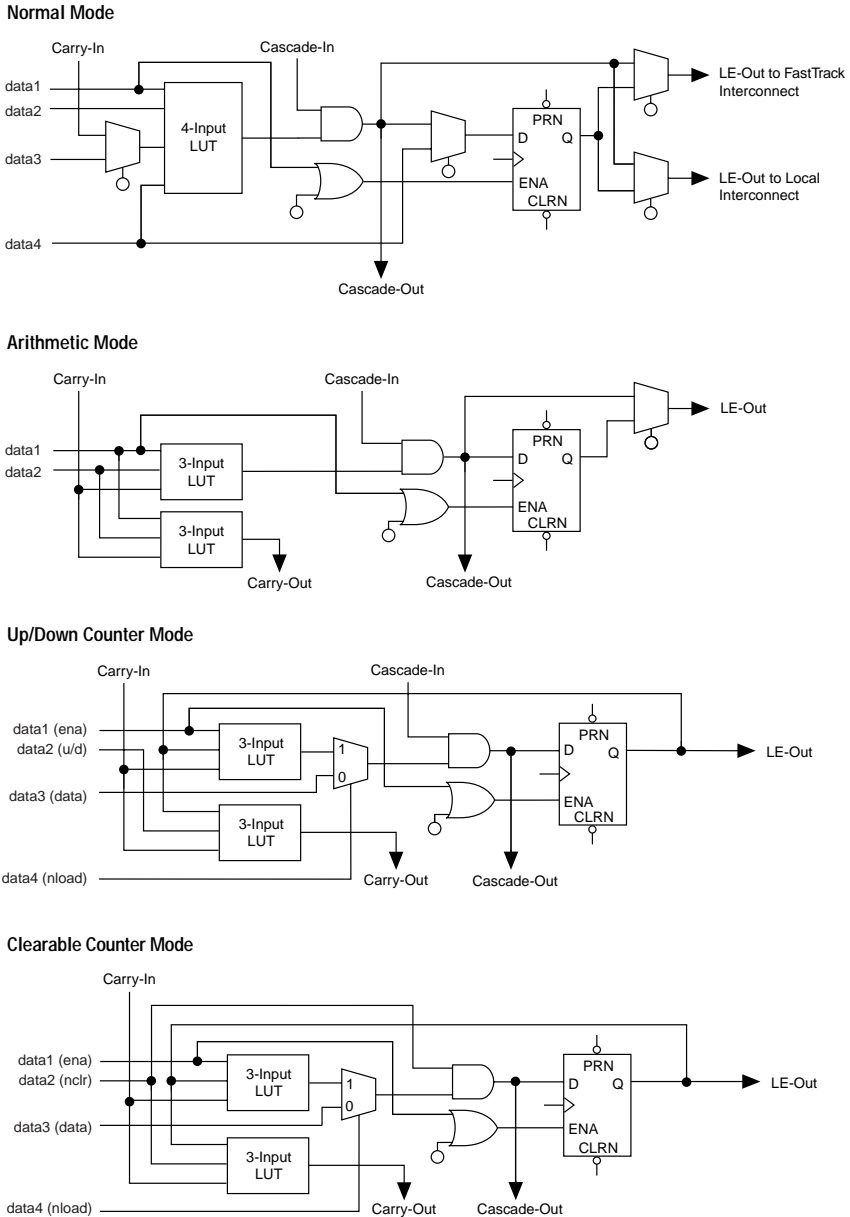*Figure 10. FLEX 10KE Cascade Chain Operation*

Figure 11 shows the LE operating modes.

*Figure 11. FLEX 10KE LE Operating Modes*

### Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Altera Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. Either the register or the LUT can be used to drive both the local interconnect and the FastTrack Interconnect routing structure at the same time.

The LUT and the register in the LE can be used independently (register packing). To support register packing, the LE has two outputs; one drives the local interconnect, and the other drives the FastTrack Interconnect routing structure. The DATA4 signal can drive the register directly, allowing the LUT to compute a function that is independent of the registered signal; a three-input function can be computed in the LUT, and a fourth independent signal can be registered. Alternatively, a four-input function can be generated, and one of the inputs to this function can be used to drive the register. The register in a packed LE can still use the clock enable, clear, and preset signals in the LE. In a packed LE, the register can drive the FastTrack Interconnect routing structure while the LUT drives the local interconnect, or vice versa.

### Arithmetic Mode

The arithmetic mode offers 2 three-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 11 on page 22, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three signals: a, b, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

### Up/Down Counter Mode

The up/down counter mode offers counter enable, clock enable, synchronous up/down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Use 2 three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the clear and preset register control signals without using the LUT resources.

On all FLEX 10KE devices (except EPF10K50E and EPF10K200E devices), the input path from the I/O pad to the FastTrack Interconnect has a programmable delay element that can be used to guarantee a zero hold time. EPF10K50S and EPF10K200S devices also support this feature. Depending on the placement of the IOE relative to what it is driving, the designer may choose to turn on the programmable delay to ensure a zero hold time or turn it off to minimize setup time. This feature is used to reduce setup time for complex pin-to-register paths (e.g., PCI designs).

Each IOE selects the clock, clear, clock enable, and output enable controls from a network of I/O control signals called the peripheral control bus. The peripheral control bus uses high-speed drivers to minimize signal skew across the device and provides up to 12 peripheral control signals that can be allocated as follows:

■   Up to eight output enable signals
■   Up to six clock enable signals
■   Up to two clock signals
■   Up to two clear signals

If more than six clock enable or eight output enable signals are required, each IOE on the device can be controlled by clock enable and output enable signals driven by specific LEs. In addition to the two clock signals available on the peripheral control bus, each IOE can use one of two dedicated clock pins. Each peripheral control signal can be driven by any of the dedicated input pins or the first LE of each LAB in a particular row. In addition, a LE in a different row can drive a column interconnect, which causes a row interconnect to drive the peripheral control signal. The chip-wide reset signal resets all IOE registers, overriding any other control signals.

When a dedicated clock pin drives IOE registers, it can be inverted for all IOEs in the device. All IOEs must use the same sense of the clock. For example, if any IOE uses the inverted clock, all IOEs must use the inverted clock and no IOE can use the non-inverted clock. However, LEs can still use the true or complement of the clock on a LAB-by-LAB basis.

The incoming signal may be inverted at the dedicated clock pin and will drive all IOEs. For the true and complement of a clock to be used to drive IOEs, drive it into both global clock pins. One global clock pin will supply the true, and the other will supply the complement.

When the true and complement of a dedicated input drives IOE clocks, two signals on the peripheral control bus are consumed, one for each sense of the clock.

### Row-to-IOE Connections

When an IOE is used as an input signal, it can drive two separate row channels. The signal is accessible by all LEs within that row. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the row channels. Up to eight IOEs connect to each side of each row channel (see Figure 16).

*Figure 16. FLEX 10KE Row-to-IOE Connections*

*The values for m and n are provided in Table 10.*
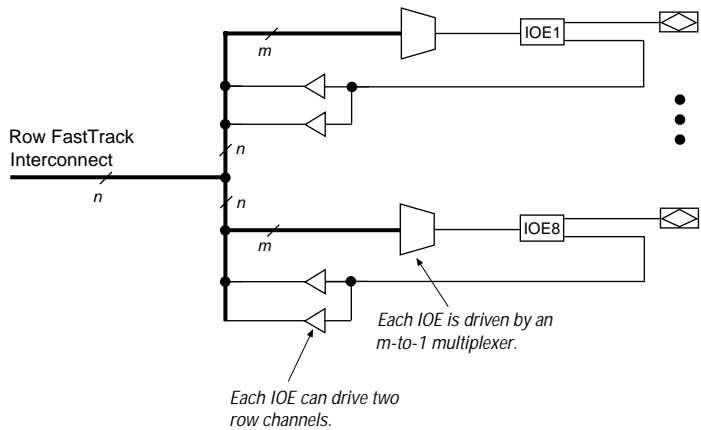


Table 10 lists the FLEX 10KE row-to-IOE interconnect resources.

| Table 10. FLEX 10KE Row-to-IOE Interconnect Resources | | |
|---|---|---|
| Device | Channels per Row (n) | Row Channels per Pin (m) |
| EPF10K30E | 216 | 27 |
| EPF10K50E EPF10K50S | 216 | 27 |
| EPF10K100E | 312 | 39 |
| EPF10K130E | 312 | 39 |
| EPF10K200E EPF10K200S | 312 | 39 |

## SameFrame Pin-Outs

FLEX 10KE devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EPF10K30E device in a 256-pin FineLine BGA package to an EPF10K200S device in a 672-pin FineLine BGA package.

The Altera software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software generates pin-outs describing how to lay out a board to take advantage of this migration (see Figure 18).

*Figure 18. SameFrame Pin-Out Example*



Printed Circuit Board
Designed for 672-Pin FineLine BGA Package

100-Pin FineLine BGA

256-Pin FineLine BGA

256-Pin FineLine BGA Package
(Reduced I/O Count or
Logic Requirements)

672-Pin FineLine BGA Package
(Increased I/O Count or
Logic Requirements)
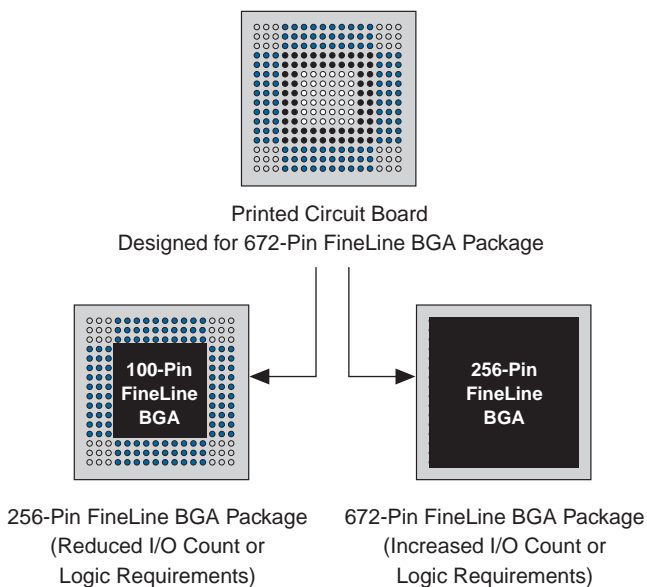
*Table 20. 2.5-V EPF10K50E & EPF10K200E Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------|-----------|------------|-----|-----|------|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3), (4)* | 2.30 (2.30) | 2.70 (2.70) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(3), (4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(3), (4)* | 2.30 (2.30) | 2.70 (2.70) | V |
| $V_I$ | Input voltage | *(5)* | −0.5 | 5.75 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient temperature | For commercial use | 0 | 70 | °C |
| | | For industrial use | −40 | 85 | °C |
| $T_J$ | Operating temperature | For commercial use | 0 | 85 | °C |
| | | For industrial use | −40 | 100 | °C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

*Table 21. 2.5-V EPF10K30E, EPF10K50S, EPF10K100E, EPF10K130E & EPF10K200S Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------|-----------|------------|-----|-----|------|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3), (4)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(3), (4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(3), (4)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_I$ | Input voltage | *(5)* | −0.5 | 5.75 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient temperature | For commercial use | 0 | 70 | °C |
| | | For industrial use | −40 | 85 | °C |
| $T_J$ | Operating temperature | For commercial use | 0 | 85 | °C |
| | | For industrial use | −40 | 100 | °C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

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Timing simulation and delay prediction are available with the Altera Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

Figure 24 shows the overall timing model, which maps the possible paths to and from the various elements of the FLEX 10KE device.

*Figure 24. FLEX 10KE Device Timing Model*
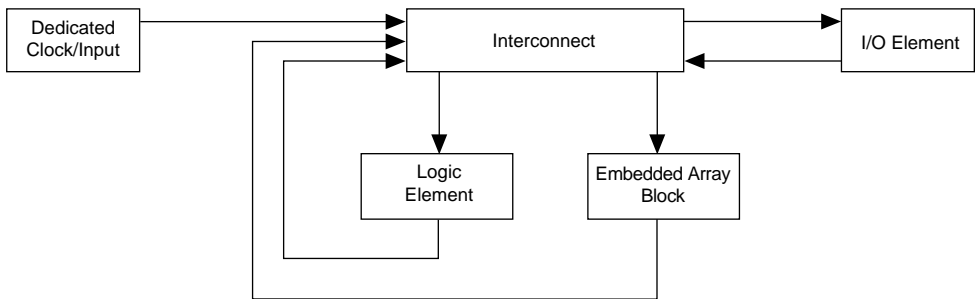


Figures 25 through 28 show the delays that correspond to various paths and functions within the LE, IOE, EAB, and bidirectional timing models.

*Table 30. External Bidirectional Timing Parameters*    *Note (9)*

| Symbol | Parameter | Conditions |
|--------|-----------|------------|
| $t_{INSUBIDIR}$ | Setup time for bi-directional pins with global clock at same-row or same-column LE register | |
| $t_{INHBIDIR}$ | Hold time for bidirectional pins with global clock at same-row or same-column LE register | |
| $t_{INH}$ | Hold time with global clock at IOE register | |
| $t_{OUTCOBIDIR}$ | Clock-to-output delay for bidirectional pins with global clock at IOE register | C1 = 35 pF |
| $t_{XZBIDIR}$ | Synchronous IOE output buffer disable delay | C1 = 35 pF |
| $t_{ZXBIDIR}$ | Synchronous IOE output buffer enable delay, slow slew rate= off | C1 = 35 pF |

*Notes to tables:*

(1)  Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.
(2)  Operating conditions:   VCCIO = 3.3 V ±10% for commercial or industrial use.
(3)  Operating conditions:   VCCIO = 2.5 V ±5% for commercial or industrial use in EPF10K30E, EPF10K50S, EPF10K100E, EPF10K130E, and EPF10K200S devices.
(4)  Operating conditions:   VCCIO = 3.3 V.
(5)  Because the RAM in the EAB is self-timed, this parameter can be ignored when the WE signal is registered.
(6)  EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.
(7)  These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.
(8)  Contact Altera Applications for test circuit specifications and test conditions.
(9)  This timing parameter is sample-tested only.
(10) This parameter is measured with the measurement and test conditions, including load, specified in the PCI Local Bus Specification, revision 2.2.

### Table 31. EPF10K30E Device LE Timing Microparameters  (Part 2 of 2) *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CGENR}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CASC}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_C$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{CO}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{COMB}$ | | 0.4 | | 0.4 | | 0.6 | ns |
| $t_{SU}$ | 0.4 | | 0.6 | | 0.6 | | ns |
| $t_H$ | 0.7 | | 1.0 | | 1.3 | | ns |
| $t_{PRE}$ | | 0.8 | | 0.9 | | 1.2 | ns |
| $t_{CLR}$ | | 0.8 | | 0.9 | | 1.2 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 2.5 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 2.5 | | ns |

### Table 32. EPF10K30E Device IOE Timing Microparameters *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 2.4 | | 2.8 | | 3.8 | ns |
| $t_{IOC}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{IOCO}$ | | 1.0 | | 1.1 | | 1.6 | ns |
| $t_{IOCOMB}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{IOSU}$ | 1.2 | | 1.4 | | 1.9 | | ns |
| $t_{IOH}$ | 0.3 | | 0.4 | | 0.5 | | ns |
| $t_{IOCLR}$ | | 1.0 | | 1.1 | | 1.6 | ns |
| $t_{OD1}$ | | 1.9 | | 2.3 | | 3.0 | ns |
| $t_{OD2}$ | | 1.4 | | 1.8 | | 2.5 | ns |
| $t_{OD3}$ | | 4.4 | | 5.2 | | 7.0 | ns |
| $t_{XZ}$ | | 2.7 | | 3.1 | | 4.3 | ns |
| $t_{ZX1}$ | | 2.7 | | 3.1 | | 4.3 | ns |
| $t_{ZX2}$ | | 2.2 | | 2.6 | | 3.8 | ns |
| $t_{ZX3}$ | | 5.2 | | 6.0 | | 8.3 | ns |
| $t_{INREG}$ | | 3.4 | | 4.1 | | 5.5 | ns |
| $t_{IOFD}$ | | 0.8 | | 1.3 | | 2.4 | ns |
| $t_{INCOMB}$ | | 0.8 | | 1.3 | | 2.4 | ns |

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## Table 45. EPF10K100E Device LE Timing Microparameters *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CGENR}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CASC}$ | | 0.6 | | 0.9 | | 1.2 | ns |
| $t_C$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{CO}$ | | 0.6 | | 0.8 | | 1.1 | ns |
| $t_{COMB}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{SU}$ | 0.4 | | 0.6 | | 0.7 | | ns |
| $t_H$ | 0.5 | | 0.7 | | 0.9 | | ns |
| $t_{PRE}$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{CLR}$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{CH}$ | 1.5 | | 2.0 | | 2.5 | | ns |
| $t_{CL}$ | 1.5 | | 2.0 | | 2.5 | | ns |

## Table 46. EPF10K100E Device IOE Timing Microparameters *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 1.7 | | 2.0 | | 2.6 | ns |
| $t_{IOC}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{IOCO}$ | | 1.4 | | 1.6 | | 2.1 | ns |
| $t_{IOCOMB}$ | | 0.5 | | 0.7 | | 0.9 | ns |
| $t_{IOSU}$ | 0.8 | | 1.0 | | 1.3 | | ns |
| $t_{IOH}$ | 0.7 | | 0.9 | | 1.2 | | ns |
| $t_{IOCLR}$ | | 0.5 | | 0.7 | | 0.9 | ns |
| $t_{OD1}$ | | 3.0 | | 4.2 | | 5.6 | ns |
| $t_{OD2}$ | | 3.0 | | 4.2 | | 5.6 | ns |
| $t_{OD3}$ | | 4.0 | | 5.5 | | 7.3 | ns |
| $t_{XZ}$ | | 3.5 | | 4.6 | | 6.1 | ns |
| $t_{ZX1}$ | | 3.5 | | 4.6 | | 6.1 | ns |
| $t_{ZX2}$ | | 3.5 | | 4.6 | | 6.1 | ns |
| $t_{ZX3}$ | | 4.5 | | 5.9 | | 7.8 | ns |
| $t_{INREG}$ | | 2.0 | | 2.6 | | 3.5 | ns |
| $t_{IOFD}$ | | 0.5 | | 0.8 | | 1.2 | ns |
| $t_{INCOMB}$ | | 0.5 | | 0.8 | | 1.2 | ns |

*Table 59. EPF10K200E Device LE Timing Microparameters* *(Part 2 of 2)* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_H$ | 0.9 | | 1.1 | | 1.5 | | ns |
| $t_{PRE}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{CLR}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 3.0 | | ns |

*Table 60. EPF10K200E Device IOE Timing Microparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 1.6 | | 1.9 | | 2.6 | ns |
| $t_{IOC}$ | | 0.3 | | 0.3 | | 0.5 | ns |
| $t_{IOCO}$ | | 1.6 | | 1.9 | | 2.6 | ns |
| $t_{IOCOMB}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{IOSU}$ | 0.8 | | 0.9 | | 1.2 | | ns |
| $t_{IOH}$ | 0.7 | | 0.8 | | 1.1 | | ns |
| $t_{IOCLR}$ | | 0.2 | | 0.2 | | 0.3 | ns |
| $t_{OD1}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{OD2}$ | | 0.1 | | 0.2 | | 0.7 | ns |
| $t_{OD3}$ | | 2.5 | | 3.0 | | 3.9 | ns |
| $t_{XZ}$ | | 4.4 | | 5.3 | | 7.1 | ns |
| $t_{ZX1}$ | | 4.4 | | 5.3 | | 7.1 | ns |
| $t_{ZX2}$ | | 3.9 | | 4.8 | | 6.9 | ns |
| $t_{ZX3}$ | | 6.3 | | 7.6 | | 10.1 | ns |
| $t_{INREG}$ | | 4.8 | | 5.7 | | 7.7 | ns |
| $t_{IOFD}$ | | 1.5 | | 1.8 | | 2.4 | ns |
| $t_{INCOMB}$ | | 1.5 | | 1.8 | | 2.4 | ns |

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Table 61. EPF10K200E Device EAB Internal Microparameters *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 2.0 | | 2.4 | | 3.2 | ns |
| $t_{EABDATA1}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{EABWE1}$ | | 1.4 | | 1.7 | | 2.3 | ns |
| $t_{EABWE2}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABRE1}$ | | 0 | | 0 | | 0 | ns |
| $t_{EABRE2}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{EABCLK}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCO}$ | | 0.8 | | 0.9 | | 1.2 | ns |
| $t_{EABBYPASS}$ | | 0.0 | | 0.1 | | 0.1 | ns |
| $t_{EABSU}$ | 0.9 | | 1.1 | | 1.5 | | ns |
| $t_{EABH}$ | 0.4 | | 0.5 | | 0.6 | | ns |
| $t_{EABCLR}$ | 0.8 | | 0.9 | | 1.2 | | ns |
| $t_{AA}$ | | 3.1 | | 3.7 | | 4.9 | ns |
| $t_{WP}$ | 3.3 | | 4.0 | | 5.3 | | ns |
| $t_{RP}$ | 0.9 | | 1.1 | | 1.5 | | ns |
| $t_{WDSU}$ | 0.9 | | 1.1 | | 1.5 | | ns |
| $t_{WDH}$ | 0.1 | | 0.1 | | 0.1 | | ns |
| $t_{WASU}$ | 1.3 | | 1.6 | | 2.1 | | ns |
| $t_{WAH}$ | 2.1 | | 2.5 | | 3.3 | | ns |
| $t_{RASU}$ | 2.2 | | 2.6 | | 3.5 | | ns |
| $t_{RAH}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{WO}$ | | 2.0 | | 2.4 | | 3.2 | ns |
| $t_{DD}$ | | 2.0 | | 2.4 | | 3.2 | ns |
| $t_{EABOUT}$ | | 0.0 | | 0.1 | | 0.1 | ns |
| $t_{EABCH}$ | 1.5 | | 2.0 | | 2.5 | | ns |
| $t_{EABCL}$ | 3.3 | | 4.0 | | 5.3 | | ns |

Table 62. EPF10K200E Device EAB Internal Timing Macroparameters  (Part 1 of 2) *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABAA}$ | | 5.1 | | 6.4 | | 8.4 | ns |
| $t_{EABRCOMB}$ | 5.1 | | 6.4 | | 8.4 | | ns |
| $t_{EABRCREG}$ | 4.8 | | 5.7 | | 7.6 | | ns |
| $t_{EABWP}$ | 3.3 | | 4.0 | | 5.3 | | ns |

*Table 66. EPF10K50S Device LE Timing Microparameters  (Part 2 of 2) Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CGENR}$ | | 0.1 | | 0.1 | | 0.1 | ns |
| $t_{CASC}$ | | 0.5 | | 0.8 | | 1.0 | ns |
| $t_C$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{CO}$ | | 0.6 | | 0.6 | | 0.7 | ns |
| $t_{COMB}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{SU}$ | 0.5 | | 0.6 | | 0.7 | | ns |
| $t_H$ | 0.5 | | 0.6 | | 0.8 | | ns |
| $t_{PRE}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{CLR}$ | | 0.8 | | 1.0 | | 1.2 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 3.0 | | ns |

*Table 67. EPF10K50S Device IOE Timing Microparameters  Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 1.3 | | 1.3 | | 1.9 | ns |
| $t_{IOC}$ | | 0.3 | | 0.4 | | 0.4 | ns |
| $t_{IOCO}$ | | 1.7 | | 2.1 | | 2.6 | ns |
| $t_{IOCOMB}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{IOSU}$ | 0.8 | | 1.0 | | 1.3 | | ns |
| $t_{IOH}$ | 0.4 | | 0.5 | | 0.6 | | ns |
| $t_{IOCLR}$ | | 0.2 | | 0.2 | | 0.4 | ns |
| $t_{OD1}$ | | 1.2 | | 1.2 | | 1.9 | ns |
| $t_{OD2}$ | | 0.7 | | 0.8 | | 1.7 | ns |
| $t_{OD3}$ | | 2.7 | | 3.0 | | 4.3 | ns |
| $t_{XZ}$ | | 4.7 | | 5.7 | | 7.5 | ns |
| $t_{ZX1}$ | | 4.7 | | 5.7 | | 7.5 | ns |
| $t_{ZX2}$ | | 4.2 | | 5.3 | | 7.3 | ns |
| $t_{ZX3}$ | | 6.2 | | 7.5 | | 9.9 | ns |
| $t_{INREG}$ | | 3.5 | | 4.2 | | 5.6 | ns |
| $t_{IOFD}$ | | 1.1 | | 1.3 | | 1.8 | ns |
| $t_{INCOMB}$ | | 1.1 | | 1.3 | | 1.8 | ns |

## Table 74. EPF10K200S Device IOE Timing Microparameters  (Part 2 of 2)   *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ZX2}$ | | 4.5 | | 4.8 | | 6.6 | ns |
| $t_{ZX3}$ | | 6.6 | | 7.6 | | 10.1 | ns |
| $t_{INREG}$ | | 3.7 | | 5.7 | | 7.7 | ns |
| $t_{IOFD}$ | | 1.8 | | 3.4 | | 4.0 | ns |
| $t_{INCOMB}$ | | 1.8 | | 3.4 | | 4.0 | ns |

## Table 75. EPF10K200S Device EAB Internal Microparameters   *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 1.8 | | 2.4 | | 3.2 | ns |
| $t_{EABDATA1}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{EABWE1}$ | | 1.1 | | 1.7 | | 2.3 | ns |
| $t_{EABWE2}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABRE1}$ | | 0 | | 0 | | 0 | ns |
| $t_{EABRE2}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{EABCLK}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCO}$ | | 0.8 | | 0.9 | | 1.2 | ns |
| $t_{EABBYPASS}$ | | 0.0 | | 0.1 | | 0.1 | ns |
| $t_{EABSU}$ | 0.7 | | 1.1 | | 1.5 | | ns |
| $t_{EABH}$ | 0.4 | | 0.5 | | 0.6 | | ns |
| $t_{EABCLR}$ | 0.8 | | 0.9 | | 1.2 | | ns |
| $t_{AA}$ | | 2.1 | | 3.7 | | 4.9 | ns |
| $t_{WP}$ | 2.1 | | 4.0 | | 5.3 | | ns |
| $t_{RP}$ | 1.1 | | 1.1 | | 1.5 | | ns |
| $t_{WDSU}$ | 0.5 | | 1.1 | | 1.5 | | ns |
| $t_{WDH}$ | 0.1 | | 0.1 | | 0.1 | | ns |
| $t_{WASU}$ | 1.1 | | 1.6 | | 2.1 | | ns |
| $t_{WAH}$ | 1.6 | | 2.5 | | 3.3 | | ns |
| $t_{RASU}$ | 1.6 | | 2.6 | | 3.5 | | ns |
| $t_{RAH}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{WO}$ | | 2.0 | | 2.4 | | 3.2 | ns |
| $t_{DD}$ | | 2.0 | | 2.4 | | 3.2 | ns |
| $t_{EABOUT}$ | | 0.0 | | 0.1 | | 0.1 | ns |
| $t_{EABCH}$ | 1.5 | | 2.0 | | 2.5 | | ns |
| $t_{EABCL}$ | 2.1 | | 2.8 | | 3.8 | | ns |