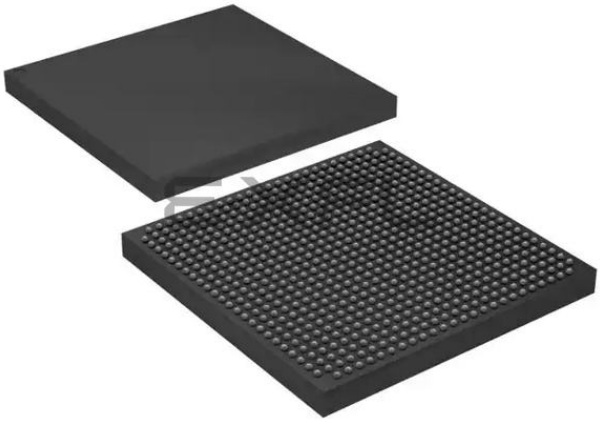

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 1248 |
| Number of Logic Elements/Cells | 9984 |
| Total RAM Bits | 98304 |
| Number of I/O | 470 |
| Number of Gates | 513000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 672-BBGA |
| Supplier Device Package | 672-FBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epf10k200sfi672-2b |

- Software design support and automatic place-and-route provided by Altera's development systems for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800
- Flexible package options
  - Available in a variety of packages with 144 to 672 pins, including the innovative FineLine BGA™ packages (see Tables 3 and 4)
  - SameFrame™ pin-out compatibility between FLEX 10KA and FLEX 10KE devices across a range of device densities and pin counts
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), DesignWare components, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, VeriBest, and Viewlogic

*Table 3. FLEX 10KE Package Options & I/O Pin Count* *Notes (1), (2)*

| Device | 144-Pin TQFP | 208-Pin PQFP | 240-Pin PQFP RQFP | 256-Pin FineLine BGA | 356-Pin BGA | 484-Pin FineLine BGA | 599-Pin PGA | 600-Pin BGA | 672-Pin FineLine BGA |
|---|---|---|---|---|---|---|---|---|---|
| EPF10K30E | 102 | 147 | | 176 | | 220 | | | 220 *(3)* |
| EPF10K50E | 102 | 147 | 189 | 191 | | 254 | | | 254 *(3)* |
| EPF10K50S | 102 | 147 | 189 | 191 | 220 | 254 | | | 254 *(3)* |
| EPF10K100E | | 147 | 189 | 191 | 274 | 338 | | | 338 *(3)* |
| EPF10K130E | | | 186 | | 274 | 369 | | 424 | 413 |
| EPF10K200E | | | | | | | 470 | 470 | 470 |
| EPF10K200S | | | 182 | | 274 | 369 | 470 | 470 | 470 |

***Notes:***

(1) FLEX 10KE device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), pin-grid array (PGA), and ball-grid array (BGA) packages.

(2) Devices in the same package are pin-compatible, although some devices have more I/O pins than others. When planning device migration, use the I/O pins that are common to all devices.

(3) This option is supported with a 484-pin FineLine BGA package. By using SameFrame pin migration, all FineLine BGA packages are pin-compatible. For example, a board can be designed to support 256-pin, 484-pin, and 672-pin FineLine BGA packages. The Altera software automatically avoids conflicting pins when future migration is set.

### Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Altera Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. Either the register or the LUT can be used to drive both the local interconnect and the FastTrack Interconnect routing structure at the same time.

The LUT and the register in the LE can be used independently (register packing). To support register packing, the LE has two outputs; one drives the local interconnect, and the other drives the FastTrack Interconnect routing structure. The DATA4 signal can drive the register directly, allowing the LUT to compute a function that is independent of the registered signal; a three-input function can be computed in the LUT, and a fourth independent signal can be registered. Alternatively, a four-input function can be generated, and one of the inputs to this function can be used to drive the register. The register in a packed LE can still use the clock enable, clear, and preset signals in the LE. In a packed LE, the register can drive the FastTrack Interconnect routing structure while the LUT drives the local interconnect, or vice versa.

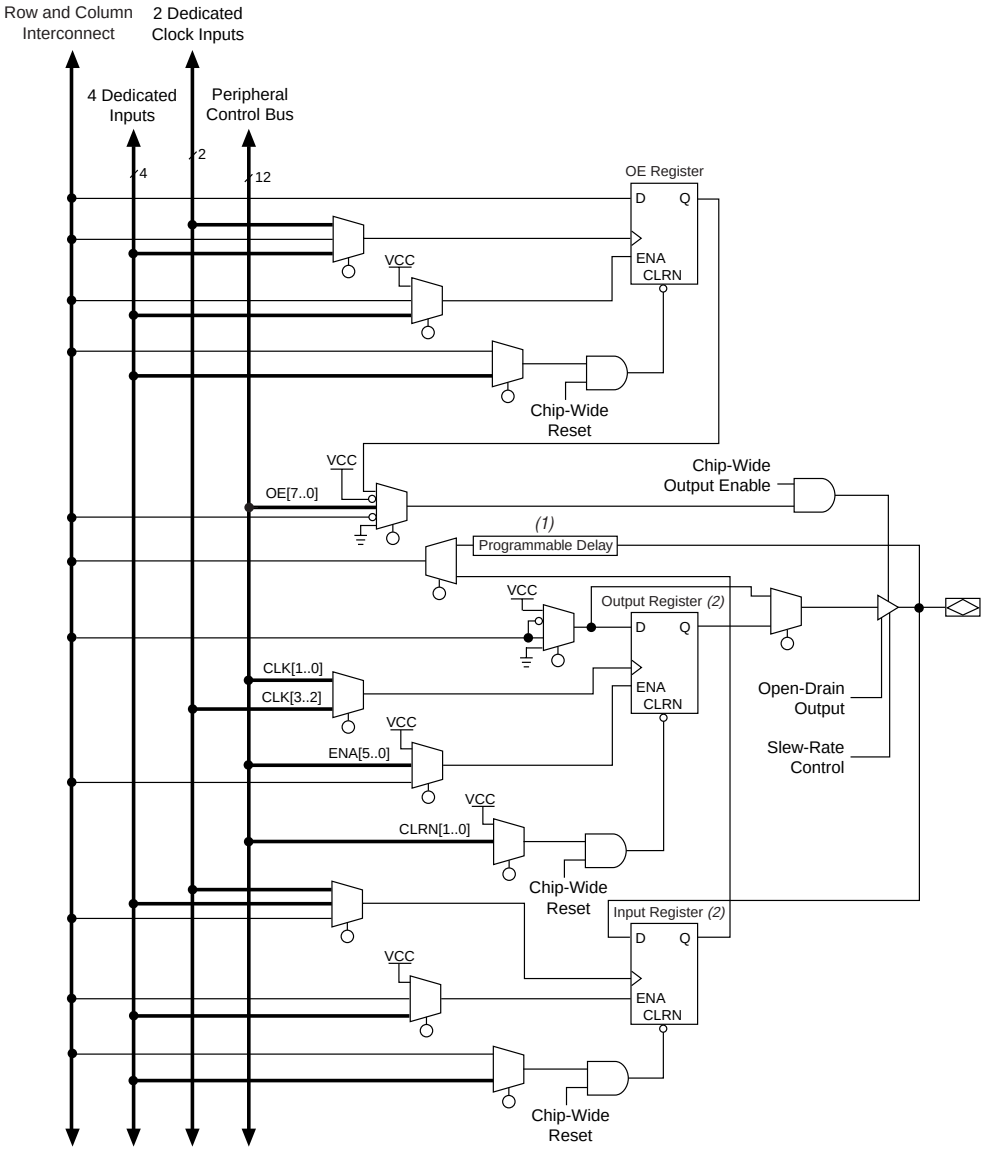
### Arithmetic Mode

The arithmetic mode offers 2 three-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 11 on page 22, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three signals: a, b, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

### Up/Down Counter Mode

The up / down counter mode offers counter enable, clock enable, synchronous up / down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Use 2 three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the clear and preset register control signals without using the LUT resources.

*Figure 15. FLEX 10KE Bidirectional I/O Registers*




***Note:***

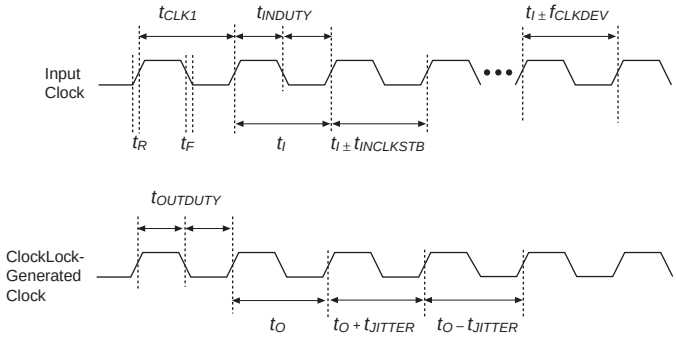
(1) All FLEX 10KE devices (except the EPF10K50E and EPF10K200E devices) have a programmable input delay buffer on the input path.

## ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. Figure 19 shows the incoming and generated clock specifications.

***Figure 19. Specifications for Incoming & Generated Clocks***

*The $t_I$ parameter refers to the nominal input clock period; the $t_O$ parameter refers to the nominal output clock period.*



Tables 12 and 13 summarize the ClockLock and ClockBoost parameters for -1 and -2 speed-grade devices, respectively.

*Table 12. ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices*

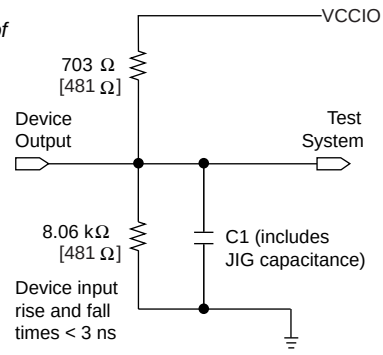
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_R$ | Input rise time | | | | 5 | ns |
| $t_F$ | Input fall time | | | | 5 | ns |
| $t_{INDUTY}$ | Input duty cycle | | 40 | | 60 | % |
| $f_{CLK1}$ | Input clock frequency (ClockBoost clock multiplication factor equals 1) | | 25 | | 180 | MHz |
| $f_{CLK2}$ | Input clock frequency (ClockBoost clock multiplication factor equals 2) | | 16 | | 90 | MHz |
| $f_{CLKDEV}$ | Input deviation from user specification in the MAX+PLUS II software *(1)* | | | | 25,000 *(2)* | PPM |
| $t_{INCLKSTB}$ | Input clock stability (measured between adjacent clocks) | | | | 100 | ps |
| $t_{LOCK}$ | Time required for ClockLock or ClockBoost to acquire lock *(3)* | | | | 10 | µs |
| $t_{JITTER}$ | Jitter on ClockLock or ClockBoost-generated clock *(4)* | $t_{INCLKSTB}$ < 100 | | | 250 | ps |
| | | $t_{INCLKSTB}$ < 50 | | | 200 *(4)* | ps |
| $t_{OUTDUTY}$ | Duty cycle for ClockLock or ClockBoost-generated clock | | 40 | 50 | 60 | % |

## Generic Testing

Each FLEX 10KE device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for FLEX 10KE devices are made under conditions equivalent to those shown in Figure 21. Multiple test patterns can be used to configure devices during all stages of the production flow.

***Figure 21. FLEX 10KE AC Test Conditions***

*Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V devices or outputs. Numbers without brackets are for 3.3-V. devices or outputs.*




## Operating Conditions

Tables 19 through 23 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V FLEX 10KE devices.

***Table 19. FLEX 10KE 2.5-V Device Absolute Maximum Ratings*** *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage | With respect to ground *(2)* | –0.5 | 3.6 | V |
| $V_{CCIO}$ | | | –0.5 | 4.6 | V |
| $V_I$ | DC input voltage | | –2.0 | 5.75 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | PQFP, TQFP, BGA, and FineLine BGA packages, under bias | | 135 | ° C |
| | | Ceramic PGA packages, under bias | | 150 | ° C |

*Table 20. 2.5-V EPF10K50E & EPF10K200E Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3)*, *(4)* | 2.30 (2.30) | 2.70 (2.70) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(3)*, *(4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(3)*, *(4)* | 2.30 (2.30) | 2.70 (2.70) | V |
| $V_I$ | Input voltage | *(5)* | –0.5 | 5.75 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient temperature | For commercial use | 0 | 70 | ° C |
| | | For industrial use | –40 | 85 | ° C |
| $T_J$ | Operating temperature | For commercial use | 0 | 85 | ° C |
| | | For industrial use | –40 | 100 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

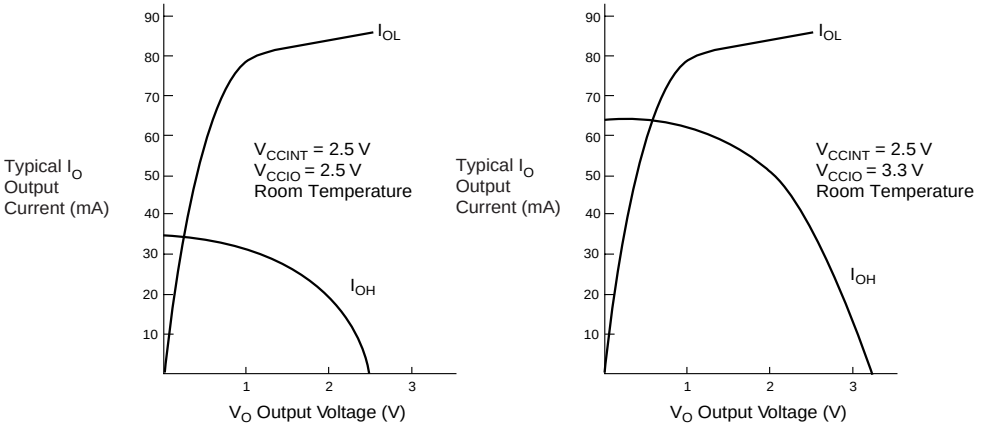
*Table 21. 2.5-V EPF10K30E, EPF10K50S, EPF10K100E, EPF10K130E & EPF10K200S Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3)*, *(4)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(3)*, *(4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(3)*, *(4)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_I$ | Input voltage | *(5)* | –0.5 | 5.75 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient temperature | For commercial use | 0 | 70 | ° C |
| | | For industrial use | –40 | 85 | ° C |
| $T_J$ | Operating temperature | For commercial use | 0 | 85 | ° C |
| | | For industrial use | –40 | 100 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

**Table 22. FLEX 10KE 2.5-V Device DC Operating Conditions** *Notes (6), (7)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 1.7, 0.5 × $V_{CCIO}$ *(8)* | | 5.75 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | 0.8, 0.3 × $V_{CCIO}$ *(8)* | V |
| $V_{OH}$ | 3.3-V high-level TTL output voltage | $I_{OH}$ = –8 mA DC, $V_{CCIO}$ = 3.00 V *(9)* | 2.4 | | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(9)* | $V_{CCIO}$ – 0.2 | | | V |
| | 3.3-V high-level PCI output voltage | $I_{OH}$ = –0.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(9)* | 0.9 × $V_{CCIO}$ | | | V |
| | 2.5-V high-level output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 2.30 V *(9)* | 2.1 | | | V |
| | | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.30 V *(9)* | 2.0 | | | V |
| | | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.30 V *(9)* | 1.7 | | | V |
| $V_{OL}$ | 3.3-V low-level TTL output voltage | $I_{OL}$ = 12 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | | | 0.2 | V |
| | 3.3-V low-level PCI output voltage | $I_{OL}$ = 1.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(10)* | | | 0.1 × $V_{CCIO}$ | V |
| | 2.5-V low-level output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | | | 0.2 | V |
| | | $I_{OL}$ = 1 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | | | 0.4 | V |
| | | $I_{OL}$ = 2 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | | | 0.7 | V |
| $I_I$ | Input pin leakage current | $V_I$ = $V_{CCIOmax}$ to 0 V *(11)* | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current | $V_O$ = $V_{CCIOmax}$ to 0 V *(11)* | –10 | | 10 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) | $V_I$ = ground, no load, no toggling inputs | | 5 | | mA |
| | | $V_I$ = ground, no load, no toggling inputs *(12)* | | 10 | | mA |
| $R_{CONF}$ | Value of I/O pin pull-up resistor before and during configuration | $V_{CCIO}$ = 3.0 V *(13)* | 20 | | 50 | k¾ |
| | | $V_{CCIO}$ = 2.3 V *(13)* | 30 | | 80 | k¾ |

***Figure 23. Output Drive Characteristics of FLEX 10KE Devices*** *Note (1)*




***Note:***
(1) These are transient (AC) currents.

## Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Device performance can be estimated by following the signal path from a source, through the interconnect, to the destination. For example, the registered performance between two LEs on the same row can be calculated by adding the following parameters:

- LE register clock-to-output delay ($t_{CO}$)
- Interconnect delay ($t_{SAMEROW}$)
- LE look-up table delay ($t_{LUT}$)
- LE register setup time ($t_{SU}$)

The routing delay depends on the placement of the source and destination LEs. A more complex registered path may involve multiple combinatorial LEs between the source and destination LEs.

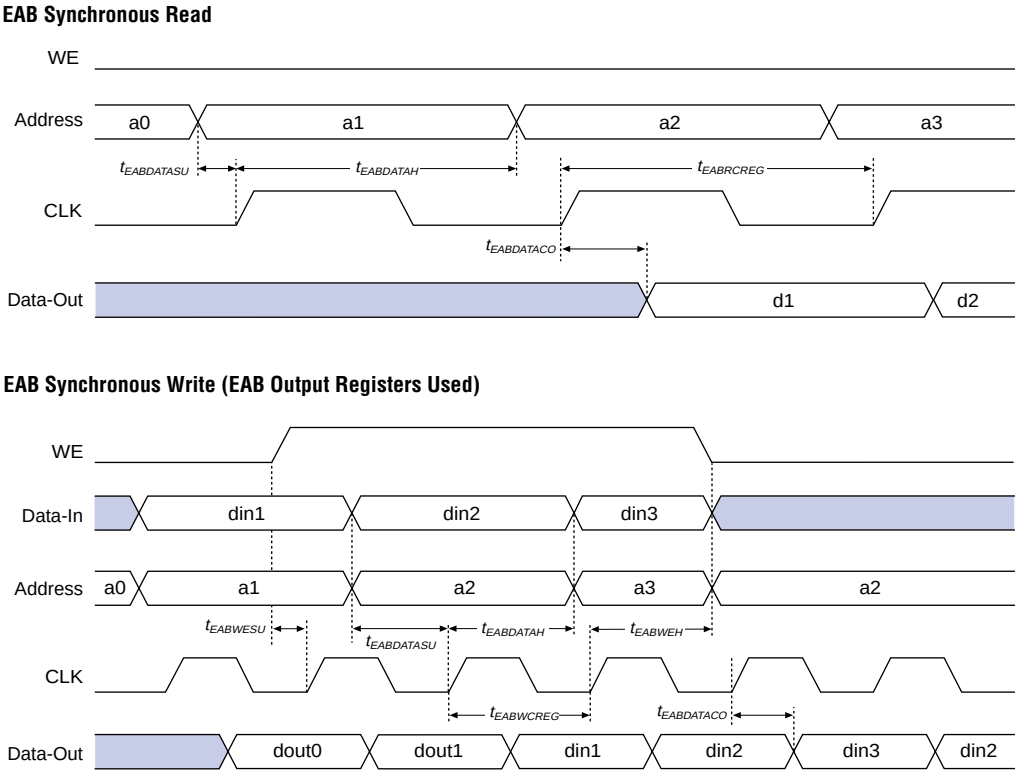
| *Table 27. EAB Timing Macroparameters* *Note (1), (6)* | | |
|---|---|---|
| **Symbol** | **Parameter** | **Conditions** |
| $t_{EABAA}$ | EAB address access delay | |
| $t_{EABRCCOMB}$ | EAB asynchronous read cycle time | |
| $t_{EABRCREG}$ | EAB synchronous read cycle time | |
| $t_{EABWP}$ | EAB write pulse width | |
| $t_{EABWCCOMB}$ | EAB asynchronous write cycle time | |
| $t_{EABWCREG}$ | EAB synchronous write cycle time | |
| $t_{EABDD}$ | EAB data-in to data-out valid delay | |
| $t_{EABDATACO}$ | EAB clock-to-output delay when using output registers | |
| $t_{EABDATASU}$ | EAB data/address setup time before clock when using input register | |
| $t_{EABDATAH}$ | EAB data/address hold time after clock when using input register | |
| $t_{EABWESU}$ | EAB WE setup time before clock when using input register | |
| $t_{EABWEH}$ | EAB WE hold time after clock when using input register | |
| $t_{EABWDSU}$ | EAB data setup time before falling edge of write pulse when not using input registers | |
| $t_{EABWDH}$ | EAB data hold time after falling edge of write pulse when not using input registers | |
| $t_{EABWASU}$ | EAB address setup time before rising edge of write pulse when not using input registers | |
| $t_{EABWAH}$ | EAB address hold time after falling edge of write pulse when not using input registers | |
| $t_{EABWO}$ | EAB write enable to data output valid delay | |

| *Table 30. External Bidirectional Timing Parameters* *Note (9)* | | |
|---|---|---|
| **Symbol** | **Parameter** | **Conditions** |
| $t_{INSUBIDIR}$ | Setup time for bi-directional pins with global clock at same-row or same-column LE register | |
| $t_{INHBIDIR}$ | Hold time for bidirectional pins with global clock at same-row or same-column LE register | |
| $t_{INH}$ | Hold time with global clock at IOE register | |
| $t_{OUTCOBIDIR}$ | Clock-to-output delay for bidirectional pins with global clock at IOE register | C1 = 35 pF |
| $t_{XZBIDIR}$ | Synchronous IOE output buffer disable delay | C1 = 35 pF |
| $t_{ZXBIDIR}$ | Synchronous IOE output buffer enable delay, slow slew rate= off | C1 = 35 pF |

***Notes to tables:***

(1) Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.
(2) Operating conditions: VCCIO = 3.3 V ±10% for commercial or industrial use.
(3) Operating conditions: VCCIO = 2.5 V ±5% for commercial or industrial use in EPF10K30E, EPF10K50S, EPF10K100E, EPF10K130E, and EPF10K200S devices.
(4) Operating conditions: VCCIO = 3.3 V.
(5) Because the RAM in the EAB is self-timed, this parameter can be ignored when the WE signal is registered.
(6) EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.
(7) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.
(8) Contact Altera Applications for test circuit specifications and test conditions.
(9) This timing parameter is sample-tested only.
(10) This parameter is measured with the measurement and test conditions, including load, specified in the PCI Local Bus Specification, revision 2.2.

*Figure 30. EAB Synchronous Timing Waveforms*




Tables 31 through 37 show EPF10K30E device internal and external timing parameters.

*Table 31. EPF10K30E Device LE Timing Microparameters (Part 1 of 2)* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{CLUT}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{RLUT}$ | | 0.6 | | 0.7 | | 1.0 | ns |
| $t_{PACKED}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{EN}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{CICO}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.5 | | 0.7 | ns |

*Table 37. EPF10K30E External Bidirectional Timing Parameters* *Notes (1), (2)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ (3) | 2.8 | | 3.9 | | 5.2 | | ns |
| $t_{INHBIDIR}$ (3) | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSUBIDIR}$ (4) | 3.8 | | 4.9 | | – | | ns |
| $t_{INHBIDIR}$ (4) | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCOBIDIR}$ (3) | 2.0 | 4.9 | 2.0 | 5.9 | 2.0 | 7.6 | ns |
| $t_{XZBIDIR}$ (3) | | 6.1 | | 7.5 | | 9.7 | ns |
| $t_{ZXBIDIR}$ (3) | | 6.1 | | 7.5 | | 9.7 | ns |
| $t_{OUTCOBIDIR}$ (4) | 0.5 | 3.9 | 0.5 | 4.9 | – | – | ns |
| $t_{XZBIDIR}$ (4) | | 5.1 | | 6.5 | | – | ns |
| $t_{ZXBIDIR}$ (4) | | 5.1 | | 6.5 | | – | ns |

***Notes to tables:***

(1) All timing parameters are described in Tables 24 through 30 in this data sheet.
(2) These parameters are specified by characterization.
(3) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 38 through 44 show EPF10K50E device internal and external timing parameters.

*Table 38. EPF10K50E Device LE Timing Microparameters (Part 1 of 2)* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 0.6 | | 0.9 | | 1.3 | ns |
| $t_{CLUT}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{RLUT}$ | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{PACKED}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{EN}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{CICO}$ | | 0.2 | | 0.2 | | 0.3 | ns |
| $t_{CGEN}$ | | 0.5 | | 0.5 | | 0.8 | ns |
| $t_{CGENR}$ | | 0.2 | | 0.2 | | 0.3 | ns |
| $t_{CASC}$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{C}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{CO}$ | | 0.7 | | 0.7 | | 0.9 | ns |
| $t_{COMB}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{SU}$ | 0.7 | | 0.7 | | 0.8 | | ns |

*Table 45. EPF10K100E Device LE Timing Microparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CGENR}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CASC}$ | | 0.6 | | 0.9 | | 1.2 | ns |
| $t_{C}$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{CO}$ | | 0.6 | | 0.8 | | 1.1 | ns |
| $t_{COMB}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{SU}$ | 0.4 | | 0.6 | | 0.7 | | ns |
| $t_{H}$ | 0.5 | | 0.7 | | 0.9 | | ns |
| $t_{PRE}$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{CLR}$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{CH}$ | 1.5 | | 2.0 | | 2.5 | | ns |
| $t_{CL}$ | 1.5 | | 2.0 | | 2.5 | | ns |

*Table 46. EPF10K100E Device IOE Timing Microparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 1.7 | | 2.0 | | 2.6 | ns |
| $t_{IOC}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{IOCO}$ | | 1.4 | | 1.6 | | 2.1 | ns |
| $t_{IOCOMB}$ | | 0.5 | | 0.7 | | 0.9 | ns |
| $t_{IOSU}$ | 0.8 | | 1.0 | | 1.3 | | ns |
| $t_{IOH}$ | 0.7 | | 0.9 | | 1.2 | | ns |
| $t_{IOCLR}$ | | 0.5 | | 0.7 | | 0.9 | ns |
| $t_{OD1}$ | | 3.0 | | 4.2 | | 5.6 | ns |
| $t_{OD2}$ | | 3.0 | | 4.2 | | 5.6 | ns |
| $t_{OD3}$ | | 4.0 | | 5.5 | | 7.3 | ns |
| $t_{XZ}$ | | 3.5 | | 4.6 | | 6.1 | ns |
| $t_{ZX1}$ | | 3.5 | | 4.6 | | 6.1 | ns |
| $t_{ZX2}$ | | 3.5 | | 4.6 | | 6.1 | ns |
| $t_{ZX3}$ | | 4.5 | | 5.9 | | 7.8 | ns |
| $t_{INREG}$ | | 2.0 | | 2.6 | | 3.5 | ns |
| $t_{IOFD}$ | | 0.5 | | 0.8 | | 1.2 | ns |
| $t_{INCOMB}$ | | 0.5 | | 0.8 | | 1.2 | ns |

**Table 47. EPF10K100E Device EAB Internal Microparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 1.5 | | 2.0 | | 2.6 | ns |
| $t_{EABDATA1}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABWE1}$ | | 1.5 | | 2.0 | | 2.6 | ns |
| $t_{EABWE2}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{EABRE1}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{EABRE2}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCLK}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCO}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{EABBYPASS}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{EABSU}$ | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{EABH}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{EABCLR}$ | 0.3 | | 0.4 | | 0.5 | | ns |
| $t_{AA}$ | | 4.0 | | 5.1 | | 6.6 | ns |
| $t_{WP}$ | 2.7 | | 3.5 | | 4.7 | | ns |
| $t_{RP}$ | 1.0 | | 1.3 | | 1.7 | | ns |
| $t_{WDSU}$ | 1.0 | | 1.3 | | 1.7 | | ns |
| $t_{WDH}$ | 0.2 | | 0.2 | | 0.3 | | ns |
| $t_{WASU}$ | 1.6 | | 2.1 | | 2.8 | | ns |
| $t_{WAH}$ | 1.6 | | 2.1 | | 2.8 | | ns |
| $t_{RASU}$ | 3.0 | | 3.9 | | 5.2 | | ns |
| $t_{RAH}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{WO}$ | | 1.5 | | 2.0 | | 2.6 | ns |
| $t_{DD}$ | | 1.5 | | 2.0 | | 2.6 | ns |
| $t_{EABOUT}$ | | 0.2 | | 0.3 | | 0.3 | ns |
| $t_{EABCH}$ | 1.5 | | 2.0 | | 2.5 | | ns |
| $t_{EABCL}$ | 2.7 | | 3.5 | | 4.7 | | ns |

**Table 48. EPF10K100E Device EAB Internal Timing Macroparameters** *(Part 1 of 2)* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABAA}$ | | 5.9 | | 7.6 | | 9.9 | ns |
| $t_{EABRCOMB}$ | 5.9 | | 7.6 | | 9.9 | | ns |
| $t_{EABRCREG}$ | 5.1 | | 6.5 | | 8.5 | | ns |
| $t_{EABWP}$ | 2.7 | | 3.5 | | 4.7 | | ns |

Tables 52 through 58 show EPF10K130E device internal and external timing parameters.

**Table 52. EPF10K130E Device LE Timing Microparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 0.6 | | 0.9 | | 1.3 | ns |
| $t_{CLUT}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{RLUT}$ | | 0.7 | | 0.9 | | 0.2 | ns |
| $t_{PACKED}$ | | 0.3 | | 0.5 | | 0.6 | ns |
| $t_{EN}$ | | 0.2 | | 0.3 | | 0.4 | ns |
| $t_{CICO}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.6 | | 0.8 | ns |
| $t_{CGENR}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CASC}$ | | 0.6 | | 0.9 | | 1.2 | ns |
| $t_{C}$ | | 0.3 | | 0.5 | | 0.6 | ns |
| $t_{CO}$ | | 0.5 | | 0.7 | | 0.8 | ns |
| $t_{COMB}$ | | 0.3 | | 0.5 | | 0.6 | ns |
| $t_{SU}$ | 0.5 | | 0.7 | | 0.8 | | ns |
| $t_{H}$ | 0.6 | | 0.7 | | 1.0 | | ns |
| $t_{PRE}$ | | 0.9 | | 1.2 | | 1.6 | ns |
| $t_{CLR}$ | | 0.9 | | 1.2 | | 1.6 | ns |
| $t_{CH}$ | 1.5 | | 1.5 | | 2.5 | | ns |
| $t_{CL}$ | 1.5 | | 1.5 | | 2.5 | | ns |

**Table 53. EPF10K130E Device IOE Timing Microparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 1.3 | | 1.5 | | 2.0 | ns |
| $t_{IOC}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{IOCO}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{IOCOMB}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{IOSU}$ | 1.0 | | 1.2 | | 1.6 | | ns |
| $t_{IOH}$ | 0.9 | | 0.9 | | 1.4 | | ns |
| $t_{IOCLR}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{OD1}$ | | 2.8 | | 4.1 | | 5.5 | ns |
| $t_{OD2}$ | | 2.8 | | 4.1 | | 5.5 | ns |

**Table 59. EPF10K200E Device LE Timing Microparameters** *(Part 2 of 2)* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_H$ | 0.9 | | 1.1 | | 1.5 | | ns |
| $t_{PRE}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{CLR}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 3.0 | | ns |

**Table 60. EPF10K200E Device IOE Timing Microparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 1.6 | | 1.9 | | 2.6 | ns |
| $t_{IOC}$ | | 0.3 | | 0.3 | | 0.5 | ns |
| $t_{IOCO}$ | | 1.6 | | 1.9 | | 2.6 | ns |
| $t_{IOCOMB}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{IOSU}$ | 0.8 | | 0.9 | | 1.2 | | ns |
| $t_{IOH}$ | 0.7 | | 0.8 | | 1.1 | | ns |
| $t_{IOCLR}$ | | 0.2 | | 0.2 | | 0.3 | ns |
| $t_{OD1}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{OD2}$ | | 0.1 | | 0.2 | | 0.7 | ns |
| $t_{OD3}$ | | 2.5 | | 3.0 | | 3.9 | ns |
| $t_{XZ}$ | | 4.4 | | 5.3 | | 7.1 | ns |
| $t_{ZX1}$ | | 4.4 | | 5.3 | | 7.1 | ns |
| $t_{ZX2}$ | | 3.9 | | 4.8 | | 6.9 | ns |
| $t_{ZX3}$ | | 6.3 | | 7.6 | | 10.1 | ns |
| $t_{INREG}$ | | 4.8 | | 5.7 | | 7.7 | ns |
| $t_{IOFD}$ | | 1.5 | | 1.8 | | 2.4 | ns |
| $t_{INCOMB}$ | | 1.5 | | 1.8 | | 2.4 | ns |

**Table 61. EPF10K200E Device EAB Internal Microparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 2.0 | | 2.4 | | 3.2 | ns |
| $t_{EABDATA1}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{EABWE1}$ | | 1.4 | | 1.7 | | 2.3 | ns |
| $t_{EABWE2}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABRE1}$ | | 0 | | 0 | | 0 | ns |
| $t_{EABRE2}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{EABCLK}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCO}$ | | 0.8 | | 0.9 | | 1.2 | ns |
| $t_{EABBYPASS}$ | | 0.0 | | 0.1 | | 0.1 | ns |
| $t_{EABSU}$ | 0.9 | | 1.1 | | 1.5 | | ns |
| $t_{EABH}$ | 0.4 | | 0.5 | | 0.6 | | ns |
| $t_{EABCLR}$ | 0.8 | | 0.9 | | 1.2 | | ns |
| $t_{AA}$ | | 3.1 | | 3.7 | | 4.9 | ns |
| $t_{WP}$ | 3.3 | | 4.0 | | 5.3 | | ns |
| $t_{RP}$ | 0.9 | | 1.1 | | 1.5 | | ns |
| $t_{WDSU}$ | 0.9 | | 1.1 | | 1.5 | | ns |
| $t_{WDH}$ | 0.1 | | 0.1 | | 0.1 | | ns |
| $t_{WASU}$ | 1.3 | | 1.6 | | 2.1 | | ns |
| $t_{WAH}$ | 2.1 | | 2.5 | | 3.3 | | ns |
| $t_{RASU}$ | 2.2 | | 2.6 | | 3.5 | | ns |
| $t_{RAH}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{WO}$ | | 2.0 | | 2.4 | | 3.2 | ns |
| $t_{DD}$ | | 2.0 | | 2.4 | | 3.2 | ns |
| $t_{EABOUT}$ | | 0.0 | | 0.1 | | 0.1 | ns |
| $t_{EABCH}$ | 1.5 | | 2.0 | | 2.5 | | ns |
| $t_{EABCL}$ | 3.3 | | 4.0 | | 5.3 | | ns |

**Table 62. EPF10K200E Device EAB Internal Timing Macroparameters (Part 1 of 2)** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABAA}$ | | 5.1 | | 6.4 | | 8.4 | ns |
| $t_{EABRCOMB}$ | 5.1 | | 6.4 | | 8.4 | | ns |
| $t_{EABRCREG}$ | 4.8 | | 5.7 | | 7.6 | | ns |
| $t_{EABWP}$ | 3.3 | | 4.0 | | 5.3 | | ns |

*Table 68. EPF10K50S Device EAB Internal Microparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 1.7 | | 2.4 | | 3.2 | ns |
| $t_{EABDATA2}$ | | 0.4 | | 0.6 | | 0.8 | ns |
| $t_{EABWE1}$ | | 1.0 | | 1.4 | | 1.9 | ns |
| $t_{EABWE2}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABRE1}$ | | 0.0 | | 0.0 | | 0.0 | |
| $t_{EABRE2}$ | | 0.4 | | 0.6 | | 0.8 | |
| $t_{EABCLK}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCO}$ | | 0.8 | | 1.1 | | 1.5 | ns |
| $t_{EABBYPASS}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABSU}$ | 0.7 | | 1.0 | | 1.3 | | ns |
| $t_{EABH}$ | 0.4 | | 0.6 | | 0.8 | | ns |
| $t_{EABCLR}$ | 0.8 | | 1.1 | | 1.5 | | |
| $t_{AA}$ | | 2.0 | | 2.8 | | 3.8 | ns |
| $t_{WP}$ | 2.0 | | 2.8 | | 3.8 | | ns |
| $t_{RP}$ | 1.0 | | 1.4 | | 1.9 | | |
| $t_{WDSU}$ | 0.5 | | 0.7 | | 0.9 | | ns |
| $t_{WDH}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{WASU}$ | 1.0 | | 1.4 | | 1.9 | | ns |
| $t_{WAH}$ | 1.5 | | 2.1 | | 2.9 | | ns |
| $t_{RASU}$ | 1.5 | | 2.1 | | 2.8 | | |
| $t_{RAH}$ | 0.1 | | 0.1 | | 0.2 | | |
| $t_{WO}$ | | 2.1 | | 2.9 | | 4.0 | ns |
| $t_{DD}$ | | 2.1 | | 2.9 | | 4.0 | ns |
| $t_{EABOUT}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCH}$ | 1.5 | | 2.0 | | 2.5 | | ns |
| $t_{EABCL}$ | 1.5 | | 2.0 | | 2.5 | | ns |

Additionally, the Altera software offers several features that help plan for future device migration by preventing the use of conflicting I/O pins.

*Table 81. I/O Counts for FLEX 10KA & FLEX 10KE Devices*

| FLEX 10KA | | FLEX 10KE | |
|---|---|---|---|
| **Device** | **I/O Count** | **Device** | **I/O Count** |
| EPF10K30AF256 | 191 | EPF10K30EF256 | 176 |
| EPF10K30AF484 | 246 | EPF10K30EF484 | 220 |
| EPF10K50VB356 | 274 | EPF10K50SB356 | 220 |
| EPF10K50VF484 | 291 | EPF10K50EF484 | 254 |
| EPF10K50VF484 | 291 | EPF10K50SF484 | 254 |
| EPF10K100AF484 | 369 | EPF10K100EF484 | 338 |

## Configuration Schemes

The configuration data for a FLEX 10KE device can be loaded with one of five configuration schemes (see Table 82), chosen on the basis of the target application. An EPC1, EPC2, or EPC16 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of a FLEX 10KE device, allowing automatic configuration on system power-up.

Multiple FLEX 10KE devices can be configured in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device. Additional FLEX 10K, FLEX 10KA, FLEX 10KE, and FLEX 6000 devices can be configured in the same serial chain.

*Table 82. Data Sources for FLEX 10KE Configuration*

| Configuration Scheme | Data Source |
|---|---|
| Configuration device | EPC1, EPC2, or EPC16 configuration device |
| Passive serial (PS) | BitBlaster, ByteBlasterMV, or MasterBlaster download cables, or serial data source |
| Passive parallel asynchronous (PPA) | Parallel data source |
| Passive parallel synchronous (PPS) | Parallel data source |
| JTAG | BitBlaster or ByteBlasterMV download cables, or microprocessor with a Jam STAPL file or JBC file |