Intel - EPF10K200SRC240-3B Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	1248
Number of Logic Elements/Cells	9984
Total RAM Bits	98304
Number of I/O	182
Number of Gates	513000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-RQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k200src240-3b

Table 2. FLEX 10KE Device Features

Feature	EPF10K100E *(2)*	EPF10K130E	EPF10K200E EPF10K200S
Typical gates *(1)*	100,000	130,000	200,000
Maximum system gates	257,000	342,000	513,000
Logic elements (LEs)	4,992	6,656	9,984
EABs	12	16	24
Total RAM bits	49,152	65,536	98,304
Maximum user I/O pins	338	413	470

Note to tables:

(1) The embedded IEEE Std. 1149.1 JTAG circuitry adds up to 31,250 gates in addition to the listed typical or maximum system gates.

(2) New EPF10K100B designs should use EPF10K100E devices.

…and More Features

  - Fabricated on an advanced process and operate with a 2.5-V internal supply voltage
  - In-circuit reconfigurability (ICR) via external configuration devices, intelligent controller, or JTAG port
  - ClockLock™ and ClockBoost™ options for reduced clock delay/skew and clock multiplication
  - Built-in low-skew clock distribution trees
  - 100% functional testing of all devices; test vectors or scan chains are not required
  - Pull-up on I/O pins before and during configuration
- Flexible interconnect
  - FastTrack® Interconnect continuous routing structure for fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Tri-state emulation that implements internal tri-state buses
  - Up to six global clock signals and four global clear signals
- Powerful I/O pins
  - Individual tri-state output enable control for each pin
  - Open-drain option on each I/O pin
  - Programmable output slew-rate control to reduce switching noise
  - Clamp to V_{CCIO} user-selectable on a pin-by-pin basis
  - Supports hot-socketing

- Software design support and automatic place-and-route provided by Altera's development systems for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800
- Flexible package options
  - Available in a variety of packages with 144 to 672 pins, including the innovative FineLine BGA™ packages (see Tables 3 and 4)
  - SameFrame™ pin-out compatibility between FLEX 10KA and FLEX 10KE devices across a range of device densities and pin counts
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), DesignWare components, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, VeriBest, and Viewlogic

Table 3. FLEX 10KE Package Options & I/O Pin Count *Notes (1), (2)*

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP RQFP	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA	599-Pin PGA	600-Pin BGA	672-Pin FineLine BGA
EPF10K30E	102	147		176		220			220 *(3)*
EPF10K50E	102	147	189	191		254			254 *(3)*
EPF10K50S	102	147	189	191	220	254			254 *(3)*
EPF10K100E		147	189	191	274	338			338 *(3)*
EPF10K130E			186		274	369		424	413
EPF10K200E							470	470	470
EPF10K200S			182		274	369	470	470	470

Notes:

(1) FLEX 10KE device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), pin-grid array (PGA), and ball-grid array (BGA) packages.

(2) Devices in the same package are pin-compatible, although some devices have more I/O pins than others. When planning device migration, use the I/O pins that are common to all devices.

(3) This option is supported with a 484-pin FineLine BGA package. By using SameFrame pin migration, all FineLine BGA packages are pin-compatible. For example, a board can be designed to support 256-pin, 484-pin, and 672-pin FineLine BGA packages. The Altera software automatically avoids conflicting pins when future migration is set.

Table 4. FLEX 10KE Package Sizes

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP RQFP	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA	599-Pin PGA	600-Pin BGA	672-Pin FineLine BGA
Pitch (mm)	0.50	0.50	0.50	1.0	1.27	1.0	–	1.27	1.0
Area (mm^2)	484	936	1,197	289	1,225	529	3,904	2,025	729
Length × width (mm × mm)	22 × 22	30.6 × 30.6	34.6 × 34.6	17 × 17	35 × 35	23 × 23	62.5 × 62.5	45 × 45	27 × 27

General Description

Altera FLEX 10KE devices are enhanced versions of FLEX 10K devices. Based on reconfigurable CMOS SRAM elements, the FLEX architecture incorporates all features necessary to implement common gate array megafunctions. With up to 200,000 typical gates, FLEX 10KE devices provide the density, speed, and features to integrate entire systems, including multiple 32-bit buses, into a single device.

The ability to reconfigure FLEX 10KE devices enables 100% testing prior to shipment and allows the designer to focus on simulation and design verification. FLEX 10KE reconfigurability eliminates inventory management for gate array designs and generation of test vectors for fault coverage.

Table 5 shows FLEX 10KE performance for some common designs. All performance values were obtained with Synopsys DesignWare or LPM functions. Special design techniques are not required to implement the applications; the designer simply infers or instantiates a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

Similar to the FLEX 10KE architecture, embedded gate arrays are the fastest-growing segment of the gate array market. As with standard gate arrays, embedded gate arrays implement general logic in a conventional "sea-of-gates" architecture. Additionally, embedded gate arrays have dedicated die areas for implementing large, specialized functions. By embedding functions in silicon, embedded gate arrays reduce die area and increase speed when compared to standard gate arrays. While embedded megafunctions typically cannot be customized, FLEX 10KE devices are programmable, providing the designer with full control over embedded megafunctions and general logic, while facilitating iterative design changes during debugging.

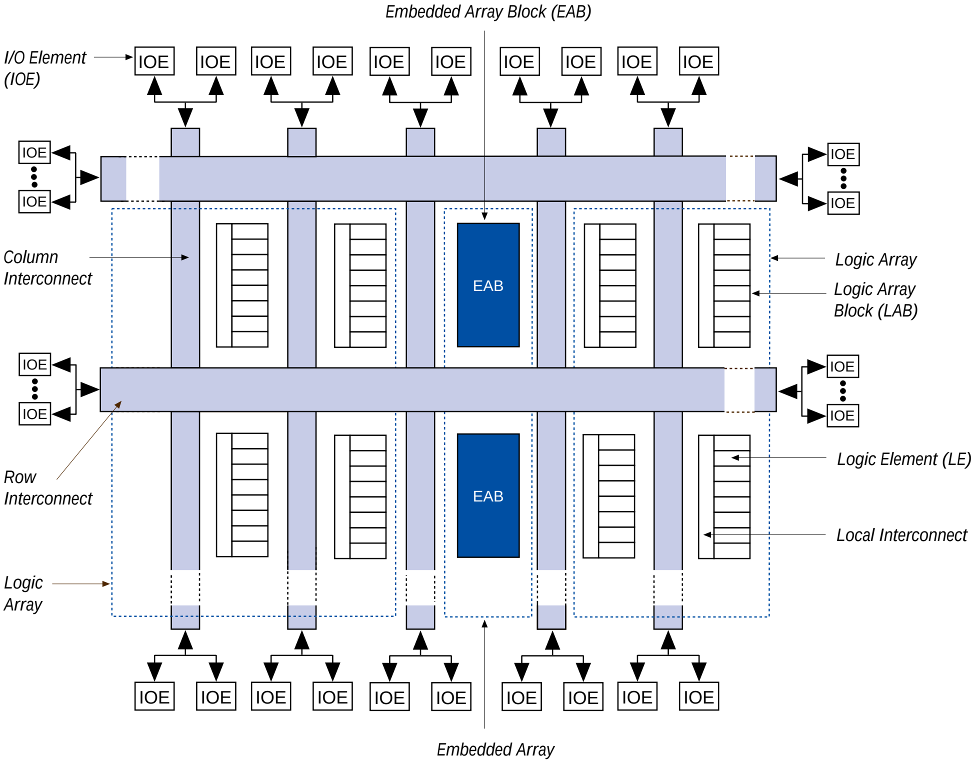
Each FLEX 10KE device contains an embedded array and a logic array. The embedded array is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), wide data-path manipulation, microcontroller applications, and data-transformation functions. The logic array performs the same function as the sea-of-gates in the gate array and is used to implement general logic such as counters, adders, state machines, and multiplexers. The combination of embedded and logic arrays provides the high performance and high density of embedded gate arrays, enabling designers to implement an entire system on a single device.

FLEX 10KE devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers the EPC1, EPC2, and EPC16 configuration devices, which configure FLEX 10KE devices via a serial data stream. Configuration data can also be downloaded from system RAM or via the Altera BitBlaster™, ByteBlasterMV™, or MasterBlaster download cables. After a FLEX 10KE device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 85 ms, real-time changes can be made during system operation.

FLEX 10KE devices contain an interface that permits microprocessors to configure FLEX 10KE devices serially or in-parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat a FLEX 10KE device as memory and configure it by writing to a virtual memory location, making it easy to reconfigure the device.

Figure 1 shows a block diagram of the FLEX 10KE architecture. Each group of LEs is combined into an LAB; groups of LABs are arranged into rows and columns. Each row also contains a single EAB. The LABs and EABs are interconnected by the FastTrack Interconnect routing structure. IOEs are located at the end of each row and column of the FastTrack Interconnect routing structure.

Figure 1. FLEX 10KE Device Block Diagram



FLEX 10KE devices provide six dedicated inputs that drive the flipflops' control inputs and ensure the efficient distribution of high-speed, low-skew (less than 1.5 ns) control signals. These signals use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect routing structure. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device.

EABs provide flexible options for driving and controlling clock signals. Different clocks and clock enables can be used for reading and writing to the EAB. Registers can be independently inserted on the data input, EAB output, write address, write enable signals, read address, and read enable signals. The global signals and the EAB local interconnect can drive write enable, read enable, and clock enable signals. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control write enable, read enable, clear, clock, and clock enable signals.

An EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs (see Figures 2 and 4). The column interconnect, which is adjacent to the EAB, has twice as many channels as other columns in the device.

Logic Array Block

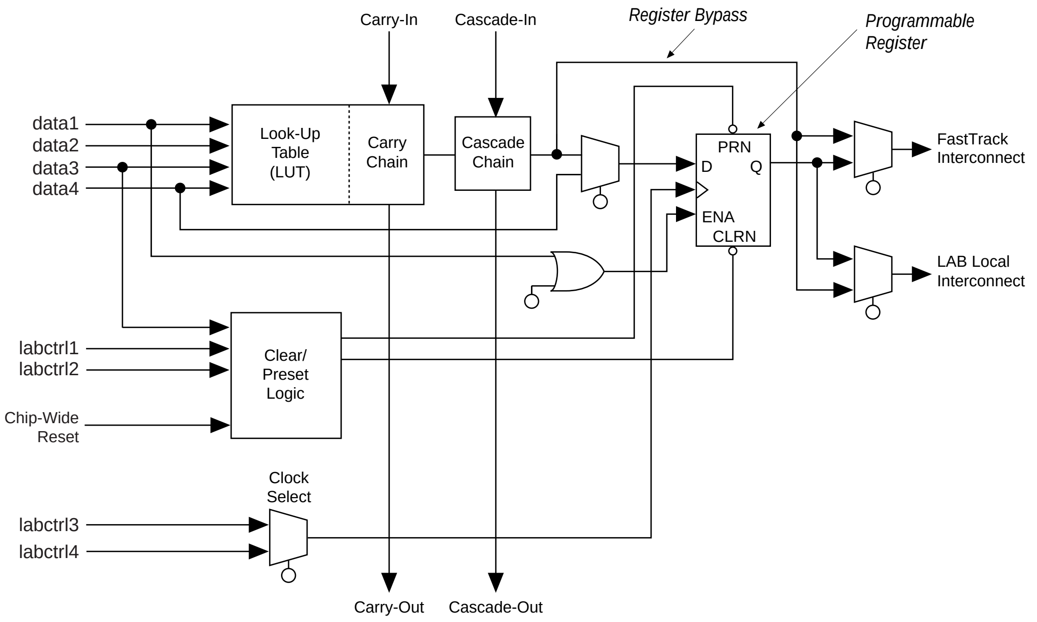
An LAB consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure to the FLEX 10KE architecture, facilitating efficient routing with optimum device utilization and high performance (see Figure 7).

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks, the other two can be used for clear / preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I / O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I / O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LE in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated from LE outputs.

Logic Element

The LE, the smallest unit of logic in the FLEX 10KE architecture, has a compact size that provides efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous clock enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect routing structure (see Figure 8).

Figure 8. FLEX 10KE Logic Element



SameFrame Pin-Outs

FLEX 10KE devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density / package combinations. For example, a single board layout can support a range of devices from an EPF10K30E device in a 256-pin FineLine BGA package to an EPF10K200S device in a 672-pin FineLine BGA package.

The Altera software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software generates pin-outs describing how to lay out a board to take advantage of this migration (see Figure 18).

Figure 18. SameFrame Pin-Out Example

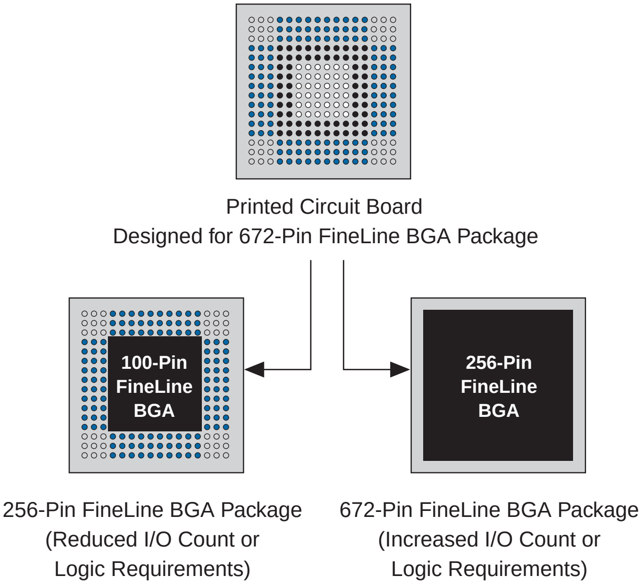


Figure 20 shows the timing requirements for the JTAG signals.

Figure 20. FLEX 10KE JTAG Waveforms

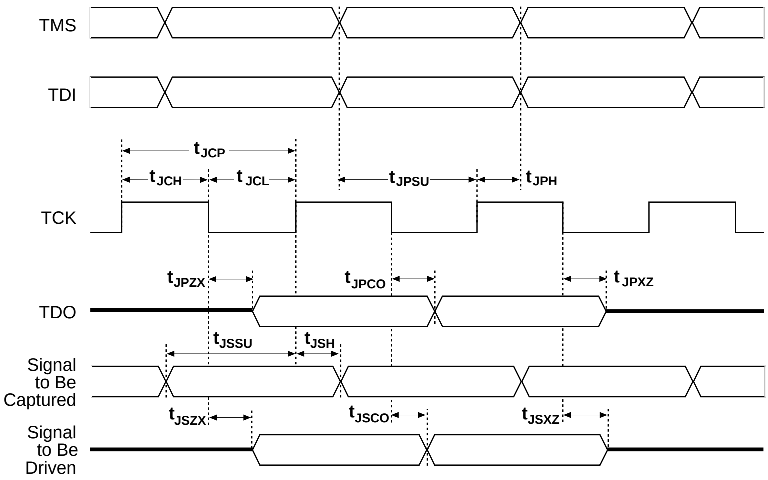


Table 18 shows the timing parameters and values for FLEX 10KE devices.

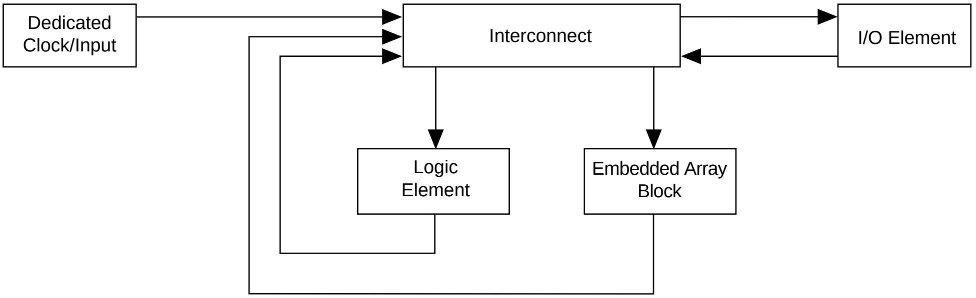
Table 18. FLEX 10KE JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

Timing simulation and delay prediction are available with the Altera Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

Figure 24 shows the overall timing model, which maps the possible paths to and from the various elements of the FLEX 10KE device.

Figure 24. FLEX 10KE Device Timing Model



Figures 25 through 28 show the delays that correspond to various paths and functions within the LE, IOE, EAB, and bidirectional timing models.

Table 31. EPF10K30E Device LE Timing Microparameters (Part 2 of 2) Note (1)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{CGENR}		0.1		0.1		0.2	ns
t_{CASC}		0.6		0.8		1.0	ns
t_C		0.0		0.0		0.0	ns
t_{CO}		0.3		0.4		0.5	ns
t_{COMB}		0.4		0.4		0.6	ns
t_{SU}	0.4		0.6		0.6		ns
t_H	0.7		1.0		1.3		ns
t_{PRE}		0.8		0.9		1.2	ns
t_{CLR}		0.8		0.9		1.2	ns
t_{CH}	2.0		2.5		2.5		ns
t_{CL}	2.0		2.5		2.5		ns

Table 32. EPF10K30E Device IOE Timing Microparameters Note (1)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{IOD}		2.4		2.8		3.8	ns
t_{IOC}		0.3		0.4		0.5	ns
t_{IOCO}		1.0		1.1		1.6	ns
t_{IOCOMB}		0.0		0.0		0.0	ns
t_{IOSU}	1.2		1.4		1.9		ns
t_{IOH}	0.3		0.4		0.5		ns
t_{IOCLR}		1.0		1.1		1.6	ns
t_{OD1}		1.9		2.3		3.0	ns
t_{OD2}		1.4		1.8		2.5	ns
t_{OD3}		4.4		5.2		7.0	ns
t_{XZ}		2.7		3.1		4.3	ns
t_{ZX1}		2.7		3.1		4.3	ns
t_{ZX2}		2.2		2.6		3.8	ns
t_{ZX3}		5.2		6.0		8.3	ns
t_{INREG}		3.4		4.1		5.5	ns
t_{IOFD}		0.8		1.3		2.4	ns
t_{INCOMB}		0.8		1.3		2.4	ns

Table 37. EPF10K30E External Bidirectional Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (3)	2.8		3.9		5.2		ns
$t_{INHBIDIR}$ (3)	0.0		0.0		0.0		ns
$t_{INSUBIDIR}$ (4)	3.8		4.9		–		ns
$t_{INHBIDIR}$ (4)	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ (3)	2.0	4.9	2.0	5.9	2.0	7.6	ns
$t_{XZBIDIR}$ (3)		6.1		7.5		9.7	ns
$t_{ZXBIDIR}$ (3)		6.1		7.5		9.7	ns
$t_{OUTCOBIDIR}$ (4)	0.5	3.9	0.5	4.9	–	–	ns
$t_{XZBIDIR}$ (4)		5.1		6.5		–	ns
$t_{ZXBIDIR}$ (4)		5.1		6.5		–	ns

Notes to tables:

(1) All timing parameters are described in Tables 24 through 30 in this data sheet.
(2) These parameters are specified by characterization.
(3) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 38 through 44 show EPF10K50E device internal and external timing parameters.

Table 38. EPF10K50E Device LE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.6		0.9		1.3	ns
t_{CLUT}		0.5		0.6		0.8	ns
t_{RLUT}		0.7		0.8		1.1	ns
t_{PACKED}		0.4		0.5		0.6	ns
t_{EN}		0.6		0.7		0.9	ns
t_{CICO}		0.2		0.2		0.3	ns
t_{CGEN}		0.5		0.5		0.8	ns
t_{CGENR}		0.2		0.2		0.3	ns
t_{CASC}		0.8		1.0		1.4	ns
t_{C}		0.5		0.6		0.8	ns
t_{CO}		0.7		0.7		0.9	ns
t_{COMB}		0.5		0.6		0.8	ns
t_{SU}	0.7		0.7		0.8		ns

Table 47. EPF10K100E Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.5		2.0		2.6	ns
$t_{EABDATA1}$		0.0		0.0		0.0	ns
t_{EABWE1}		1.5		2.0		2.6	ns
t_{EABWE2}		0.3		0.4		0.5	ns
t_{EABRE1}		0.3		0.4		0.5	ns
t_{EABRE2}		0.0		0.0		0.0	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.3		0.4		0.5	ns
$t_{EABBYPASS}$		0.1		0.1		0.2	ns
t_{EABSU}	0.8		1.0		1.4		ns
t_{EABH}	0.1		0.1		0.2		ns
t_{EABCLR}	0.3		0.4		0.5		ns
t_{AA}		4.0		5.1		6.6	ns
t_{WP}	2.7		3.5		4.7		ns
t_{RP}	1.0		1.3		1.7		ns
t_{WDSU}	1.0		1.3		1.7		ns
t_{WDH}	0.2		0.2		0.3		ns
t_{WASU}	1.6		2.1		2.8		ns
t_{WAH}	1.6		2.1		2.8		ns
t_{RASU}	3.0		3.9		5.2		ns
t_{RAH}	0.1		0.1		0.2		ns
t_{WO}		1.5		2.0		2.6	ns
t_{DD}		1.5		2.0		2.6	ns
t_{EABOUT}		0.2		0.3		0.3	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	2.7		3.5		4.7		ns

Table 48. EPF10K100E Device EAB Internal Timing Macroparameters *(Part 1 of 2)* *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		5.9		7.6		9.9	ns
$t_{EABRCOMB}$	5.9		7.6		9.9		ns
$t_{EABRCREG}$	5.1		6.5		8.5		ns
t_{EABWP}	2.7		3.5		4.7		ns

Table 48. EPF10K100E Device EAB Internal Timing Macroparameters *(Part 2 of 2)* *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABWCOMB}$	5.9		7.7		10.3		ns
$t_{EABWCREG}$	5.4		7.0		9.4		ns
t_{EABDD}		3.4		4.5		5.9	ns
$t_{EABDATACO}$		0.5		0.7		0.8	ns
$t_{EABDATASU}$	0.8		1.0		1.4		ns
$t_{EABDATAH}$	0.1		0.1		0.2		ns
$t_{EABWESU}$	1.1		1.4		1.9		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.0		1.3		1.7		ns
t_{EABWDH}	0.2		0.2		0.3		ns
$t_{EABWASU}$	4.1		5.2		6.8		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		3.4		4.5		5.9	ns

Table 49. EPF10K100E Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		3.1		3.6		4.4	ns
t_{DIN2LE}		0.3		0.4		0.5	ns
$t_{DIN2DATA}$		1.6		1.8		2.0	ns
$t_{DCLK2IOE}$		0.8		1.1		1.4	ns
$t_{DCLK2LE}$		0.3		0.4		0.5	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		1.5		2.5		3.4	ns
$t_{SAMECOLUMN}$		0.4		1.0		1.6	ns
$t_{DIFFROW}$		1.9		3.5		5.0	ns
$t_{TWOROWS}$		3.4		6.0		8.4	ns
$t_{LEPERIPH}$		4.3		5.4		6.5	ns
$t_{LABCARRY}$		0.5		0.7		0.9	ns
$t_{LABCASC}$		0.8		1.0		1.4	ns

Tables 52 through 58 show EPF10K130E device internal and external timing parameters.

Table 52. EPF10K130E Device LE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.6		0.9		1.3	ns
t_{CLUT}		0.6		0.8		1.0	ns
t_{RLUT}		0.7		0.9		0.2	ns
t_{PACKED}		0.3		0.5		0.6	ns
t_{EN}		0.2		0.3		0.4	ns
t_{CICO}		0.1		0.1		0.2	ns
t_{CGEN}		0.4		0.6		0.8	ns
t_{CGENR}		0.1		0.1		0.2	ns
t_{CASC}		0.6		0.9		1.2	ns
t_{C}		0.3		0.5		0.6	ns
t_{CO}		0.5		0.7		0.8	ns
t_{COMB}		0.3		0.5		0.6	ns
t_{SU}	0.5		0.7		0.8		ns
t_{H}	0.6		0.7		1.0		ns
t_{PRE}		0.9		1.2		1.6	ns
t_{CLR}		0.9		1.2		1.6	ns
t_{CH}	1.5		1.5		2.5		ns
t_{CL}	1.5		1.5		2.5		ns

Table 53. EPF10K130E Device IOE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{IOD}		1.3		1.5		2.0	ns
t_{IOC}		0.0		0.0		0.0	ns
t_{IOCO}		0.6		0.8		1.0	ns
t_{IOCOMB}		0.6		0.8		1.0	ns
t_{IOSU}	1.0		1.2		1.6		ns
t_{IOH}	0.9		0.9		1.4		ns
t_{IOCLR}		0.6		0.8		1.0	ns
t_{OD1}		2.8		4.1		5.5	ns
t_{OD2}		2.8		4.1		5.5	ns

Table 54. EPF10K130E Device EAB Internal Microparameters *(Part 2 of 2)* *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DD}		1.5		2.0		2.6	ns
t_{EABOUT}		0.2		0.3		0.3	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	2.7		3.5		4.7		ns

Table 55. EPF10K130E Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		5.9		7.5		9.9	ns
$t_{EABRCOMB}$	5.9		7.5		9.9		ns
$t_{EABRCREG}$	5.1		6.4		8.5		ns
t_{EABWP}	2.7		3.5		4.7		ns
$t_{EABWCOMB}$	5.9		7.7		10.3		ns
$t_{EABWCREG}$	5.4		7.0		9.4		ns
t_{EABDD}		3.4		4.5		5.9	ns
$t_{EABDATACO}$		0.5		0.7		0.8	ns
$t_{EABDATASU}$	0.8		1.0		1.4		ns
$t_{EABDATAH}$	0.1		0.1		0.2		ns
$t_{EABWESU}$	1.1		1.4		1.9		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.0		1.3		1.7		ns
t_{EABWDH}	0.2		0.2		0.3		ns
$t_{EABWASU}$	4.1		5.1		6.8		ns
t_{EABWAH}	0.0		0.0		0.0		ns
t_{EABWO}		3.4		4.5		5.9	ns

Table 58. EPF10K130E External Bidirectional Timing Parameters Notes (1), (2)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ (3)	2.2		2.4		3.2		ns
$t_{INHBIDIR}$ (3)	0.0		0.0		0.0		ns
$t_{INSUBIDIR}$ (4)	2.8		3.0		–		ns
$t_{INHBIDIR}$ (4)	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ (3)	2.0	5.0	2.0	7.0	2.0	9.2	ns
$t_{XZBIDIR}$ (3)		5.6		8.1		10.8	ns
$t_{ZXBIDIR}$ (3)		5.6		8.1		10.8	ns
$t_{OUTCOBIDIR}$ (4)	0.5	4.0	0.5	6.0	–	–	ns
$t_{XZBIDIR}$ (4)		4.6		7.1		–	ns
$t_{ZXBIDIR}$ (4)		4.6		7.1		–	ns

Notes to tables:

(1) All timing parameters are described in Tables 24 through 30 in this data sheet.
(2) These parameters are specified by characterization.
(3) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 59 through 65 show EPF10K200E device internal and external timing parameters.

Table 59. EPF10K200E Device LE Timing Microparameters *(Part 1 of 2)* Note (1)

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.7		0.8		1.2	ns
t_{CLUT}		0.4		0.5		0.6	ns
t_{RLUT}		0.6		0.7		0.9	ns
t_{PACKED}		0.3		0.5		0.7	ns
t_{EN}		0.4		0.5		0.6	ns
t_{CICO}		0.2		0.2		0.3	ns
t_{CGEN}		0.4		0.4		0.6	ns
t_{CGENR}		0.2		0.2		0.3	ns
t_{CASC}		0.7		0.8		1.2	ns
t_{C}		0.5		0.6		0.8	ns
t_{CO}		0.5		0.6		0.8	ns
t_{COMB}		0.4		0.6		0.8	ns
t_{SU}	0.4		0.6		0.7		ns

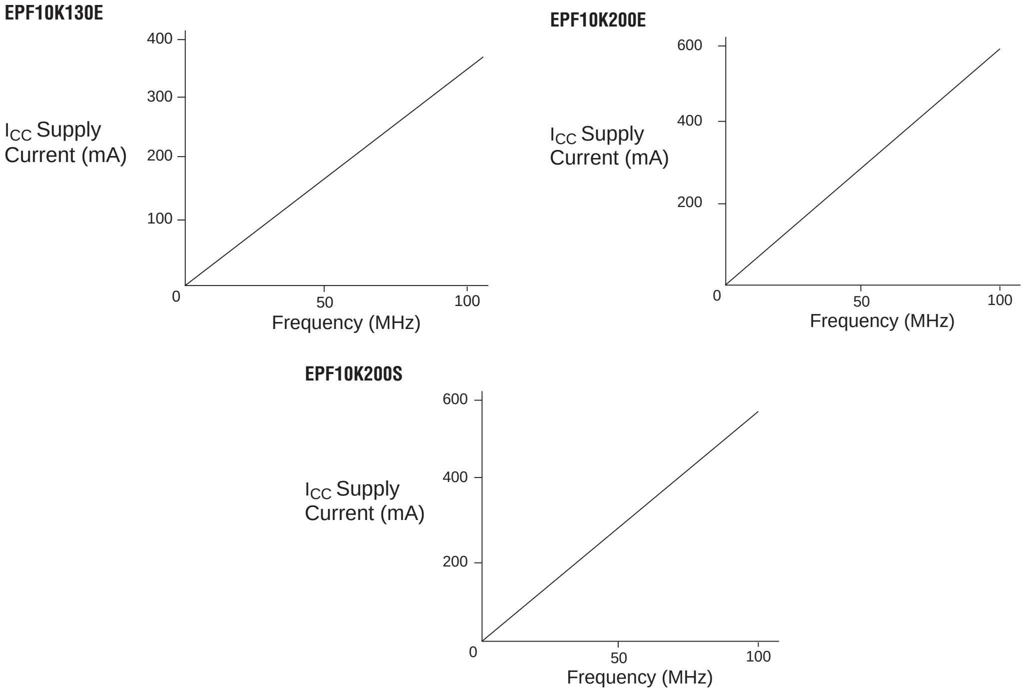
Table 61. EPF10K200E Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		2.0		2.4		3.2	ns
$t_{EABDATA1}$		0.4		0.5		0.6	ns
t_{EABWE1}		1.4		1.7		2.3	ns
t_{EABWE2}		0.0		0.0		0.0	ns
t_{EABRE1}		0		0		0	ns
t_{EABRE2}		0.4		0.5		0.6	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.8		0.9		1.2	ns
$t_{EABBYPASS}$		0.0		0.1		0.1	ns
t_{EABSU}	0.9		1.1		1.5		ns
t_{EABH}	0.4		0.5		0.6		ns
t_{EABCLR}	0.8		0.9		1.2		ns
t_{AA}		3.1		3.7		4.9	ns
t_{WP}	3.3		4.0		5.3		ns
t_{RP}	0.9		1.1		1.5		ns
t_{WDSU}	0.9		1.1		1.5		ns
t_{WDH}	0.1		0.1		0.1		ns
t_{WASU}	1.3		1.6		2.1		ns
t_{WAH}	2.1		2.5		3.3		ns
t_{RASU}	2.2		2.6		3.5		ns
t_{RAH}	0.1		0.1		0.2		ns
t_{WO}		2.0		2.4		3.2	ns
t_{DD}		2.0		2.4		3.2	ns
t_{EABOUT}		0.0		0.1		0.1	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	3.3		4.0		5.3		ns

Table 62. EPF10K200E Device EAB Internal Timing Macroparameters (Part 1 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		5.1		6.4		8.4	ns
$t_{EABRCOMB}$	5.1		6.4		8.4		ns
$t_{EABRCREG}$	4.8		5.7		7.6		ns
t_{EABWP}	3.3		4.0		5.3		ns

Figure 31. FLEX 10KE $I_{CCACTIVE}$ vs. Operating Frequency (Part 2 of 2)



Configuration & Operation

The FLEX 10KE architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The FLEX 10KE architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. The process of physically loading the SRAM data into the device is called *configuration*. Before configuration, as V_{CC} rises, the device initiates a Power-On Reset (POR). This POR event clears the device and prepares it for configuration. The FLEX 10KE POR time does not exceed 50 µs.

When configuring with a configuration device, refer to the respective configuration device data sheet for POR timing information.

Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the Altera Digital Library for pin-out information.

Revision History

The information contained in the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.5 supersedes information published in previous versions.

Version 2.5

The following changes were made to the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.5:

- *Note (1)* added to Figure 23.
- Text added to "I/O Element" section on page 34.
- Updated Table 22.

Version 2.4

The following changes were made to the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.4: updated text on page 34 and page 63.