Intel - EPF10K200SRC240-3N Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	1248
Number of Logic Elements/Cells	9984
Total RAM Bits	98304
Number of I/O	182
Number of Gates	513000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-RQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k200src240-3n

Table 2. FLEX 10KE Device Features

Feature	EPF10K100E *(2)*	EPF10K130E	EPF10K200E EPF10K200S
Typical gates *(1)*	100,000	130,000	200,000
Maximum system gates	257,000	342,000	513,000
Logic elements (LEs)	4,992	6,656	9,984
EABs	12	16	24
Total RAM bits	49,152	65,536	98,304
Maximum user I/O pins	338	413	470

Note to tables:

(1) The embedded IEEE Std. 1149.1 JTAG circuitry adds up to 31,250 gates in addition to the listed typical or maximum system gates.

(2) New EPF10K100B designs should use EPF10K100E devices.

…and More Features

- Fabricated on an advanced process and operate with a 2.5-V internal supply voltage
- In-circuit reconfigurability (ICR) via external configuration devices, intelligent controller, or JTAG port
- ClockLock™ and ClockBoost™ options for reduced clock delay/skew and clock multiplication
- Built-in low-skew clock distribution trees
- 100% functional testing of all devices; test vectors or scan chains are not required
- Pull-up on I/O pins before and during configuration

■ Flexible interconnect

- FastTrack® Interconnect continuous routing structure for fast, predictable interconnect delays
- Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
- Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
- Tri-state emulation that implements internal tri-state buses
- Up to six global clock signals and four global clear signals

■ Powerful I/O pins

- Individual tri-state output enable control for each pin
- Open-drain option on each I/O pin
- Programmable output slew-rate control to reduce switching noise
- Clamp to V_{CCIO} user-selectable on a pin-by-pin basis
- Supports hot-socketing

Embedded Array Block

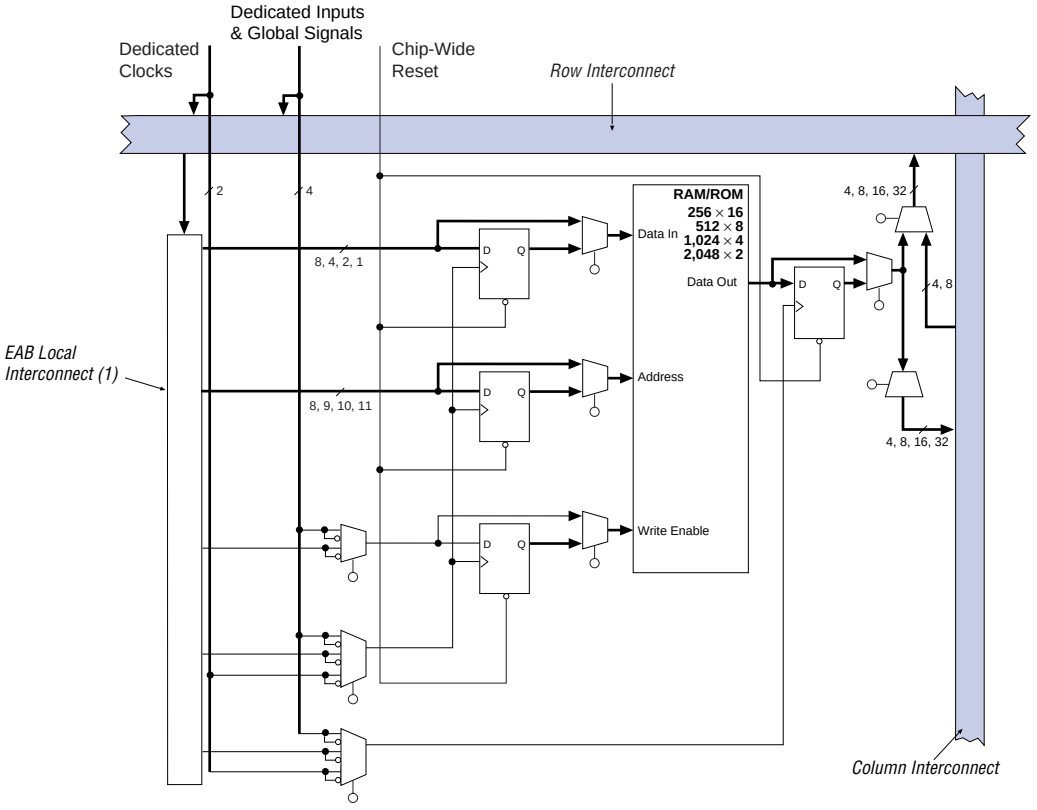
The EAB is a flexible block of RAM, with registers on the input and output ports, that is used to implement common gate array megafunctions. Because it is large and flexible, the EAB is suitable for functions such as multipliers, vector scalars, and error correction circuits. These functions can be combined in applications such as digital filters and microcontrollers.

Logic functions are implemented by programming the EAB with a read-only pattern during configuration, thereby creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of EABs. The large capacity of EABs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or field-programmable gate array (FPGA) RAM blocks. For example, a single EAB can implement any function with 8 inputs and 16 outputs. Parameterized functions such as LPM functions can take advantage of the EAB automatically.

The FLEX 10KE EAB provides advantages over FPGAs, which implement on-board RAM as arrays of small, distributed RAM blocks. These small FPGA RAM blocks must be connected together to make RAM blocks of manageable size. The RAM blocks are connected together using multiplexers implemented with more logic blocks. These extra multiplexers cause extra delay, which slows down the RAM block. FPGA RAM blocks are also prone to routing problems because small blocks of RAM must be connected together to make larger blocks. In contrast, EABs can be used to implement large, dedicated blocks of RAM that eliminate these timing and routing concerns.

The FLEX 10KE enhanced EAB adds dual-port capability to the existing EAB structure. The dual-port structure is ideal for FIFO buffers with one or two clocks. The FLEX 10KE EAB can also support up to 16-bit-wide RAM blocks and is backward-compatible with any design containing FLEX 10K EABs. The FLEX 10KE EAB can act in dual-port or single-port mode. When in dual-port mode, separate clocks may be used for EAB read and write sections, which allows the EAB to be written and read at different rates. It also has separate synchronous clock enable signals for the EAB read and write sections, which allow independent control of these sections.

Figure 4. FLEX 10KE Device in Single-Port RAM Mode



Note:

(1) EPF10K30E, EPF10K50E, and EPF10K50S devices have 88 EAB local interconnect channels; EPF10K100E, EPF10K130E, EPF10K200E, and EPF10K200S devices have 104 EAB local interconnect channels.

EABs can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the write enable signal. In contrast, the EAB's synchronous RAM generates its own write enable signal and is self-timed with respect to the input or write clock. A circuit using the EAB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

Clearable Counter Mode

The clearable counter mode is similar to the up / down counter mode, but supports a synchronous clear instead of the up / down control. The clear function is substituted for the cascade-in signal in the up / down counter mode. Use 2 three-input LUTs: one generates the counter data, and the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer. The output of this multiplexer is ANDed with a synchronous clear signal.

Internal Tri-State Emulation

Internal tri-state emulation provides internal tri-states without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable (OE) signals select which signal drives the bus. However, if multiple OE signals are active, contending signals can be driven onto the bus. Conversely, if no OE signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The Altera software automatically implements tri-state bus functionality with a multiplexer.

Clear & Preset Logic Control

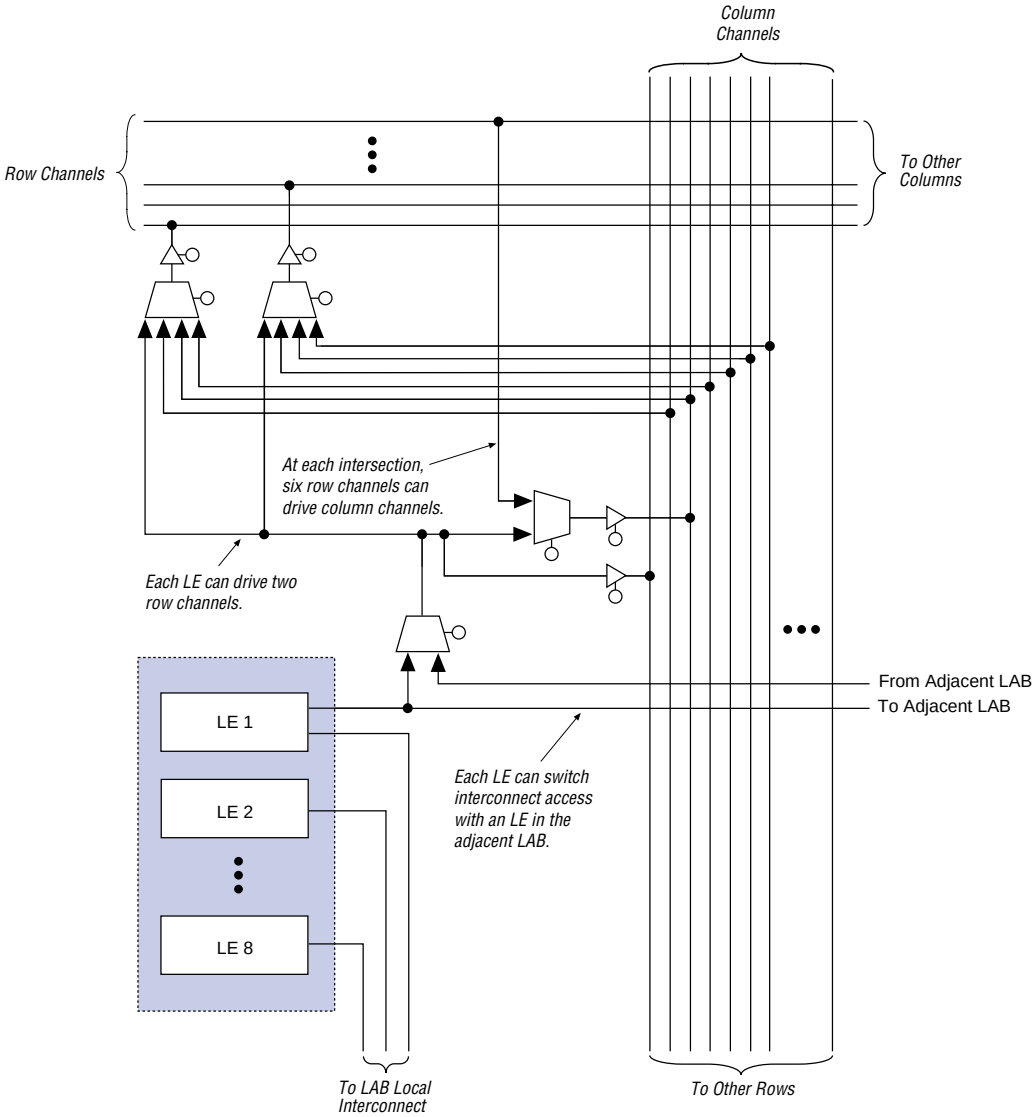
Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. The clear and preset control structure of the LE asynchronously loads signals into a register. Either LABCTRL1 or LABCTRL2 can control the asynchronous clear. Alternatively, the register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

During compilation, the Altera Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six modes chosen during design entry:

- Asynchronous clear
- Asynchronous preset
- Asynchronous clear and preset
- Asynchronous load with clear
- Asynchronous load with preset
- Asynchronous load without clear or preset

Figure 13. FLEX 10KE LAB Connections to Row & Column Interconnect



For improved routing, the row interconnect consists of a combination of full-length and half-length channels. The full-length channels connect to all LABs in a row; the half-length channels connect to the LABs in half of the row. The EAB can be driven by the half-length channels in the left half of the row and by the full-length channels. The EAB drives out to the full-length channels. In addition to providing a predictable, row-wide interconnect, this architecture provides increased routing resources. Two neighboring LABs can be connected using a half-row channel, thereby saving the other half of the channel for the other half of the row.

Table 7 summarizes the FastTrack Interconnect routing structure resources available in each FLEX 10KE device.

Table 7. FLEX 10KE FastTrack Interconnect Resources

Device	Rows	Channels per Row	Columns	Channels per Column
EPF10K30E	6	216	36	24
EPF10K50E EPF10K50S	10	216	36	24
EPF10K100E	12	312	52	24
EPF10K130E	16	312	52	32
EPF10K200E EPF10K200S	24	312	52	48

In addition to general-purpose I/O pins, FLEX 10KE devices have six dedicated input pins that provide low-skew signal distribution across the device. These six inputs can be used for global clock, clear, preset, and peripheral output enable and clock enable control signals. These signals are available as control signals for all LABs and IOEs in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device.

Figure 14 shows the interconnection of adjacent LABs and EABs, with row, column, and local interconnects, as well as the associated cascade and carry chains. Each LAB is labeled according to its location: a letter represents the row and a number represents the column. For example, LAB B3 is in row B, column 3.

Table 9. Peripheral Bus Sources for EPF10K100E, EPF10K130E, EPF10K200E & EPF10K200S Devices

Peripheral Control Signal	EPF10K100E	EPF10K130E	EPF10K200E EPF10K200S
OE0	Row A	Row C	Row G
OE1	Row C	Row E	Row I
OE2	Row E	Row G	Row K
OE3	Row L	Row N	Row R
OE4	Row I	Row K	Row O
OE5	Row K	Row M	Row Q
CLKENA0/CLK0/GLOBAL0	Row F	Row H	Row L
CLKENA1/OE6/GLOBAL1	Row D	Row F	Row J
CLKENA2/CLR0	Row B	Row D	Row H
CLKENA3/OE7/GLOBAL2	Row H	Row J	Row N
CLKENA4/CLR1	Row J	Row L	Row P
CLKENA5/CLK1/GLOBAL3	Row G	Row I	Row M

Signals on the peripheral control bus can also drive the four global signals, referred to as GLOBAL0 through GLOBAL3 in Tables 8 and 9. An internally generated signal can drive a global signal, providing the same low-skew, low-delay characteristics as a signal driven by an input pin. An LE drives the global signal by driving a row line that drives the peripheral bus, which then drives the global signal. This feature is ideal for internally generated clear or clock signals with high fan-out. However, internally driven global signals offer no advantage over the general-purpose interconnect for routing data signals. The dedicated input pin should be driven to a known logic state (such as ground) and not be allowed to float.

The chip-wide output enable pin is an active-high pin (DEV_OE) that can be used to tri-state all pins on the device. This option can be set in the Altera software. On EPF10K50E and EPF10K200E devices, the built-in I/O pin pull-up resistors (which are active during configuration) are active when the chip-wide output enable pin is asserted. The registers in the IOE can also be reset by the chip-wide reset pin.

Row-to-IOE Connections

When an IOE is used as an input signal, it can drive two separate row channels. The signal is accessible by all LEs within that row. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the row channels. Up to eight IOEs connect to each side of each row channel (see Figure 16).

Figure 16. FLEX 10KE Row-to-IOE Connections

The values for m and n are provided in Table 10.

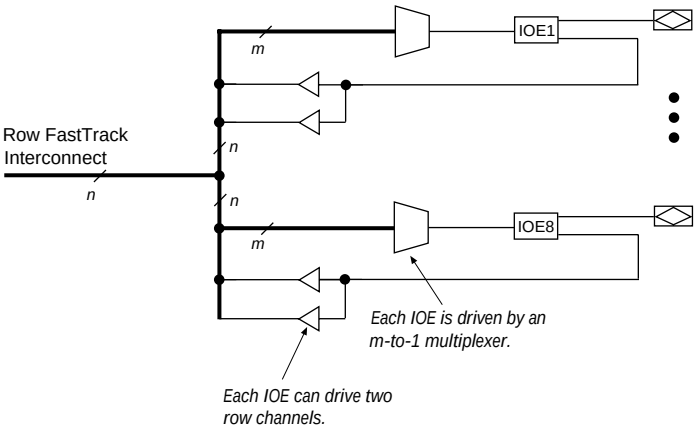


Table 10 lists the FLEX 10KE row-to-IOE interconnect resources.

Table 10. FLEX 10KE Row-to-IOE Interconnect Resources

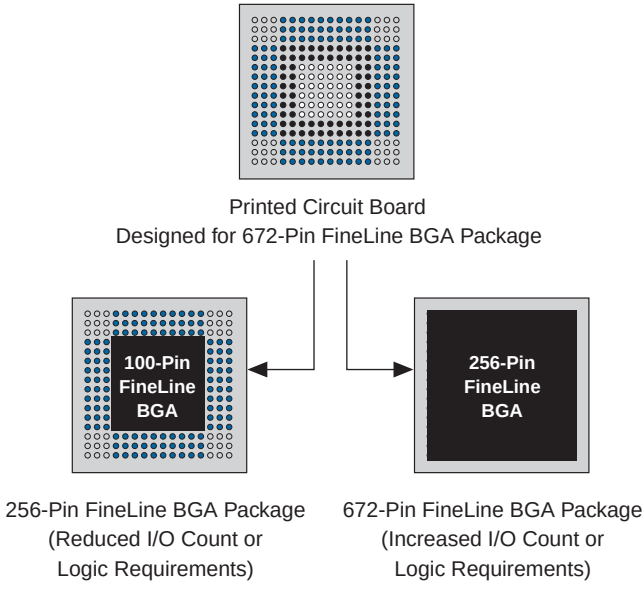
Device	Channels per Row *(n)*	Row Channels per Pin *(m)*
EPF10K30E	216	27
EPF10K50E EPF10K50S	216	27
EPF10K100E	312	39
EPF10K130E	312	39
EPF10K200E EPF10K200S	312	39

SameFrame Pin-Outs

FLEX 10KE devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density / package combinations. For example, a single board layout can support a range of devices from an EPF10K30E device in a 256-pin FineLine BGA package to an EPF10K200S device in a 672-pin FineLine BGA package.

The Altera software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software generates pin-outs describing how to lay out a board to take advantage of this migration (see Figure 18).

Figure 18. SameFrame Pin-Out Example



The VCCINT pins must always be connected to a 2.5-V power supply. With a 2.5-V V_{CCINT} level, input voltages are compatible with 2.5-V, 3.3-V, and 5.0-V inputs. The VCCIO pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels higher than 3.0 V achieve a faster timing delay of t_{OD2} instead of t_{OD1}.

Table 14 summarizes FLEX 10KE MultiVolt I/O support.

Table 14. FLEX 10KE MultiVolt I/O Support

V_{CCIO} (V)	Input Signal (V)			Output Signal (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓ *(1)*	✓ *(1)*	✓		
3.3	✓	✓	✓ *(1)*	✓ *(2)*	✓	✓

Notes:

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than V_{CCIO}.

(2) When V_{CCIO} = 3.3 V, a FLEX 10KE device can drive a 2.5-V device that has 3.3-V tolerant inputs.

Open-drain output pins on FLEX 10KE devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a V_{IH} of 3.5 V. When the open-drain pin is active, it will drive low. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The I_{OL} current specification should be considered when selecting a pull-up resistor.

Power Sequencing & Hot-Socketing

Because FLEX 10KE devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into FLEX 10KE devices before and during power up without damaging the device. Additionally, FLEX 10KE devices do not drive out during power up. Once operating conditions are reached, FLEX 10KE devices operate as specified by the user.

Figure 22 shows the required relationship between V_{CCIO} and V_{CCINT} for 3.3-V PCI compliance.

Figure 22. Relationship between V_{CCIO} & V_{CCINT} for 3.3-V PCI Compliance

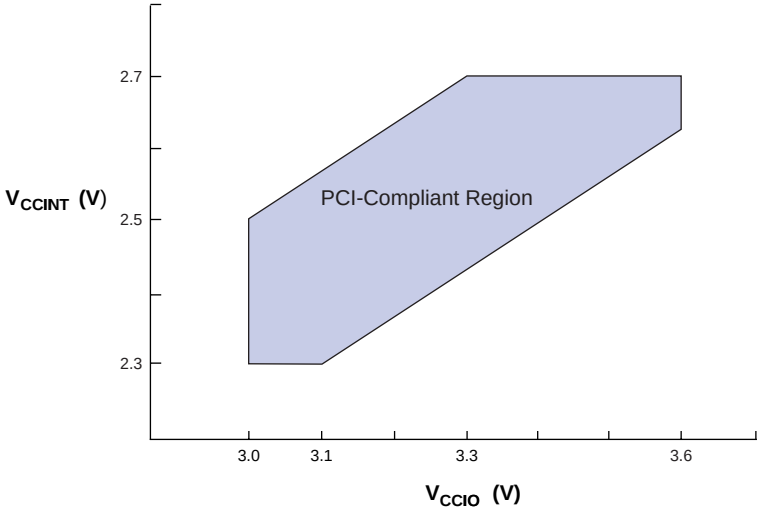


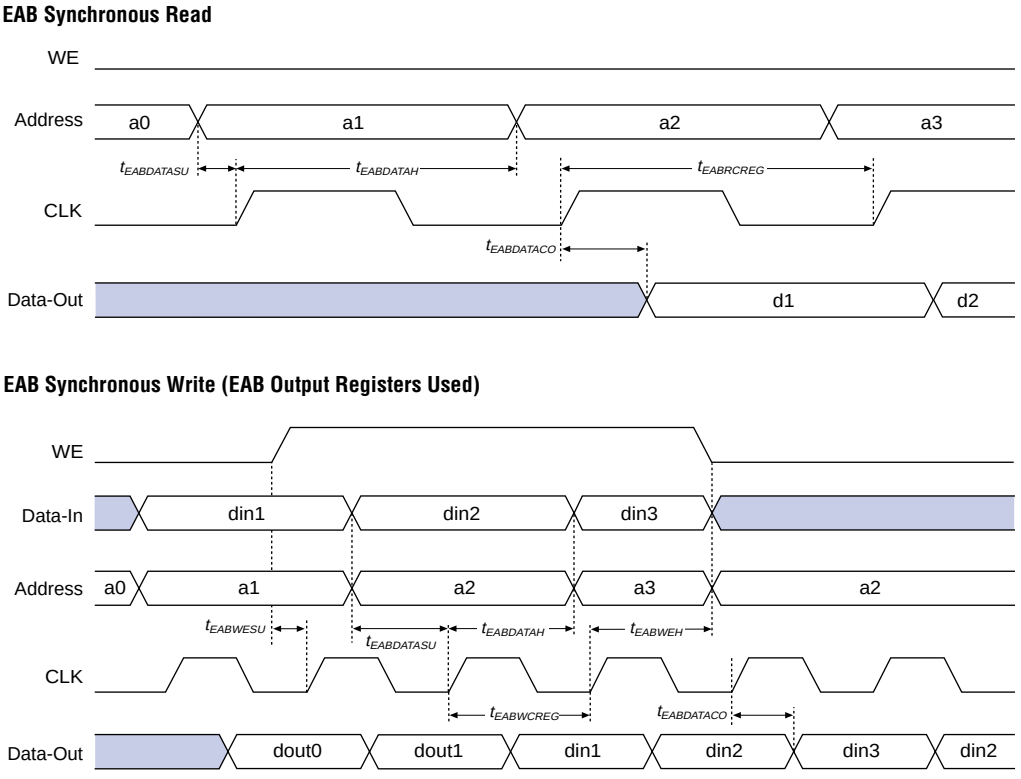
Figure 23 shows the typical output drive characteristics of FLEX 10KE devices with 3.3-V and 2.5-V V_{CCIO}. The output driver is compliant to the 3.3-V ***PCI Local Bus Specification, Revision 2.2*** (when VCCIO pins are connected to 3.3 V). FLEX 10KE devices with a -1 speed grade also comply with the drive strength requirements of the ***PCI Local Bus Specification, Revision 2.2*** (when VCCINT pins are powered with a minimum supply of 2.375 V, and VCCIO pins are connected to 3.3 V). Therefore, these devices can be used in open 5.0-V PCI systems.

Table 24. LE Timing Microparameters (Part 2 of 2) *Note (1)*		
Symbol	**Parameter**	**Condition**
t_{CLR}	LE register clear delay	
t_{CH}	Minimum clock high time from clock pin	
t_{CL}	Minimum clock low time from clock pin	

Table 25. IOE Timing Microparameters *Note (1)*		
Symbol	**Parameter**	**Conditions**
t_{IOD}	IOE data delay	
t_{IOC}	IOE register control signal delay	
t_{IOCO}	IOE register clock-to-output delay	
t_{IOCOMB}	IOE combinatorial delay	
t_{IOSU}	IOE register setup time for data and enable signals before clock; IOE register recovery time after asynchronous clear	
t_{IOH}	IOE register hold time for data and enable signals after clock	
t_{IOCLR}	IOE register clear time	
t_{OD1}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 3.3 V	C1 = 35 pF *(2)*
t_{OD2}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 2.5 V	C1 = 35 pF *(3)*
t_{OD3}	Output buffer and pad delay, slow slew rate = on	C1 = 35 pF *(4)*
t_{XZ}	IOE output buffer disable delay	
t_{ZX1}	IOE output buffer enable delay, slow slew rate = off, V_{CCIO} = 3.3 V	C1 = 35 pF *(2)*
t_{ZX2}	IOE output buffer enable delay, slow slew rate = off, V_{CCIO} = 2.5 V	C1 = 35 pF *(3)*
t_{ZX3}	IOE output buffer enable delay, slow slew rate = on	C1 = 35 pF *(4)*
t_{INREG}	IOE input pad and buffer to IOE register delay	
t_{IOFD}	IOE register feedback delay	
t_{INCOMB}	IOE input pad and buffer to FastTrack Interconnect delay	

Table 27. EAB Timing Macroparameters *Note (1), (6)*		
Symbol	**Parameter**	**Conditions**
t_{EABAA}	EAB address access delay	
$t_{EABRCCOMB}$	EAB asynchronous read cycle time	
$t_{EABRCREG}$	EAB synchronous read cycle time	
t_{EABWP}	EAB write pulse width	
$t_{EABWCCOMB}$	EAB asynchronous write cycle time	
$t_{EABWCREG}$	EAB synchronous write cycle time	
t_{EABDD}	EAB data-in to data-out valid delay	
$t_{EABDATACO}$	EAB clock-to-output delay when using output registers	
$t_{EABDATASU}$	EAB data/address setup time before clock when using input register	
$t_{EABDATAH}$	EAB data/address hold time after clock when using input register	
$t_{EABWESU}$	EAB WE setup time before clock when using input register	
t_{EABWEH}	EAB WE hold time after clock when using input register	
$t_{EABWDSU}$	EAB data setup time before falling edge of write pulse when not using input registers	
t_{EABWDH}	EAB data hold time after falling edge of write pulse when not using input registers	
$t_{EABWASU}$	EAB address setup time before rising edge of write pulse when not using input registers	
t_{EABWAH}	EAB address hold time after falling edge of write pulse when not using input registers	
t_{EABWO}	EAB write enable to data output valid delay	

Figure 30. EAB Synchronous Timing Waveforms



Tables 31 through 37 show EPF10K30E device internal and external timing parameters.

Table 31. EPF10K30E Device LE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.7		0.8		1.1	ns
t_{CLUT}		0.5		0.6		0.8	ns
t_{RLUT}		0.6		0.7		1.0	ns
t_{PACKED}		0.3		0.4		0.5	ns
t_{EN}		0.6		0.8		1.0	ns
t_{CICO}		0.1		0.1		0.2	ns
t_{CGEN}		0.4		0.5		0.7	ns

Table 35. EPF10K30E Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		1.8		2.4		2.9	ns
t_{DIN2LE}		1.5		1.8		2.4	ns
$t_{DIN2DATA}$		1.5		1.8		2.2	ns
$t_{DCLK2IOE}$		2.2		2.6		3.0	ns
$t_{DCLK2LE}$		1.5		1.8		2.4	ns
$t_{SAMELAB}$		0.1		0.2		0.3	ns
$t_{SAMEROW}$		2.0		2.4		2.7	ns
$t_{SAMECOLUMN}$		0.7		1.0		0.8	ns
$t_{DIFFROW}$		2.7		3.4		3.5	ns
$t_{TWOROWS}$		4.7		5.8		6.2	ns
$t_{LEPERIPH}$		2.7		3.4		3.8	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.8		0.8		1.1	ns

Table 36. EPF10K30E External Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		8.0		9.5		12.5	ns
t_{INSU} *(3)*	2.1		2.5		3.9		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	4.9	2.0	5.9	2.0	7.6	ns
t_{INSU} *(4)*	1.1		1.5		–		ns
t_{INH} *(4)*	0.0		0.0		–		ns
t_{OUTCO} *(4)*	0.5	3.9	0.5	4.9	–	–	ns
t_{PCISU}	3.0		4.2		–		ns
t_{PCIH}	0.0		0.0		–		ns
t_{PCICO}	2.0	6.0	2.0	7.5	–	–	ns

Table 47. EPF10K100E Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.5		2.0		2.6	ns
$t_{EABDATA1}$		0.0		0.0		0.0	ns
t_{EABWE1}		1.5		2.0		2.6	ns
t_{EABWE2}		0.3		0.4		0.5	ns
t_{EABRE1}		0.3		0.4		0.5	ns
t_{EABRE2}		0.0		0.0		0.0	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.3		0.4		0.5	ns
$t_{EABBYPASS}$		0.1		0.1		0.2	ns
t_{EABSU}	0.8		1.0		1.4		ns
t_{EABH}	0.1		0.1		0.2		ns
t_{EABCLR}	0.3		0.4		0.5		ns
t_{AA}		4.0		5.1		6.6	ns
t_{WP}	2.7		3.5		4.7		ns
t_{RP}	1.0		1.3		1.7		ns
t_{WDSU}	1.0		1.3		1.7		ns
t_{WDH}	0.2		0.2		0.3		ns
t_{WASU}	1.6		2.1		2.8		ns
t_{WAH}	1.6		2.1		2.8		ns
t_{RASU}	3.0		3.9		5.2		ns
t_{RAH}	0.1		0.1		0.2		ns
t_{WO}		1.5		2.0		2.6	ns
t_{DD}		1.5		2.0		2.6	ns
t_{EABOUT}		0.2		0.3		0.3	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	2.7		3.5		4.7		ns

Table 48. EPF10K100E Device EAB Internal Timing Macroparameters *(Part 1 of 2)* *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		5.9		7.6		9.9	ns
$t_{EABRCOMB}$	5.9		7.6		9.9		ns
$t_{EABRCREG}$	5.1		6.5		8.5		ns
t_{EABWP}	2.7		3.5		4.7		ns

Table 56. EPF10K130E Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		2.8		3.5		4.4	ns
t_{DIN2LE}		0.7		1.2		1.6	ns
$t_{DIN2DATA}$		1.6		1.9		2.2	ns
$t_{DCLK2IOE}$		1.6		2.1		2.7	ns
$t_{DCLK2LE}$		0.7		1.2		1.6	ns
$t_{SAMELAB}$		0.1		0.2		0.2	ns
$t_{SAMEROW}$		1.9		3.4		5.1	ns
$t_{SAMECOLUMN}$		0.9		2.6		4.4	ns
$t_{DIFFROW}$		2.8		6.0		9.5	ns
$t_{TWOROWS}$		4.7		9.4		14.6	ns
$t_{LEPERIPH}$		3.1		4.7		6.9	ns
$t_{LABCARRY}$		0.6		0.8		1.0	ns
$t_{LABCASC}$		0.9		1.2		1.6	ns

Table 57. EPF10K130E External Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		9.0		12.0		16.0	ns
t_{INSU} *(3)*	1.9		2.1		3.0		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	5.0	2.0	7.0	2.0	9.2	ns
t_{INSU} *(4)*	0.9		1.1		–		ns
t_{INH} *(4)*	0.0		0.0		–		ns
t_{OUTCO} *(4)*	0.5	4.0	0.5	6.0	–	–	ns
t_{PCISU}	3.0		6.2		–		ns
t_{PCIH}	0.0		0.0		–		ns
t_{PCICO}	2.0	6.0	2.0	6.9	–	–	ns

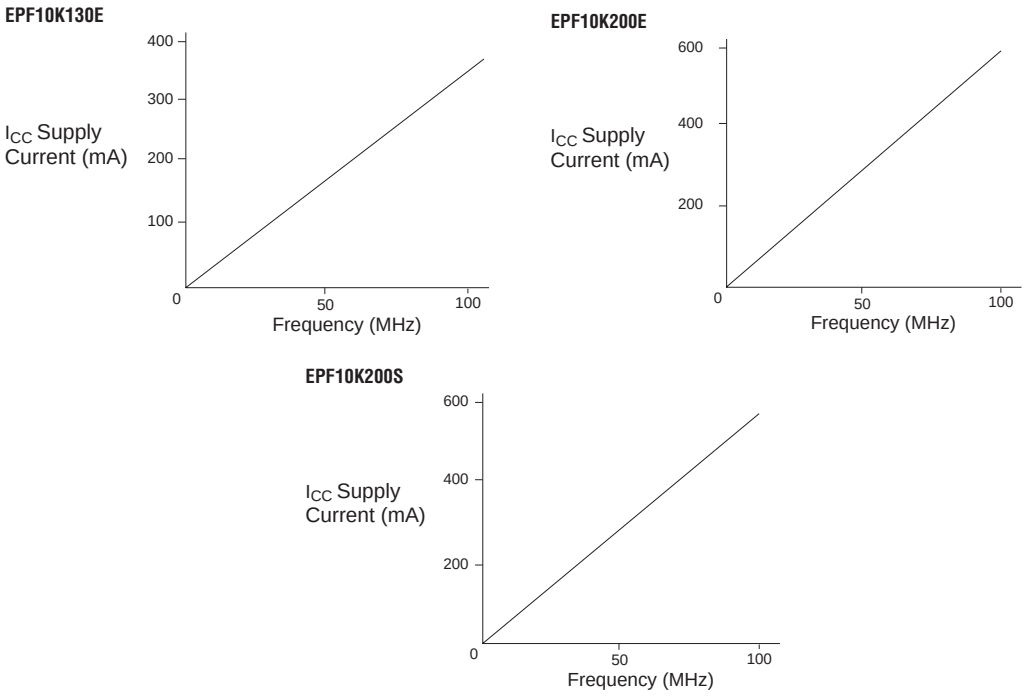
Table 61. EPF10K200E Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		2.0		2.4		3.2	ns
$t_{EABDATA1}$		0.4		0.5		0.6	ns
t_{EABWE1}		1.4		1.7		2.3	ns
t_{EABWE2}		0.0		0.0		0.0	ns
t_{EABRE1}		0		0		0	ns
t_{EABRE2}		0.4		0.5		0.6	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.8		0.9		1.2	ns
$t_{EABBYPASS}$		0.0		0.1		0.1	ns
t_{EABSU}	0.9		1.1		1.5		ns
t_{EABH}	0.4		0.5		0.6		ns
t_{EABCLR}	0.8		0.9		1.2		ns
t_{AA}		3.1		3.7		4.9	ns
t_{WP}	3.3		4.0		5.3		ns
t_{RP}	0.9		1.1		1.5		ns
t_{WDSU}	0.9		1.1		1.5		ns
t_{WDH}	0.1		0.1		0.1		ns
t_{WASU}	1.3		1.6		2.1		ns
t_{WAH}	2.1		2.5		3.3		ns
t_{RASU}	2.2		2.6		3.5		ns
t_{RAH}	0.1		0.1		0.2		ns
t_{WO}		2.0		2.4		3.2	ns
t_{DD}		2.0		2.4		3.2	ns
t_{EABOUT}		0.0		0.1		0.1	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	3.3		4.0		5.3		ns

Table 62. EPF10K200E Device EAB Internal Timing Macroparameters (Part 1 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		5.1		6.4		8.4	ns
$t_{EABRCOMB}$	5.1		6.4		8.4		ns
$t_{EABRCREG}$	4.8		5.7		7.6		ns
t_{EABWP}	3.3		4.0		5.3		ns

Figure 31. FLEX 10KE $I_{CCACTIVE}$ vs. Operating Frequency (Part 2 of 2)



Configuration & Operation

The FLEX 10KE architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

Operating Modes

The FLEX 10KE architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. The process of physically loading the SRAM data into the device is called *configuration*. Before configuration, as V_{CC} rises, the device initiates a Power-On Reset (POR). This POR event clears the device and prepares it for configuration. The FLEX 10KE POR time does not exceed 50 µs.

When configuring with a configuration device, refer to the respective configuration device data sheet for POR timing information.

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