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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	216
Number of Logic Elements/Cells	1728
Total RAM Bits	24576
Number of I/O	176
Number of Gates	119000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k30efc256-3

Table 4. FLEX 10KE Package Sizes

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP RQFP	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA	599-Pin PGA	600-Pin BGA	672-Pin FineLine BGA
Pitch (mm)	0.50	0.50	0.50	1.0	1.27	1.0	—	1.27	1.0
Area (mm ²)	484	936	1,197	289	1,225	529	3,904	2,025	729
Length × width (mm × mm)	22 × 22	30.6 × 30.6	34.6 × 34.6	17 × 17	35 × 35	23 × 23	62.5 × 62.5	45 × 45	27 × 27

General Description

Altera FLEX 10KE devices are enhanced versions of FLEX 10K devices. Based on reconfigurable CMOS SRAM elements, the FLEX architecture incorporates all features necessary to implement common gate array megafunctions. With up to 200,000 typical gates, FLEX 10KE devices provide the density, speed, and features to integrate entire systems, including multiple 32-bit buses, into a single device.

The ability to reconfigure FLEX 10KE devices enables 100% testing prior to shipment and allows the designer to focus on simulation and design verification. FLEX 10KE reconfigurability eliminates inventory management for gate array designs and generation of test vectors for fault coverage.

Table 5 shows FLEX 10KE performance for some common designs. All performance values were obtained with Synopsys DesignWare or LPM functions. Special design techniques are not required to implement the applications; the designer simply infers or instantiates a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks, the other two can be used for clear/preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I/O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I/O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LE in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated from LE outputs.

Logic Element

The LE, the smallest unit of logic in the FLEX 10KE architecture, has a compact size that provides efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous clock enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect routing structure (see [Figure 8](#)).

Figure 8. FLEX 10KE Logic Element

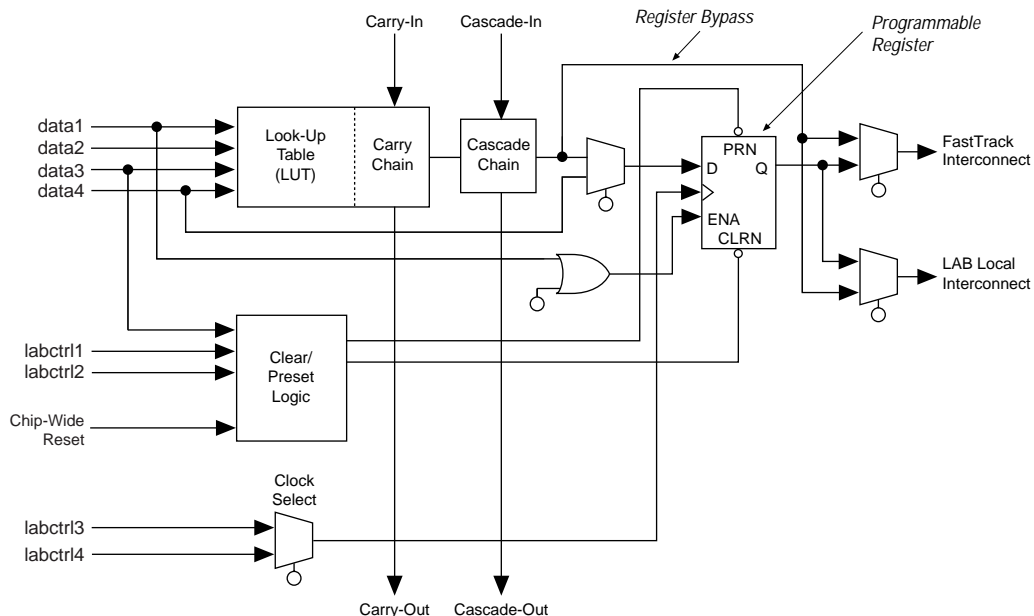
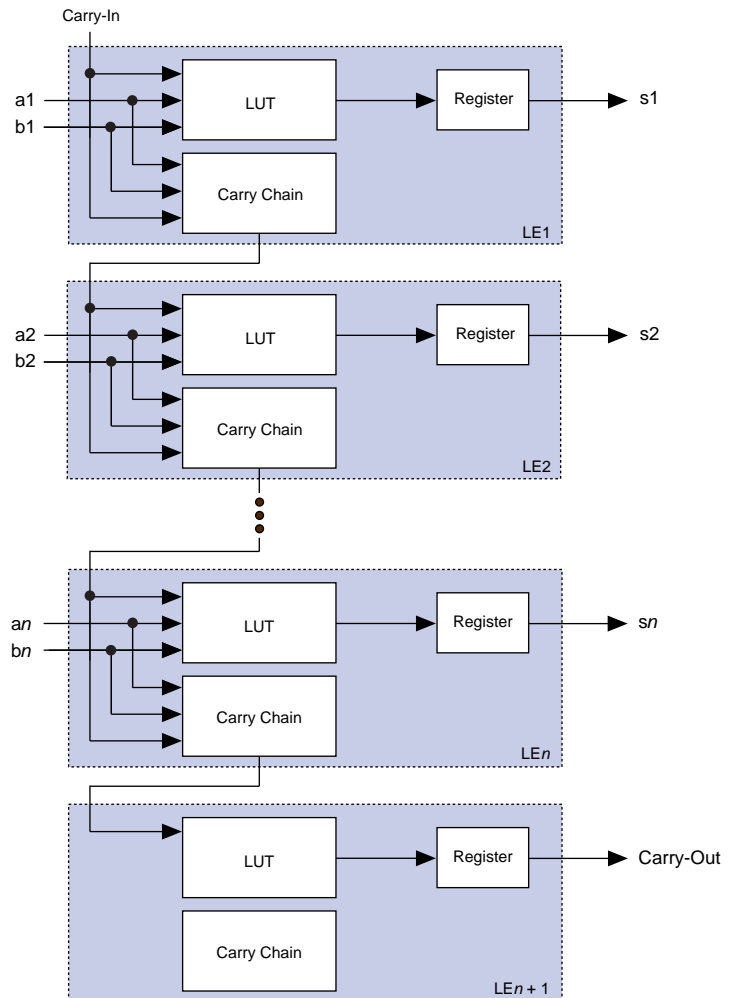


Figure 9 shows how an n -bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for an accumulator function. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal.

Figure 9. FLEX 10KE Carry Chain Operation (n -Bit Full Adder)



Clearable Counter Mode

The clearable counter mode is similar to the up/down counter mode, but supports a synchronous clear instead of the up/down control. The clear function is substituted for the cascade-in signal in the up/down counter mode. Use 2 three-input LUTs: one generates the counter data, and the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer. The output of this multiplexer is ANDed with a synchronous clear signal.

Internal Tri-State Emulation

Internal tri-state emulation provides internal tri-states without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable (OE) signals select which signal drives the bus. However, if multiple OE signals are active, contending signals can be driven onto the bus. Conversely, if no OE signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The Altera software automatically implements tri-state bus functionality with a multiplexer.

Clear & Preset Logic Control

Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. The clear and preset control structure of the LE asynchronously loads signals into a register. Either LABCTRL1 or LABCTRL2 can control the asynchronous clear. Alternatively, the register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

During compilation, the Altera Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six modes chosen during design entry:

- Asynchronous clear
- Asynchronous preset
- Asynchronous clear and preset
- Asynchronous load with clear
- Asynchronous load with preset
- Asynchronous load without clear or preset

Asynchronous Clear

The flipflop can be cleared by either LABCTRL1 or LABCTRL2. In this mode, the preset signal is tied to VCC to deactivate it.

Asynchronous Preset

An asynchronous preset is implemented as an asynchronous load, or with an asynchronous clear. If DATA3 is tied to VCC, asserting LABCTRL1 asynchronously loads a one into the register. Alternatively, the Altera software can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used for one of the LE operating modes.

Asynchronous Preset & Clear

When implementing asynchronous clear and preset, LABCTRL1 controls the preset and LABCTRL2 controls the clear. DATA3 is tied to VCC, so that asserting LABCTRL1 asynchronously loads a one into the register, effectively presetting the register. Asserting LABCTRL2 clears the register.

Asynchronous Load with Clear

When implementing an asynchronous load in conjunction with the clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear. LABCTRL2 implements the clear by controlling the register clear; LABCTRL2 does not have to feed the preset circuits.

Asynchronous Load with Preset

When implementing an asynchronous load in conjunction with preset, the Altera software provides preset control by using the clear and inverting the input and output of the register. Asserting LABCTRL2 presets the register, while asserting LABCTRL1 loads the register. The Altera software inverts the signal that drives DATA3 to account for the inversion of the register's output.

Asynchronous Load without Preset or Clear

When implementing an asynchronous load without preset or clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear.

FastTrack Interconnect Routing Structure

In the FLEX 10KE architecture, connections between LEs, EABs, and device I/O pins are provided by the FastTrack Interconnect routing structure, which is a series of continuous horizontal and vertical routing channels that traverses the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect routing structure consists of row and column interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect. The row interconnect can drive I/O pins and feed other LABs in the row. The column interconnect routes signals between rows and can drive I/O pins.

Row channels drive into the LAB or EAB local interconnect. The row signal is buffered at every LAB or EAB to reduce the effect of fan-out on delay. A row channel can be driven by an LE or by one of three column channels. These four signals feed dual 4-to-1 multiplexers that connect to two specific row channels. These multiplexers, which are connected to each LE, allow column channels to drive row channels even when all eight LEs in a LAB drive the row interconnect.

Each column of LABs or EABs is served by a dedicated column interconnect. The column interconnect that serves the EABs has twice as many channels as other column interconnects. The column interconnect can then drive I/O pins or another row's interconnect to route the signals to other LABs or EABs in the device. A signal from the column interconnect, which can be either the output of a LE or an input from an I/O pin, must be routed to the row interconnect before it can enter a LAB or EAB. Each row channel that is driven by an IOE or EAB can drive one specific column channel.

Access to row and column channels can be switched between LEs in adjacent pairs of LABs. For example, a LE in one LAB can drive the row and column channels normally driven by a particular LE in the adjacent LAB in the same row, and vice versa. This flexibility enables routing resources to be used more efficiently (see [Figure 13](#)).

Figure 13. FLEX 10KE LAB Connections to Row & Column Interconnect

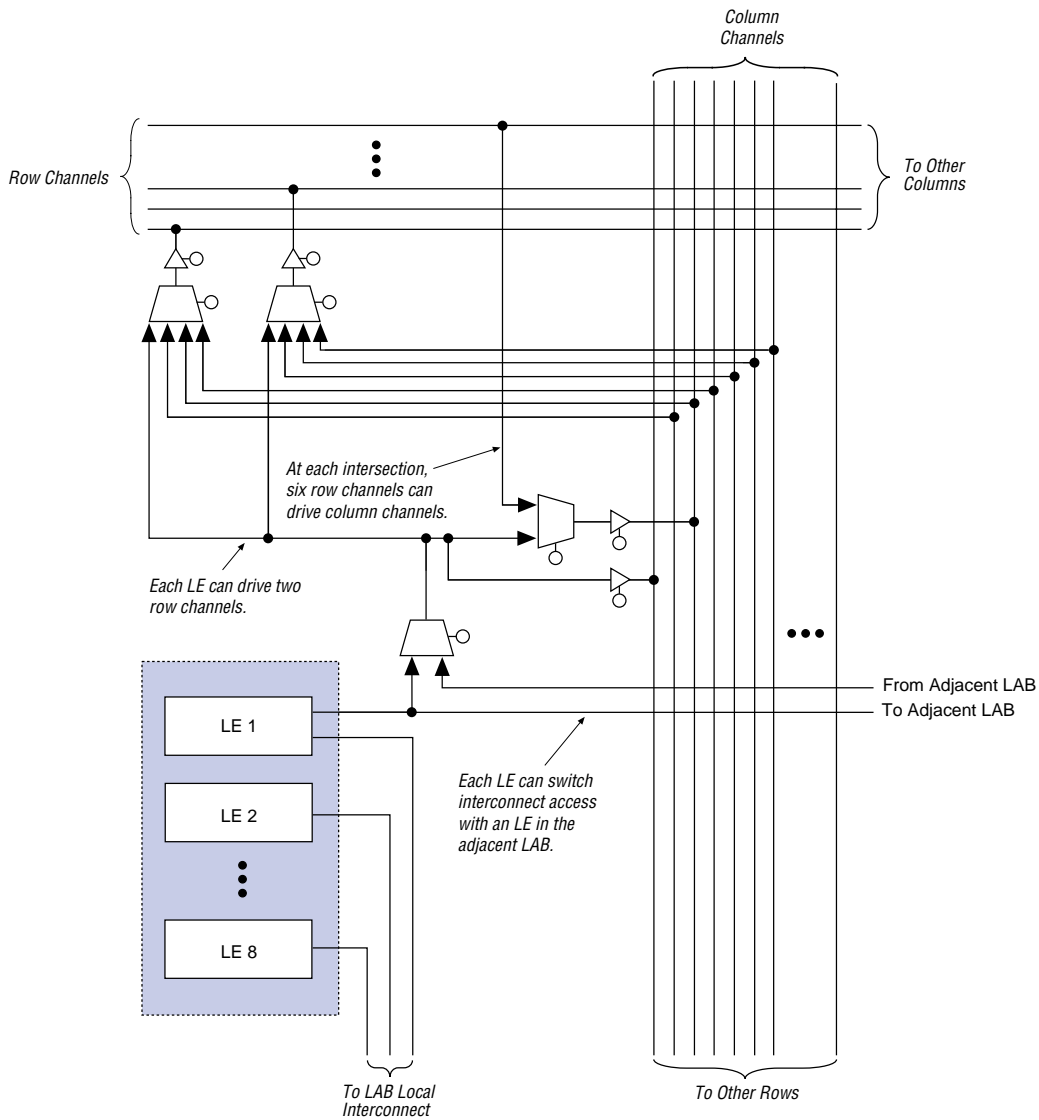
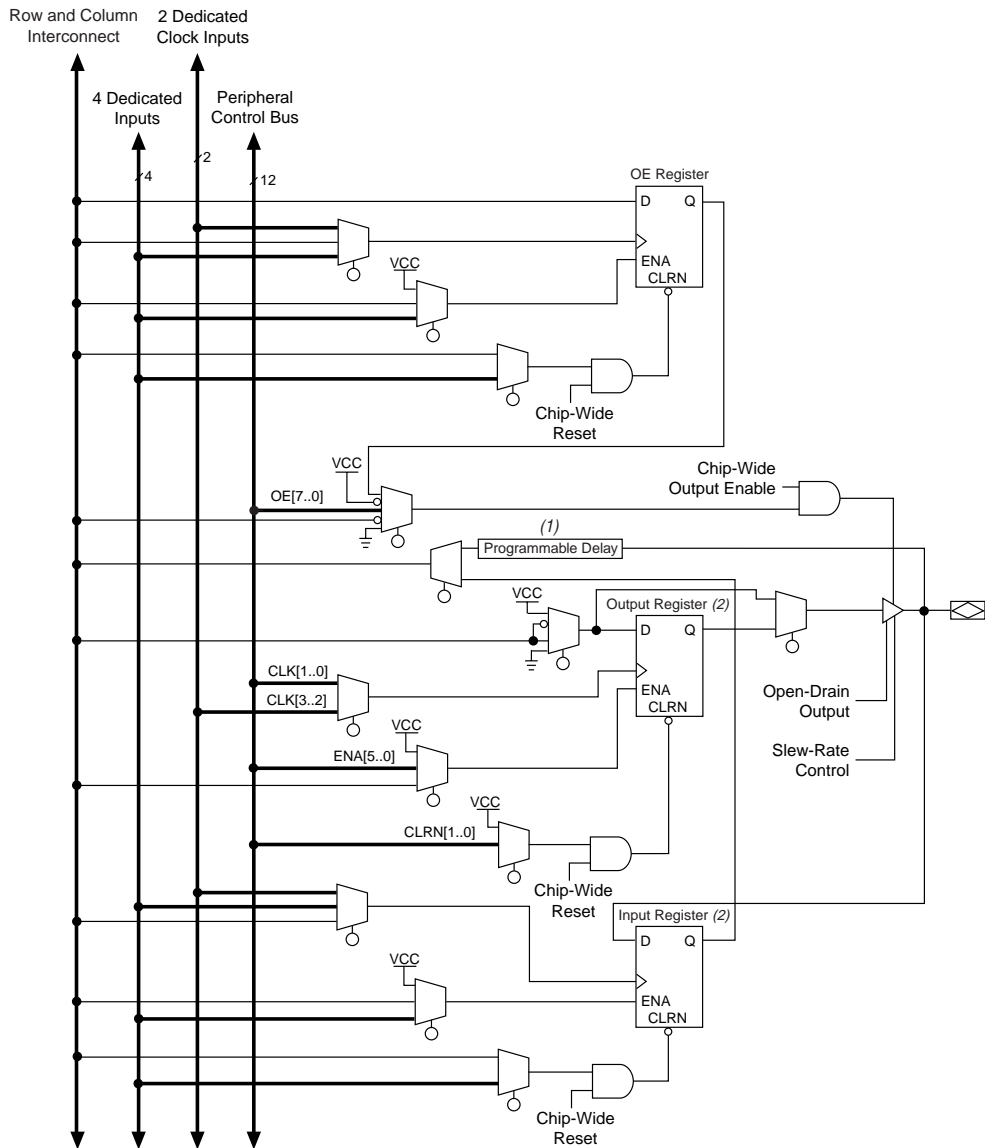


Figure 15. FLEX 10KE Bidirectional I/O Registers

**Note:**

- (1) All FLEX 10KE devices (except the EPF10K50E and EPF10K200E devices) have a programmable input delay buffer on the input path.

On all FLEX 10KE devices (except EPF10K50E and EPF10K200E devices), the input path from the I/O pad to the FastTrack Interconnect has a programmable delay element that can be used to guarantee a zero hold time. EPF10K50S and EPF10K200S devices also support this feature. Depending on the placement of the IOE relative to what it is driving, the designer may choose to turn on the programmable delay to ensure a zero hold time or turn it off to minimize setup time. This feature is used to reduce setup time for complex pin-to-register paths (e.g., PCI designs).

Each IOE selects the clock, clear, clock enable, and output enable controls from a network of I/O control signals called the peripheral control bus. The peripheral control bus uses high-speed drivers to minimize signal skew across the device and provides up to 12 peripheral control signals that can be allocated as follows:

- Up to eight output enable signals
- Up to six clock enable signals
- Up to two clock signals
- Up to two clear signals

If more than six clock enable or eight output enable signals are required, each IOE on the device can be controlled by clock enable and output enable signals driven by specific LEs. In addition to the two clock signals available on the peripheral control bus, each IOE can use one of two dedicated clock pins. Each peripheral control signal can be driven by any of the dedicated input pins or the first LE of each LAB in a particular row. In addition, a LE in a different row can drive a column interconnect, which causes a row interconnect to drive the peripheral control signal. The chip-wide reset signal resets all IOE registers, overriding any other control signals.

When a dedicated clock pin drives IOE registers, it can be inverted for all IOEs in the device. All IOEs must use the same sense of the clock. For example, if any IOE uses the inverted clock, all IOEs must use the inverted clock and no IOE can use the non-inverted clock. However, LEs can still use the true or complement of the clock on a LAB-by-LAB basis.

The incoming signal may be inverted at the dedicated clock pin and will drive all IOEs. For the true and complement of a clock to be used to drive IOEs, drive it into both global clock pins. One global clock pin will supply the true, and the other will supply the complement.

When the true and complement of a dedicated input drives IOE clocks, two signals on the peripheral control bus are consumed, one for each sense of the clock.

PCI Pull-Up Clamping Diode Option

FLEX 10KE devices have a pull-up clamping diode on every I/O, dedicated input, and dedicated clock pin. PCI clamping diodes clamp the signal to the V_{CCIO} value and are required for 3.3-V PCI compliance. Clamping diodes can also be used to limit overshoot in other systems.

Clamping diodes are controlled on a pin-by-pin basis. When V_{CCIO} is 3.3 V, a pin that has the clamping diode option turned on can be driven by a 2.5-V or 3.3-V signal, but not a 5.0-V signal. When V_{CCIO} is 2.5 V, a pin that has the clamping diode option turned on can be driven by a 2.5-V signal, but not a 3.3-V or 5.0-V signal. Additionally, a clamping diode can be activated for a subset of pins, which would allow a device to bridge between a 3.3-V PCI bus and a 5.0-V device.

Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces system noise and adds a maximum delay of 4.3 ns. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate pin-by-pin or assign a default slew rate to all pins on a device-wide basis. The slow slew rate setting affects the falling edge of the output.

Open-Drain Output Option

FLEX 10KE devices provide an optional open-drain output (electrically equivalent to open-collector output) for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

MultiVolt I/O Interface

The FLEX 10KE device architecture supports the MultiVolt I/O interface feature, which allows FLEX 10KE devices in all packages to interface with systems of differing supply voltages. These devices have one set of V_{CC} pins for internal operation and input buffers (V_{CCINT}), and another set for I/O output drivers (V_{CCIO}).

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All FLEX 10KE devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. FLEX 10KE devices can also be configured using the JTAG pins through the BitBlaster or ByteBlasterMV download cable, or via hardware that uses the Jam™ STAPL programming and test language. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. FLEX 10KE devices support the JTAG instructions shown in [Table 15](#).

Table 15. FLEX 10KE JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation.
USERCODE	Selects the user electronic signature (USERCODE) register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	These instructions are used when configuring a FLEX 10KE device via JTAG ports with a BitBlaster or ByteBlasterMV download cable, or using a Jam File (.jam) or Jam Byte-Code File (.jbc) via an embedded processor.

The instruction register length of FLEX 10KE devices is 10 bits. The USERCODE register length in FLEX 10KE devices is 32 bits; 7 bits are determined by the user, and 25 bits are pre-determined. [Tables 16](#) and [17](#) show the boundary-scan register length and device IDCODE information for FLEX 10KE devices.

Table 16. FLEX 10KE Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPF10K30E	690
EPF10K50E EPF10K50S	798
EPF10K100E	1,050
EPF10K130E	1,308
EPF10K200E EPF10K200S	1,446

Table 20. 2.5-V EPF10K50E & EPF10K200E Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CCINT}	Supply voltage for internal logic and input buffers	(3), (4)	2.30 (2.30)	2.70 (2.70)	V
V _{CCIO}	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(3), (4)	2.30 (2.30)	2.70 (2.70)	V
V _I	Input voltage	(5)	−0.5	5.75	V
V _O	Output voltage		0	V _{CCIO}	V
T _A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	−40	85	° C
T _J	Operating temperature	For commercial use	0	85	° C
		For industrial use	−40	100	° C
t _R	Input rise time			40	ns
t _F	Input fall time			40	ns

Table 21. 2.5-V EPF10K30E, EPF10K50S, EPF10K100E, EPF10K130E & EPF10K200S Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CCINT}	Supply voltage for internal logic and input buffers	(3), (4)	2.375 (2.375)	2.625 (2.625)	V
V _{CCIO}	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	(3), (4)	2.375 (2.375)	2.625 (2.625)	V
V _I	Input voltage	(5)	−0.5	5.75	V
V _O	Output voltage		0	V _{CCIO}	V
T _A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	−40	85	° C
T _J	Operating temperature	For commercial use	0	85	° C
		For industrial use	−40	100	° C
t _R	Input rise time			40	ns
t _F	Input fall time			40	ns

Figure 22 shows the required relationship between V_{CCIO} and V_{CCINT} for 3.3-V PCI compliance.

Figure 22. Relationship between V_{CCIO} & V_{CCINT} for 3.3-V PCI Compliance

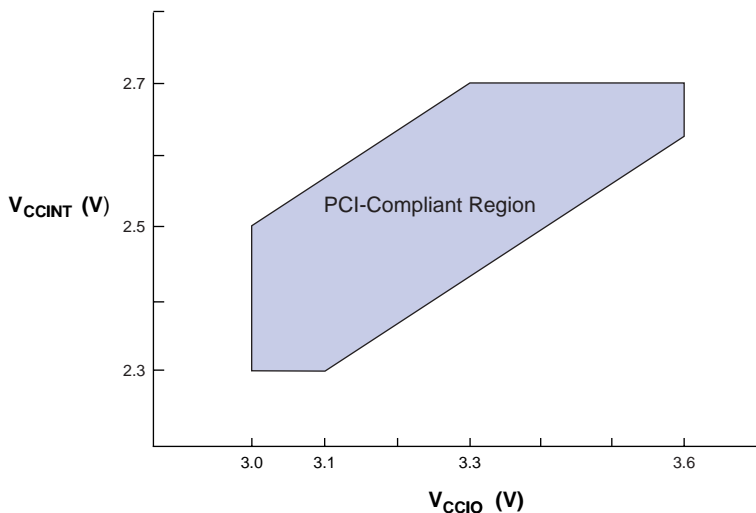
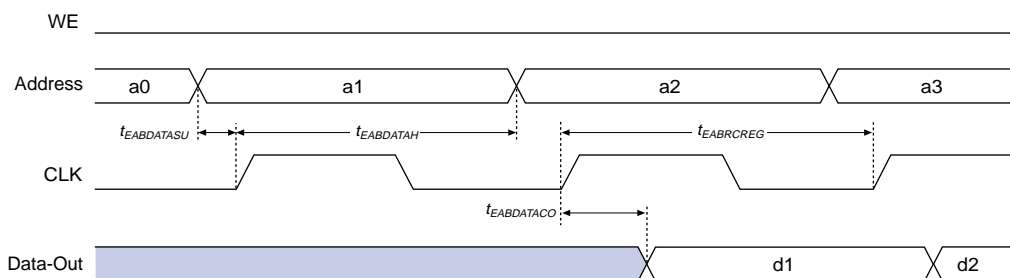
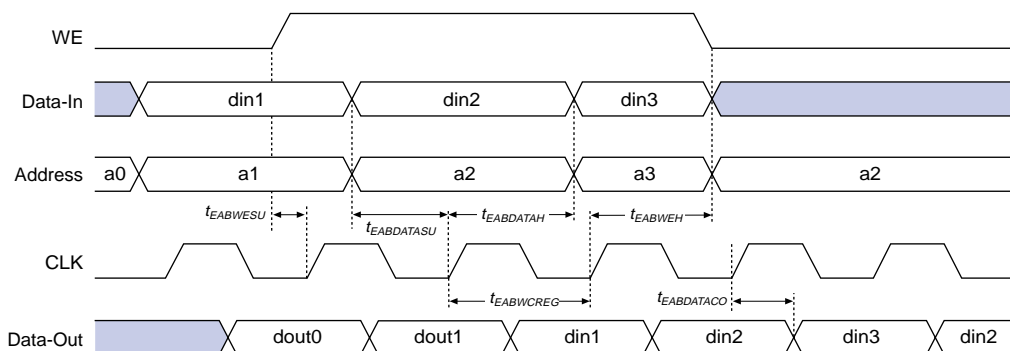


Figure 23 shows the typical output drive characteristics of FLEX 10KE devices with 3.3-V and 2.5-V V_{CCIO} . The output driver is compliant to the 3.3-V **PCI Local Bus Specification, Revision 2.2** (when V_{CCIO} pins are connected to 3.3 V). FLEX 10KE devices with a -1 speed grade also comply with the drive strength requirements of the **PCI Local Bus Specification, Revision 2.2** (when V_{CCINT} pins are powered with a minimum supply of 2.375 V, and V_{CCIO} pins are connected to 3.3 V). Therefore, these devices can be used in open 5.0-V PCI systems.

Figure 30. EAB Synchronous Timing Waveforms

EAB Synchronous Read**EAB Synchronous Write (EAB Output Registers Used)**

Tables 31 through 37 show EPF10K30E device internal and external timing parameters.

Table 31. EPF10K30E Device LE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.7		0.8		1.1	ns
t_{CLUT}		0.5		0.6		0.8	ns
t_{RLUT}		0.6		0.7		1.0	ns
t_{PACKED}		0.3		0.4		0.5	ns
t_{EN}		0.6		0.8		1.0	ns
t_{CICO}		0.1		0.1		0.2	ns
t_{CGEN}		0.4		0.5		0.7	ns

Table 35. EPF10K30E Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		1.8		2.4		2.9	ns
t_{DIN2LE}		1.5		1.8		2.4	ns
$t_{DIN2DATA}$		1.5		1.8		2.2	ns
$t_{DCLK2IOE}$		2.2		2.6		3.0	ns
$t_{DCLK2LE}$		1.5		1.8		2.4	ns
$t_{SAMELAB}$		0.1		0.2		0.3	ns
$t_{SAMEROW}$		2.0		2.4		2.7	ns
$t_{SAMECOLUMN}$		0.7		1.0		0.8	ns
$t_{DIFFROW}$		2.7		3.4		3.5	ns
$t_{TWOROWS}$		4.7		5.8		6.2	ns
$t_{LEPERIPH}$		2.7		3.4		3.8	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.8		0.8		1.1	ns

Table 36. EPF10K30E External Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DDR}		8.0		9.5		12.5	ns
t_{INSU} (3)	2.1		2.5		3.9		ns
t_{INH} (3)	0.0		0.0		0.0		ns
t_{OUTCO} (3)	2.0	4.9	2.0	5.9	2.0	7.6	ns
t_{INSU} (4)	1.1		1.5		—		ns
t_{INH} (4)	0.0		0.0		—		ns
t_{OUTCO} (4)	0.5	3.9	0.5	4.9	—	—	ns
t_{PCISU}	3.0		4.2		—		ns
t_{PCIH}	0.0		0.0		—		ns
t_{PCICO}	2.0	6.0	2.0	7.5	—	—	ns

Table 56. EPF10K130E Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		2.8		3.5		4.4	ns
t_{DIN2LE}		0.7		1.2		1.6	ns
$t_{DIN2DATA}$		1.6		1.9		2.2	ns
$t_{DCLK2IOE}$		1.6		2.1		2.7	ns
$t_{DCLK2LE}$		0.7		1.2		1.6	ns
$t_{SAMELAB}$		0.1		0.2		0.2	ns
$t_{SAMEROW}$		1.9		3.4		5.1	ns
$t_{SAMECOLUMN}$		0.9		2.6		4.4	ns
$t_{DIFFROW}$		2.8		6.0		9.5	ns
$t_{TWOROWS}$		4.7		9.4		14.6	ns
$t_{LEPERIPH}$		3.1		4.7		6.9	ns
$t_{LABCARRY}$		0.6		0.8		1.0	ns
$t_{LABCASC}$		0.9		1.2		1.6	ns

Table 57. EPF10K130E External Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		9.0		12.0		16.0	ns
t_{INSU} (3)	1.9		2.1		3.0		ns
t_{INH} (3)	0.0		0.0		0.0		ns
t_{OUTCO} (3)	2.0	5.0	2.0	7.0	2.0	9.2	ns
t_{INSU} (4)	0.9		1.1		—		ns
t_{INH} (4)	0.0		0.0		—		ns
t_{OUTCO} (4)	0.5	4.0	0.5	6.0	—	—	ns
t_{PCISU}	3.0		6.2		—		ns
t_{PCIH}	0.0		0.0		—		ns
t_{PCICO}	2.0	6.0	2.0	6.9	—	—	ns

Table 58. EPF10K130E External Bidirectional Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$ (3)	2.2		2.4		3.2		ns
t_{INHBIDIR} (3)	0.0		0.0		0.0		ns
$t_{\text{INSUBIDIR}}$ (4)	2.8		3.0		—		ns
t_{INHBIDIR} (4)	0.0		0.0		—		ns
$t_{\text{OUTCOBIDIR}}$ (3)	2.0	5.0	2.0	7.0	2.0	9.2	ns
t_{XZBIDIR} (3)		5.6		8.1		10.8	ns
t_{XZBIDIR} (3)		5.6		8.1		10.8	ns
$t_{\text{OUTCOBIDIR}}$ (4)	0.5	4.0	0.5	6.0	—	—	ns
t_{XZBIDIR} (4)		4.6		7.1		—	ns
t_{XZBIDIR} (4)		4.6		7.1		—	ns

Notes to tables:

- (1) All timing parameters are described in Tables 24 through 30 in this data sheet.
- (2) These parameters are specified by characterization.
- (3) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
- (4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 59 through 65 show EPF10K200E device internal and external timing parameters.

Table 59. EPF10K200E Device LE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.7		0.8		1.2	ns
t_{CLUT}		0.4		0.5		0.6	ns
t_{RLUT}		0.6		0.7		0.9	ns
t_{PACKED}		0.3		0.5		0.7	ns
t_{EN}		0.4		0.5		0.6	ns
t_{CICO}		0.2		0.2		0.3	ns
t_{CGEN}		0.4		0.4		0.6	ns
t_{CGENR}		0.2		0.2		0.3	ns
t_{CASC}		0.7		0.8		1.2	ns
t_{C}		0.5		0.6		0.8	ns
t_{CO}		0.5		0.6		0.8	ns
t_{COMB}		0.4		0.6		0.8	ns
t_{SU}	0.4		0.6		0.7		ns

Table 59. EPF10K200E Device LE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_H	0.9		1.1		1.5		ns
t_{PRE}		0.5		0.6		0.8	ns
t_{CLR}		0.5		0.6		0.8	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns

Table 60. EPF10K200E Device IOE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{IOD}		1.6		1.9		2.6	ns
t_{IOC}		0.3		0.3		0.5	ns
t_{IOCO}		1.6		1.9		2.6	ns
t_{IOCOMB}		0.5		0.6		0.8	ns
t_{IOSU}	0.8		0.9		1.2		ns
t_{IOH}	0.7		0.8		1.1		ns
t_{IOCLR}		0.2		0.2		0.3	ns
t_{OD1}		0.6		0.7		0.9	ns
t_{OD2}		0.1		0.2		0.7	ns
t_{OD3}		2.5		3.0		3.9	ns
t_{XZ}		4.4		5.3		7.1	ns
t_{ZX1}		4.4		5.3		7.1	ns
t_{ZX2}		3.9		4.8		6.9	ns
t_{ZX3}		6.3		7.6		10.1	ns
t_{INREG}		4.8		5.7		7.7	ns
t_{IOFD}		1.5		1.8		2.4	ns
t_{INCOMB}		1.5		1.8		2.4	ns

Table 68. EPF10K50S Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.7		2.4		3.2	ns
$t_{EABDATA2}$		0.4		0.6		0.8	ns
t_{EABWE1}		1.0		1.4		1.9	ns
t_{EABWE2}		0.0		0.0		0.0	ns
t_{EABRE1}		0.0		0.0		0.0	
t_{EABRE2}		0.4		0.6		0.8	
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.8		1.1		1.5	ns
$t_{EABYPASS}$		0.0		0.0		0.0	ns
t_{EABSU}	0.7		1.0		1.3		ns
t_{EABH}	0.4		0.6		0.8		ns
t_{EABCLR}	0.8		1.1		1.5		
t_{AA}		2.0		2.8		3.8	ns
t_{WP}	2.0		2.8		3.8		ns
t_{RP}	1.0		1.4		1.9		
t_{WDSU}	0.5		0.7		0.9		ns
t_{WDH}	0.1		0.1		0.2		ns
t_{WASU}	1.0		1.4		1.9		ns
t_{WAH}	1.5		2.1		2.9		ns
t_{RASU}	1.5		2.1		2.8		
t_{RAH}	0.1		0.1		0.2		
t_{WO}		2.1		2.9		4.0	ns
t_{DD}		2.1		2.9		4.0	ns
t_{EABOUT}		0.0		0.0		0.0	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	1.5		2.0		2.5		ns

During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

SRAM configuration elements allow FLEX 10KE devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 85 ms and can be used to reconfigure an entire system dynamically. In-field upgrades can be performed by distributing new configuration files.

Before and during configuration, all I/O pins (except dedicated inputs, clock, or configuration pins) are pulled high by a weak pull-up resistor.

Programming Files

Despite being function- and pin-compatible, FLEX 10KE devices are not programming- or configuration file-compatible with FLEX 10K or FLEX 10KA devices. A design therefore must be recompiled before it is transferred from a FLEX 10K or FLEX 10KA device to an equivalent FLEX 10KE device. This recompilation should be performed both to create a new programming or configuration file and to check design timing in FLEX 10KE devices, which has different timing characteristics than FLEX 10K or FLEX 10KA devices.

FLEX 10KE devices are generally pin-compatible with equivalent FLEX 10KA devices. In some cases, FLEX 10KE devices have fewer I/O pins than the equivalent FLEX 10KA devices. [Table 81](#) shows which FLEX 10KE devices have fewer I/O pins than equivalent FLEX 10KA devices. However, power, ground, JTAG, and configuration pins are the same on FLEX 10KA and FLEX 10KE devices, enabling migration from a FLEX 10KA design to a FLEX 10KE design.