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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

| | |
|--------------------------------|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 216 |
| Number of Logic Elements/Cells | 1728 |
| Total RAM Bits | 24576 |
| Number of I/O | 220 |
| Number of Gates | 119000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 484-BBGA |
| Supplier Device Package | 484-FBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epf10k30efc484-2 |

Similar to the FLEX 10KE architecture, embedded gate arrays are the fastest-growing segment of the gate array market. As with standard gate arrays, embedded gate arrays implement general logic in a conventional “sea-of-gates” architecture. Additionally, embedded gate arrays have dedicated die areas for implementing large, specialized functions. By embedding functions in silicon, embedded gate arrays reduce die area and increase speed when compared to standard gate arrays. While embedded megafunctions typically cannot be customized, FLEX 10KE devices are programmable, providing the designer with full control over embedded megafunctions and general logic, while facilitating iterative design changes during debugging.

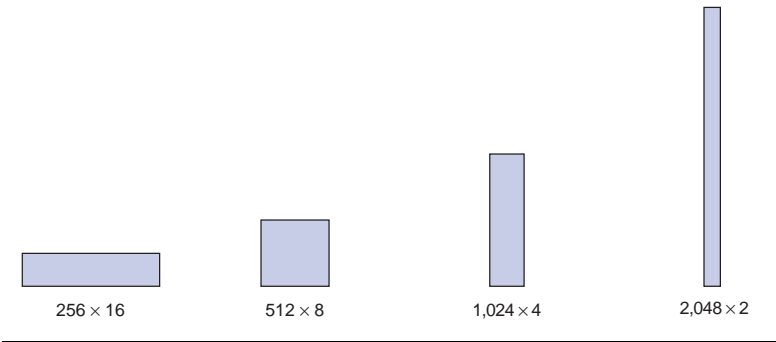
Each FLEX 10KE device contains an embedded array and a logic array. The embedded array is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), wide data-path manipulation, microcontroller applications, and data-transformation functions. The logic array performs the same function as the sea-of-gates in the gate array and is used to implement general logic such as counters, adders, state machines, and multiplexers. The combination of embedded and logic arrays provides the high performance and high density of embedded gate arrays, enabling designers to implement an entire system on a single device.

FLEX 10KE devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers the EPC1, EPC2, and EPC16 configuration devices, which configure FLEX 10KE devices via a serial data stream. Configuration data can also be downloaded from system RAM or via the Altera BitBlaster™, ByteBlasterMV™, or MasterBlaster download cables. After a FLEX 10KE device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 85 ms, real-time changes can be made during system operation.

FLEX 10KE devices contain an interface that permits microprocessors to configure FLEX 10KE devices serially or in-parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat a FLEX 10KE device as memory and configure it by writing to a virtual memory location, making it easy to reconfigure the device.

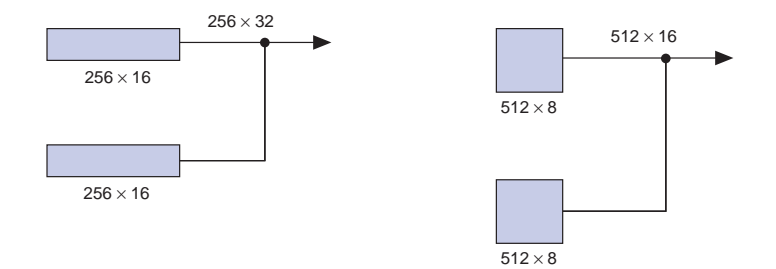
When used as RAM, each EAB can be configured in any of the following sizes: 256×16 , 512×8 , $1,024 \times 4$, or $2,048 \times 2$ (see [Figure 5](#)).

Figure 5. FLEX 10KE EAB Memory Configurations



Larger blocks of RAM are created by combining multiple EABs. For example, two 256×16 RAM blocks can be combined to form a 256×32 block; two 512×8 RAM blocks can be combined to form a 512×16 block (see [Figure 6](#)).

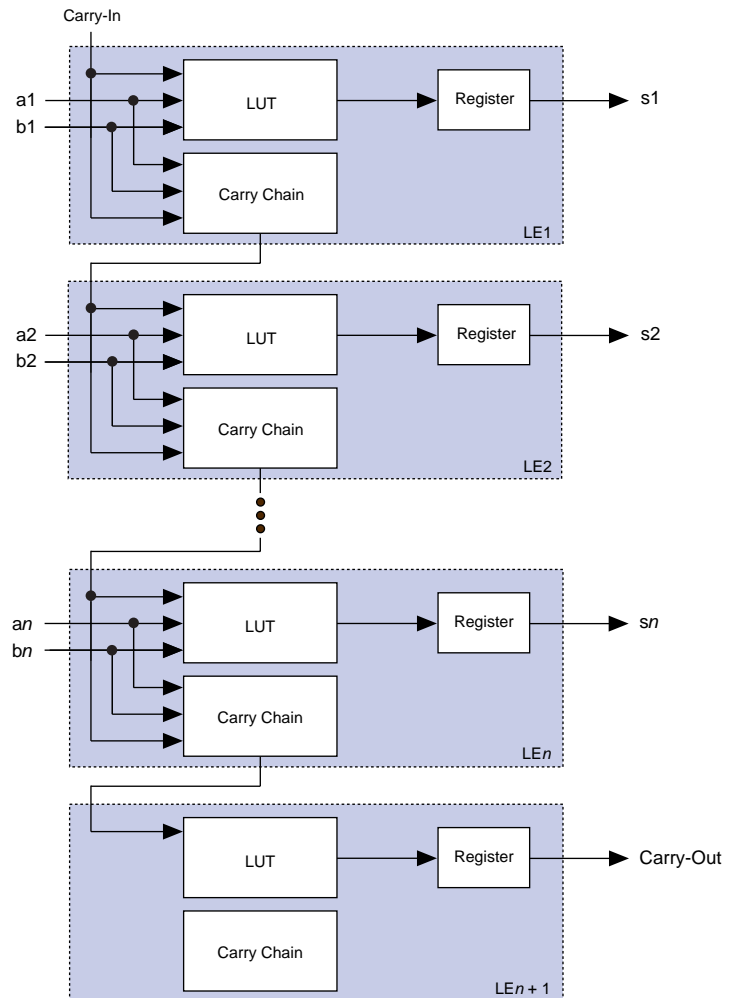
Figure 6. Examples of Combining FLEX 10KE EABs



If necessary, all EABs in a device can be cascaded to form a single RAM block. EABs can be cascaded to form RAM blocks of up to 2,048 words without impacting timing. The Altera software automatically combines EABs to meet a designer's RAM specifications.

Figure 9 shows how an n -bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for an accumulator function. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal.

Figure 9. FLEX 10KE Carry Chain Operation (n -Bit Full Adder)



LE Operating Modes

The FLEX 10KE LE can operate in the following four modes:

- Normal mode
- Arithmetic mode
- Up/down counter mode
- Clearable counter mode

Each of these modes uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. Three inputs to the LE provide clock, clear, and preset control for the register. The Altera software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that use a specific LE operating mode for optimal performance.

The architecture provides a synchronous clock enable to the register in all four modes. The Altera software can set `DATA1` to enable the register synchronously, providing easy implementation of fully synchronous designs.

FastTrack Interconnect Routing Structure

In the FLEX 10KE architecture, connections between LEs, EABs, and device I/O pins are provided by the FastTrack Interconnect routing structure, which is a series of continuous horizontal and vertical routing channels that traverses the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect routing structure consists of row and column interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect. The row interconnect can drive I/O pins and feed other LABs in the row. The column interconnect routes signals between rows and can drive I/O pins.

Row channels drive into the LAB or EAB local interconnect. The row signal is buffered at every LAB or EAB to reduce the effect of fan-out on delay. A row channel can be driven by an LE or by one of three column channels. These four signals feed dual 4-to-1 multiplexers that connect to two specific row channels. These multiplexers, which are connected to each LE, allow column channels to drive row channels even when all eight LEs in a LAB drive the row interconnect.

Each column of LABs or EABs is served by a dedicated column interconnect. The column interconnect that serves the EABs has twice as many channels as other column interconnects. The column interconnect can then drive I/O pins or another row's interconnect to route the signals to other LABs or EABs in the device. A signal from the column interconnect, which can be either the output of a LE or an input from an I/O pin, must be routed to the row interconnect before it can enter a LAB or EAB. Each row channel that is driven by an IOE or EAB can drive one specific column channel.

Access to row and column channels can be switched between LEs in adjacent pairs of LABs. For example, a LE in one LAB can drive the row and column channels normally driven by a particular LE in the adjacent LAB in the same row, and vice versa. This flexibility enables routing resources to be used more efficiently (see [Figure 13](#)).

Column-to-IOE Connections

When an IOE is used as an input, it can drive up to two separate column channels. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the column channels. Two IOEs connect to each side of the column channels. Each IOE can be driven by column channels via a multiplexer. The set of column channels is different for each IOE (see Figure 17).

Figure 17. FLEX 10KE Column-to-IOE Connections

The values for *m* and *n* are provided in Table 11.

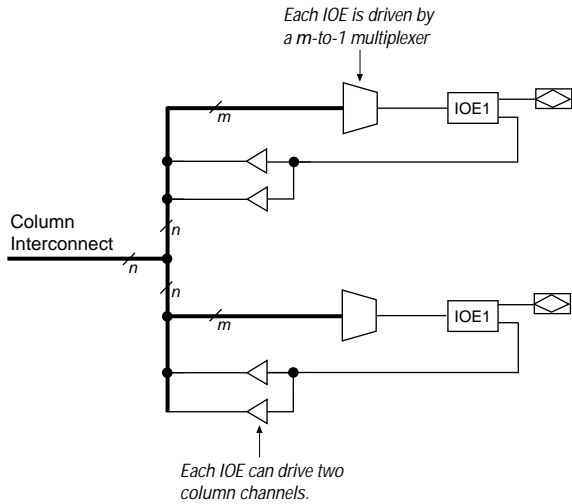


Table 11 lists the FLEX 10KE column-to-IOE interconnect resources.

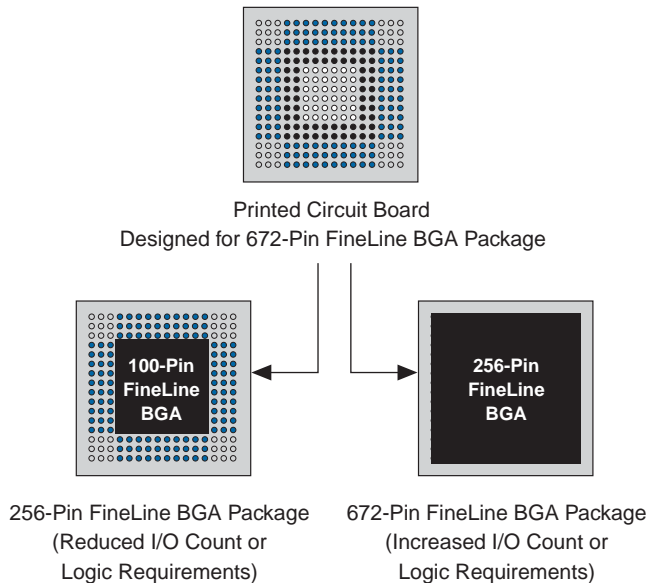
| Table 11. FLEX 10KE Column-to-IOE Interconnect Resources | | |
|--|----------------------------------|--------------------------------------|
| Device | Channels per Column (<i>n</i>) | Column Channels per Pin (<i>m</i>) |
| EPF10K30E | 24 | 16 |
| EPF10K50E EPF10K50S | 24 | 16 |
| EPF10K100E | 24 | 16 |
| EPF10K130E | 32 | 24 |
| EPF10K200E EPF10K200S | 48 | 40 |

SameFrame Pin-Outs

FLEX 10KE devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EPF10K30E device in a 256-pin FineLine BGA package to an EPF10K200S device in a 672-pin FineLine BGA package.

The Altera software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software generates pin-outs describing how to lay out a board to take advantage of this migration (see [Figure 18](#)).

Figure 18. SameFrame Pin-Out Example

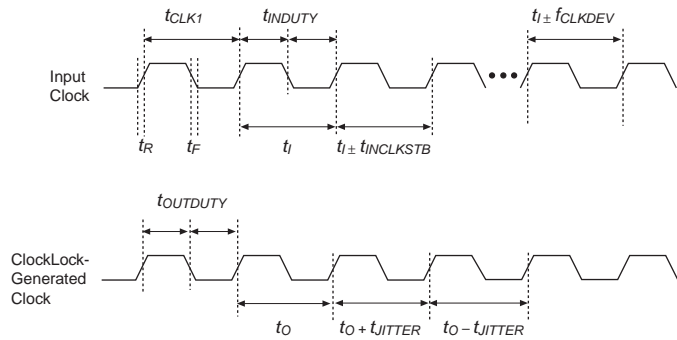


ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. Figure 19 shows the incoming and generated clock specifications.

Figure 19. Specifications for Incoming & Generated Clocks

The t_I parameter refers to the nominal input clock period; the t_O parameter refers to the nominal output clock period.



IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All FLEX 10KE devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. FLEX 10KE devices can also be configured using the JTAG pins through the BitBlaster or ByteBlasterMV download cable, or via hardware that uses the Jam™ STAPL programming and test language. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. FLEX 10KE devices support the JTAG instructions shown in [Table 15](#).

Table 15. FLEX 10KE JTAG Instructions

| JTAG Instruction | Description |
|------------------|--|
| SAMPLE/PRELOAD | Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. |
| EXTEST | Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins. |
| BYPASS | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation. |
| USERCODE | Selects the user electronic signature (USERCODE) register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO. |
| IDCODE | Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO. |
| ICR Instructions | These instructions are used when configuring a FLEX 10KE device via JTAG ports with a BitBlaster or ByteBlasterMV download cable, or using a Jam File (.jam) or Jam Byte-Code File (.jbc) via an embedded processor. |

The instruction register length of FLEX 10KE devices is 10 bits. The USERCODE register length in FLEX 10KE devices is 32 bits; 7 bits are determined by the user, and 25 bits are pre-determined. [Tables 16](#) and [17](#) show the boundary-scan register length and device IDCODE information for FLEX 10KE devices.

Table 16. FLEX 10KE Boundary-Scan Register Length

| Device | Boundary-Scan Register Length |
|--------------------------|-------------------------------|
| EPF10K30E | 690 |
| EPF10K50E EPF10K50S | 798 |
| EPF10K100E | 1,050 |
| EPF10K130E | 1,308 |
| EPF10K200E EPF10K200S | 1,446 |

Table 22. FLEX 10KE 2.5-V Device DC Operating Conditions

Notes (6), (7)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------|---|---|--------------------------------|-----|-----------------------------------|----------------|
| V_{IH} | High-level input voltage | | 1.7, $0.5 \times V_{CCIO}$ (8) | | 5.75 | V |
| V_{IL} | Low-level input voltage | | -0.5 | | 0.8, $0.3 \times V_{CCIO}$ (8) | V |
| V_{OH} | 3.3-V high-level TTL output voltage | $I_{OH} = -8$ mA DC, $V_{CCIO} = 3.00$ V (9) | 2.4 | | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.00$ V (9) | $V_{CCIO} - 0.2$ | | | V |
| | 3.3-V high-level PCI output voltage | $I_{OH} = -0.5$ mA DC, $V_{CCIO} = 3.00$ to 3.60 V (9) | $0.9 \times V_{CCIO}$ | | | V |
| | 2.5-V high-level output voltage | $I_{OH} = -0.1$ mA DC, $V_{CCIO} = 2.30$ V (9) | 2.1 | | | V |
| | | $I_{OH} = -1$ mA DC, $V_{CCIO} = 2.30$ V (9) | 2.0 | | | V |
| | | $I_{OH} = -2$ mA DC, $V_{CCIO} = 2.30$ V (9) | 1.7 | | | V |
| | | | | | | |
| V_{OL} | 3.3-V low-level TTL output voltage | $I_{OL} = 12$ mA DC, $V_{CCIO} = 3.00$ V (10) | | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.00$ V (10) | | | 0.2 | V |
| | 3.3-V low-level PCI output voltage | $I_{OL} = 1.5$ mA DC, $V_{CCIO} = 3.00$ to 3.60 V (10) | | | $0.1 \times V_{CCIO}$ | V |
| | 2.5-V low-level output voltage | $I_{OL} = 0.1$ mA DC, $V_{CCIO} = 2.30$ V (10) | | | 0.2 | V |
| | | $I_{OL} = 1$ mA DC, $V_{CCIO} = 2.30$ V (10) | | | 0.4 | V |
| | | $I_{OL} = 2$ mA DC, $V_{CCIO} = 2.30$ V (10) | | | 0.7 | V |
| | | | | | | |
| I_I | Input pin leakage current | $V_I = V_{CCIOmax}$ to 0 V (11) | -10 | | 10 | μ A |
| I_{OZ} | Tri-stated I/O pin leakage current | $V_O = V_{CCIOmax}$ to 0 V (11) | -10 | | 10 | μ A |
| I_{CC0} | V_{CC} supply current (standby) | $V_I =$ ground, no load, no toggling inputs | | 5 | | mA |
| | | $V_I =$ ground, no load, no toggling inputs (12) | | 10 | | mA |
| R_{CONF} | Value of I/O pin pull-up resistor before and during configuration | $V_{CCIO} = 3.0$ V (13) | 20 | | 50 | $k\frac{3}{4}$ |
| | | $V_{CCIO} = 2.3$ V (13) | 30 | | 80 | $k\frac{3}{4}$ |

Table 23. FLEX 10KE Device Capacitance *Note (14)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-------------|--|---|-----|-----|------|
| C_{IN} | Input capacitance | $V_{IN} = 0\text{ V}$, $f = 1.0\text{ MHz}$ | | 10 | pF |
| C_{INCLK} | Input capacitance on dedicated clock pin | $V_{IN} = 0\text{ V}$, $f = 1.0\text{ MHz}$ | | 12 | pF |
| C_{OUT} | Output capacitance | $V_{OUT} = 0\text{ V}$, $f = 1.0\text{ MHz}$ | | 10 | pF |

Notes to tables:

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input voltage is -0.5 V . During transitions, the inputs may undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns .
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) Maximum V_{CC} rise time is 100 ms , and V_{CC} must rise monotonically.
- (5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
- (6) Typical values are for $T_A = 25^\circ\text{ C}$, $V_{CCINT} = 2.5\text{ V}$, and $V_{CCIO} = 2.5\text{ V}$ or 3.3 V .
- (7) These values are specified under the FLEX 10KE Recommended Operating Conditions shown in [Tables 20 and 21](#).
- (8) The FLEX 10KE input buffers are compatible with 2.5-V , 3.3-V (LVTTTL and LVCMOS), and 5.0-V TTL and CMOS signals. Additionally, the input buffers are 3.3-V PCI compliant when V_{CCIO} and V_{CCINT} meet the relationship shown in [Figure 22](#).
- (9) The I_{OH} parameter refers to high-level TTL, PCI, or CMOS output current.
- (10) The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
- (11) This value is specified for normal device operation. The value may vary during power-up.
- (12) This parameter applies to -1 speed-grade commercial-temperature devices and -2 speed-grade-industrial temperature devices.
- (13) Pin pull-up resistance values will be lower if the pin is driven higher than V_{CCIO} by an external source.
- (14) Capacitance is sample-tested only.

Figure 22 shows the required relationship between V_{CCIO} and V_{CCINT} for 3.3-V PCI compliance.

Figure 22. Relationship between V_{CCIO} & V_{CCINT} for 3.3-V PCI Compliance

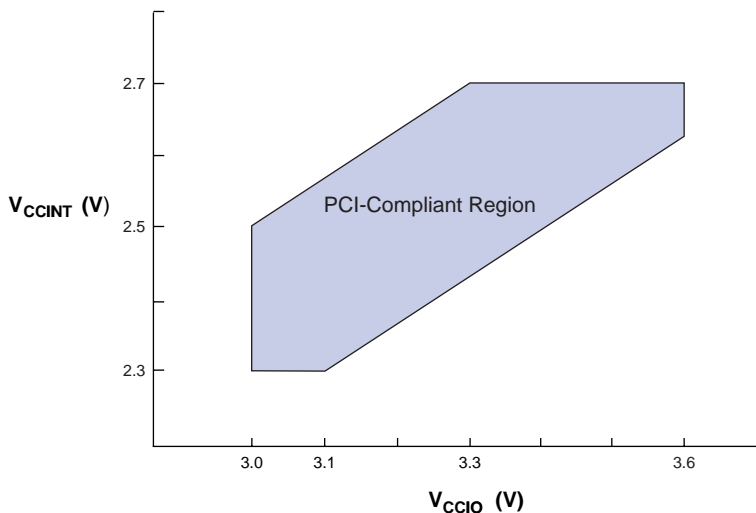


Figure 23 shows the typical output drive characteristics of FLEX 10KE devices with 3.3-V and 2.5-V V_{CCIO} . The output driver is compliant to the 3.3-V **PCI Local Bus Specification, Revision 2.2** (when V_{CCIO} pins are connected to 3.3 V). FLEX 10KE devices with a -1 speed grade also comply with the drive strength requirements of the **PCI Local Bus Specification, Revision 2.2** (when V_{CCINT} pins are powered with a minimum supply of 2.375 V, and V_{CCIO} pins are connected to 3.3 V). Therefore, these devices can be used in open 5.0-V PCI systems.

Table 31. EPF10K30E Device LE Timing Microparameters (Part 2 of 2) *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|-------------|----------------|-----|----------------|-----|----------------|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| t_{CGENR} | | 0.1 | | 0.1 | | 0.2 | ns |
| t_{CASC} | | 0.6 | | 0.8 | | 1.0 | ns |
| t_C | | 0.0 | | 0.0 | | 0.0 | ns |
| t_{CO} | | 0.3 | | 0.4 | | 0.5 | ns |
| t_{COMB} | | 0.4 | | 0.4 | | 0.6 | ns |
| t_{SU} | 0.4 | | 0.6 | | 0.6 | | ns |
| t_H | 0.7 | | 1.0 | | 1.3 | | ns |
| t_{PRE} | | 0.8 | | 0.9 | | 1.2 | ns |
| t_{CLR} | | 0.8 | | 0.9 | | 1.2 | ns |
| t_{CH} | 2.0 | | 2.5 | | 2.5 | | ns |
| t_{CL} | 2.0 | | 2.5 | | 2.5 | | ns |

Table 32. EPF10K30E Device IOE Timing Microparameters *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|--------------|----------------|-----|----------------|-----|----------------|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| t_{IOD} | | 2.4 | | 2.8 | | 3.8 | ns |
| t_{IOC} | | 0.3 | | 0.4 | | 0.5 | ns |
| t_{IOCO} | | 1.0 | | 1.1 | | 1.6 | ns |
| t_{IOCOMB} | | 0.0 | | 0.0 | | 0.0 | ns |
| t_{IOSU} | 1.2 | | 1.4 | | 1.9 | | ns |
| t_{IOH} | 0.3 | | 0.4 | | 0.5 | | ns |
| t_{IOCLR} | | 1.0 | | 1.1 | | 1.6 | ns |
| t_{OD1} | | 1.9 | | 2.3 | | 3.0 | ns |
| t_{OD2} | | 1.4 | | 1.8 | | 2.5 | ns |
| t_{OD3} | | 4.4 | | 5.2 | | 7.0 | ns |
| t_{XZ} | | 2.7 | | 3.1 | | 4.3 | ns |
| t_{ZX1} | | 2.7 | | 3.1 | | 4.3 | ns |
| t_{ZX2} | | 2.2 | | 2.6 | | 3.8 | ns |
| t_{ZX3} | | 5.2 | | 6.0 | | 8.3 | ns |
| t_{INREG} | | 3.4 | | 4.1 | | 5.5 | ns |
| t_{IOFD} | | 0.8 | | 1.3 | | 2.4 | ns |
| t_{INCOMB} | | 0.8 | | 1.3 | | 2.4 | ns |

Table 35. EPF10K30E Device Interconnect Timing Microparameters *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|------------------|----------------|-----|----------------|-----|----------------|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DIN2IOE}$ | | 1.8 | | 2.4 | | 2.9 | ns |
| t_{DIN2LE} | | 1.5 | | 1.8 | | 2.4 | ns |
| $t_{DIN2DATA}$ | | 1.5 | | 1.8 | | 2.2 | ns |
| $t_{DCLK2IOE}$ | | 2.2 | | 2.6 | | 3.0 | ns |
| $t_{DCLK2LE}$ | | 1.5 | | 1.8 | | 2.4 | ns |
| $t_{SAMELAB}$ | | 0.1 | | 0.2 | | 0.3 | ns |
| $t_{SAMEROW}$ | | 2.0 | | 2.4 | | 2.7 | ns |
| $t_{SAMECOLUMN}$ | | 0.7 | | 1.0 | | 0.8 | ns |
| $t_{DIFFROW}$ | | 2.7 | | 3.4 | | 3.5 | ns |
| $t_{TWOROWS}$ | | 4.7 | | 5.8 | | 6.2 | ns |
| $t_{LEPERIPH}$ | | 2.7 | | 3.4 | | 3.8 | ns |
| $t_{LABCARRY}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{LABCASC}$ | | 0.8 | | 0.8 | | 1.1 | ns |

Table 36. EPF10K30E External Timing Parameters *Notes (1), (2)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|-----------------|----------------|-----|----------------|-----|----------------|------|------|
| | Min | Max | Min | Max | Min | Max | |
| t_{DDR} | | 8.0 | | 9.5 | | 12.5 | ns |
| t_{INSU} (3) | 2.1 | | 2.5 | | 3.9 | | ns |
| t_{INH} (3) | 0.0 | | 0.0 | | 0.0 | | ns |
| t_{OUTCO} (3) | 2.0 | 4.9 | 2.0 | 5.9 | 2.0 | 7.6 | ns |
| t_{INSU} (4) | 1.1 | | 1.5 | | — | | ns |
| t_{INH} (4) | 0.0 | | 0.0 | | — | | ns |
| t_{OUTCO} (4) | 0.5 | 3.9 | 0.5 | 4.9 | — | — | ns |
| t_{PCISU} | 3.0 | | 4.2 | | — | | ns |
| t_{PCIH} | 0.0 | | 0.0 | | — | | ns |
| t_{PCICO} | 2.0 | 6.0 | 2.0 | 7.5 | — | — | ns |

Table 61. EPF10K200E Device EAB Internal Microparameters *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|----------------|----------------|-----|----------------|-----|----------------|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 2.0 | | 2.4 | | 3.2 | ns |
| $t_{EABDATA1}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| t_{EABWE1} | | 1.4 | | 1.7 | | 2.3 | ns |
| t_{EABWE2} | | 0.0 | | 0.0 | | 0.0 | ns |
| t_{EABRE1} | | 0 | | 0 | | 0 | ns |
| t_{EABRE2} | | 0.4 | | 0.5 | | 0.6 | ns |
| t_{EABCLK} | | 0.0 | | 0.0 | | 0.0 | ns |
| t_{EABCO} | | 0.8 | | 0.9 | | 1.2 | ns |
| $t_{EABYPASS}$ | | 0.0 | | 0.1 | | 0.1 | ns |
| t_{EABSU} | 0.9 | | 1.1 | | 1.5 | | ns |
| t_{EABH} | 0.4 | | 0.5 | | 0.6 | | ns |
| t_{EABCLR} | 0.8 | | 0.9 | | 1.2 | | ns |
| t_{AA} | | 3.1 | | 3.7 | | 4.9 | ns |
| t_{WP} | 3.3 | | 4.0 | | 5.3 | | ns |
| t_{RP} | 0.9 | | 1.1 | | 1.5 | | ns |
| t_{WDSU} | 0.9 | | 1.1 | | 1.5 | | ns |
| t_{WDH} | 0.1 | | 0.1 | | 0.1 | | ns |
| t_{WASU} | 1.3 | | 1.6 | | 2.1 | | ns |
| t_{WAH} | 2.1 | | 2.5 | | 3.3 | | ns |
| t_{RASU} | 2.2 | | 2.6 | | 3.5 | | ns |
| t_{RAH} | 0.1 | | 0.1 | | 0.2 | | ns |
| t_{WO} | | 2.0 | | 2.4 | | 3.2 | ns |
| t_{DD} | | 2.0 | | 2.4 | | 3.2 | ns |
| t_{EABOUT} | | 0.0 | | 0.1 | | 0.1 | ns |
| t_{EABCH} | 1.5 | | 2.0 | | 2.5 | | ns |
| t_{EABCL} | 3.3 | | 4.0 | | 5.3 | | ns |

Table 62. EPF10K200E Device EAB Internal Timing Macroparameters (Part 1 of 2) *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|----------------|----------------|-----|----------------|-----|----------------|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| t_{EABAA} | | 5.1 | | 6.4 | | 8.4 | ns |
| $t_{EABRCOMB}$ | 5.1 | | 6.4 | | 8.4 | | ns |
| $t_{EABRCREG}$ | 4.8 | | 5.7 | | 7.6 | | ns |
| t_{EABWP} | 3.3 | | 4.0 | | 5.3 | | ns |

Table 66. EPF10K50S Device LE Timing Microparameters (Part 2 of 2) *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|-------------|----------------|-----|----------------|-----|----------------|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| t_{CGENR} | | 0.1 | | 0.1 | | 0.1 | ns |
| t_{CASC} | | 0.5 | | 0.8 | | 1.0 | ns |
| t_C | | 0.5 | | 0.6 | | 0.8 | ns |
| t_{CO} | | 0.6 | | 0.6 | | 0.7 | ns |
| t_{COMB} | | 0.3 | | 0.4 | | 0.5 | ns |
| t_{SU} | 0.5 | | 0.6 | | 0.7 | | ns |
| t_H | 0.5 | | 0.6 | | 0.8 | | ns |
| t_{PRE} | | 0.4 | | 0.5 | | 0.7 | ns |
| t_{CLR} | | 0.8 | | 1.0 | | 1.2 | ns |
| t_{CH} | 2.0 | | 2.5 | | 3.0 | | ns |
| t_{CL} | 2.0 | | 2.5 | | 3.0 | | ns |

Table 67. EPF10K50S Device IOE Timing Microparameters *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|--------------|----------------|-----|----------------|-----|----------------|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| t_{IOD} | | 1.3 | | 1.3 | | 1.9 | ns |
| t_{IOC} | | 0.3 | | 0.4 | | 0.4 | ns |
| t_{IOCO} | | 1.7 | | 2.1 | | 2.6 | ns |
| t_{IOCOMB} | | 0.5 | | 0.6 | | 0.8 | ns |
| t_{IOSU} | 0.8 | | 1.0 | | 1.3 | | ns |
| t_{IOH} | 0.4 | | 0.5 | | 0.6 | | ns |
| t_{IOCLR} | | 0.2 | | 0.2 | | 0.4 | ns |
| t_{OD1} | | 1.2 | | 1.2 | | 1.9 | ns |
| t_{OD2} | | 0.7 | | 0.8 | | 1.7 | ns |
| t_{OD3} | | 2.7 | | 3.0 | | 4.3 | ns |
| t_{XZ} | | 4.7 | | 5.7 | | 7.5 | ns |
| t_{ZX1} | | 4.7 | | 5.7 | | 7.5 | ns |
| t_{ZX2} | | 4.2 | | 5.3 | | 7.3 | ns |
| t_{ZX3} | | 6.2 | | 7.5 | | 9.9 | ns |
| t_{INREG} | | 3.5 | | 4.2 | | 5.6 | ns |
| t_{IOFD} | | 1.1 | | 1.3 | | 1.8 | ns |
| t_{INCOMB} | | 1.1 | | 1.3 | | 1.8 | ns |

Table 76. EPF10K200S Device EAB Internal Timing Macroparameters *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|-----------------|----------------|-----|----------------|-----|----------------|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| t_{EABAA} | | 3.9 | | 6.4 | | 8.4 | ns |
| $t_{EABRCOMB}$ | 3.9 | | 6.4 | | 8.4 | | ns |
| $t_{EABRCREG}$ | 3.6 | | 5.7 | | 7.6 | | ns |
| t_{EABWP} | 2.1 | | 4.0 | | 5.3 | | ns |
| $t_{EABWCOMB}$ | 4.8 | | 8.1 | | 10.7 | | ns |
| $t_{EABWCREG}$ | 5.4 | | 8.0 | | 10.6 | | ns |
| t_{EABDD} | | 3.8 | | 5.1 | | 6.7 | ns |
| $t_{EABDATACO}$ | | 0.8 | | 1.0 | | 1.3 | ns |
| $t_{EABDATASU}$ | 1.1 | | 1.6 | | 2.1 | | ns |
| $t_{EABDATAH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWESU}$ | 0.7 | | 1.1 | | 1.5 | | ns |
| t_{EABWEH} | 0.4 | | 0.5 | | 0.6 | | ns |
| $t_{EABWDSU}$ | 1.2 | | 1.8 | | 2.4 | | ns |
| t_{EABWDH} | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWASU}$ | 1.9 | | 3.6 | | 4.7 | | ns |
| t_{EABWAH} | 0.8 | | 0.5 | | 0.7 | | ns |
| t_{EABWO} | | 3.1 | | 4.4 | | 5.8 | ns |

Table 77. EPF10K200S Device Interconnect Timing Microparameters (Part 1 of 2) *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|------------------|----------------|-----|----------------|------|----------------|------|------|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DIN2IOE}$ | | 4.4 | | 4.8 | | 5.5 | ns |
| t_{DIN2LE} | | 0.6 | | 0.6 | | 0.9 | ns |
| $t_{DIN2DATA}$ | | 1.8 | | 2.1 | | 2.8 | ns |
| $t_{DCLK2IOE}$ | | 1.7 | | 2.0 | | 2.8 | ns |
| $t_{DCLK2LE}$ | | 0.6 | | 0.6 | | 0.9 | ns |
| $t_{SAMELAB}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{SAMEROW}$ | | 3.0 | | 4.6 | | 5.7 | ns |
| $t_{SAMECOLUMN}$ | | 3.5 | | 4.9 | | 6.4 | ns |
| $t_{DIFFROW}$ | | 6.5 | | 9.5 | | 12.1 | ns |
| $t_{TWOROWS}$ | | 9.5 | | 14.1 | | 17.8 | ns |
| $t_{LEPERIPH}$ | | 5.5 | | 6.2 | | 7.2 | ns |
| $t_{LABCARRY}$ | | 0.3 | | 0.1 | | 0.2 | ns |

Table 77. EPF10K200S Device Interconnect Timing Microparameters (Part 2 of 2) *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---------------|----------------|-----|----------------|-----|----------------|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| $t_{LABCASC}$ | | 0.5 | | 1.0 | | 1.4 | ns |

Table 78. EPF10K200S External Timing Parameters *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|-------------------|----------------|-----|----------------|------|----------------|------|------|
| | Min | Max | Min | Max | Min | Max | |
| t_{DRR} | | 9.0 | | 12.0 | | 16.0 | ns |
| $t_{INSU}^{(2)}$ | 3.1 | | 3.7 | | 4.7 | | ns |
| $t_{INH}^{(2)}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}^{(2)}$ | 2.0 | 3.7 | 2.0 | 4.4 | 2.0 | 6.3 | ns |
| $t_{INSU}^{(3)}$ | 2.1 | | 2.7 | | — | | ns |
| $t_{INH}^{(3)}$ | 0.0 | | 0.0 | | — | | ns |
| $t_{OUTCO}^{(3)}$ | 0.5 | 2.7 | 0.5 | 3.4 | — | — | ns |
| t_{PCISU} | 3.0 | | 4.2 | | — | | ns |
| t_{PCIH} | 0.0 | | 0.0 | | — | | ns |
| t_{PCICO} | 2.0 | 6.0 | 2.0 | 8.9 | — | — | ns |

Table 79. EPF10K200S External Bidirectional Timing Parameters *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|------------------------|----------------|-----|----------------|-----|----------------|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}^{(2)}$ | 2.3 | | 3.4 | | 4.4 | | ns |
| $t_{INHBIDIR}^{(2)}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSUBIDIR}^{(3)}$ | 3.3 | | 4.4 | | — | | ns |
| $t_{INHBIDIR}^{(3)}$ | 0.0 | | 0.0 | | — | | ns |
| $t_{OUTCOBIDIR}^{(2)}$ | 2.0 | 3.7 | 2.0 | 4.4 | 2.0 | 6.3 | ns |
| $t_{XZBIDIR}^{(2)}$ | | 6.9 | | 7.6 | | 9.2 | ns |
| $t_{ZXBIDIR}^{(2)}$ | | 5.9 | | 6.6 | | — | ns |
| $t_{OUTCOBIDIR}^{(3)}$ | 0.5 | 2.7 | 0.5 | 3.4 | — | — | ns |
| $t_{XZBIDIR}^{(3)}$ | | 6.9 | | 7.6 | | 9.2 | ns |
| $t_{ZXBIDIR}^{(3)}$ | | 5.9 | | 6.6 | | — | ns |

Notes to tables:

- (1) All timing parameters are described in Tables 24 through 30 in this data sheet.
 (2) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
 (3) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

SRAM configuration elements allow FLEX 10KE devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 85 ms and can be used to reconfigure an entire system dynamically. In-field upgrades can be performed by distributing new configuration files.

Before and during configuration, all I/O pins (except dedicated inputs, clock, or configuration pins) are pulled high by a weak pull-up resistor.

Programming Files

Despite being function- and pin-compatible, FLEX 10KE devices are not programming- or configuration file-compatible with FLEX 10K or FLEX 10KA devices. A design therefore must be recompiled before it is transferred from a FLEX 10K or FLEX 10KA device to an equivalent FLEX 10KE device. This recompilation should be performed both to create a new programming or configuration file and to check design timing in FLEX 10KE devices, which has different timing characteristics than FLEX 10K or FLEX 10KA devices.

FLEX 10KE devices are generally pin-compatible with equivalent FLEX 10KA devices. In some cases, FLEX 10KE devices have fewer I/O pins than the equivalent FLEX 10KA devices. [Table 81](#) shows which FLEX 10KE devices have fewer I/O pins than equivalent FLEX 10KA devices. However, power, ground, JTAG, and configuration pins are the same on FLEX 10KA and FLEX 10KE devices, enabling migration from a FLEX 10KA design to a FLEX 10KE design.

Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the Altera Digital Library for pin-out information.

Revision History

The information contained in the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.5 supersedes information published in previous versions.

Version 2.5

The following changes were made to the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.5:

- *Note (1)* added to **Figure 23**.
- Text added to “**I/O Element**” section on **page 34**.
- Updated **Table 22**.

Version 2.4

The following changes were made to the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.4: updated text on **page 34** and **page 63**.