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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 216 |
| Number of Logic Elements/Cells | 1728 |
| Total RAM Bits | 24576 |
| Number of I/O | 102 |
| Number of Gates | 119000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epf10k30eti144-3 |

For more information on FLEX device configuration, see the following documents:

- *Configuration Devices for APEX & FLEX Devices Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *MasterBlaster Download Cable Data Sheet*
- *Application Note 116 (Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices)*

FLEX 10KE devices are supported by the Altera development systems, which are integrated packages that offer schematic, text (including AHDL), and waveform design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, and device configuration. The Altera software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The Altera software works easily with common gate array EDA tools for synthesis and simulation. For example, the Altera software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the Altera software contains EDA libraries that use device-specific features such as carry chains, which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the Altera development system includes DesignWare functions that are optimized for the FLEX 10KE architecture.

The Altera development system runs on Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800.

See the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet* for more information.

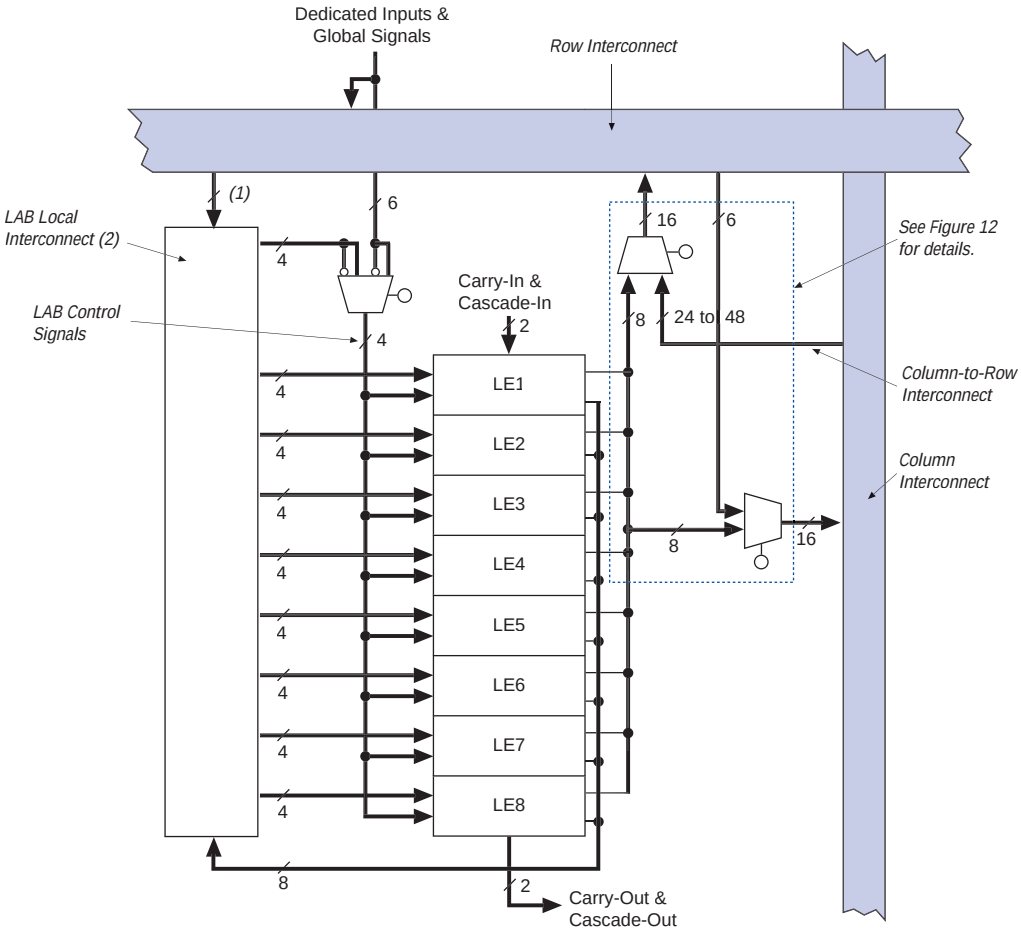
EABs provide flexible options for driving and controlling clock signals. Different clocks and clock enables can be used for reading and writing to the EAB. Registers can be independently inserted on the data input, EAB output, write address, write enable signals, read address, and read enable signals. The global signals and the EAB local interconnect can drive write enable, read enable, and clock enable signals. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control write enable, read enable, clear, clock, and clock enable signals.

An EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs (see Figures 2 and 4). The column interconnect, which is adjacent to the EAB, has twice as many channels as other columns in the device.

## Logic Array Block

An LAB consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure to the FLEX 10KE architecture, facilitating efficient routing with optimum device utilization and high performance (see Figure 7).

*Figure 7. FLEX 10KE LAB*



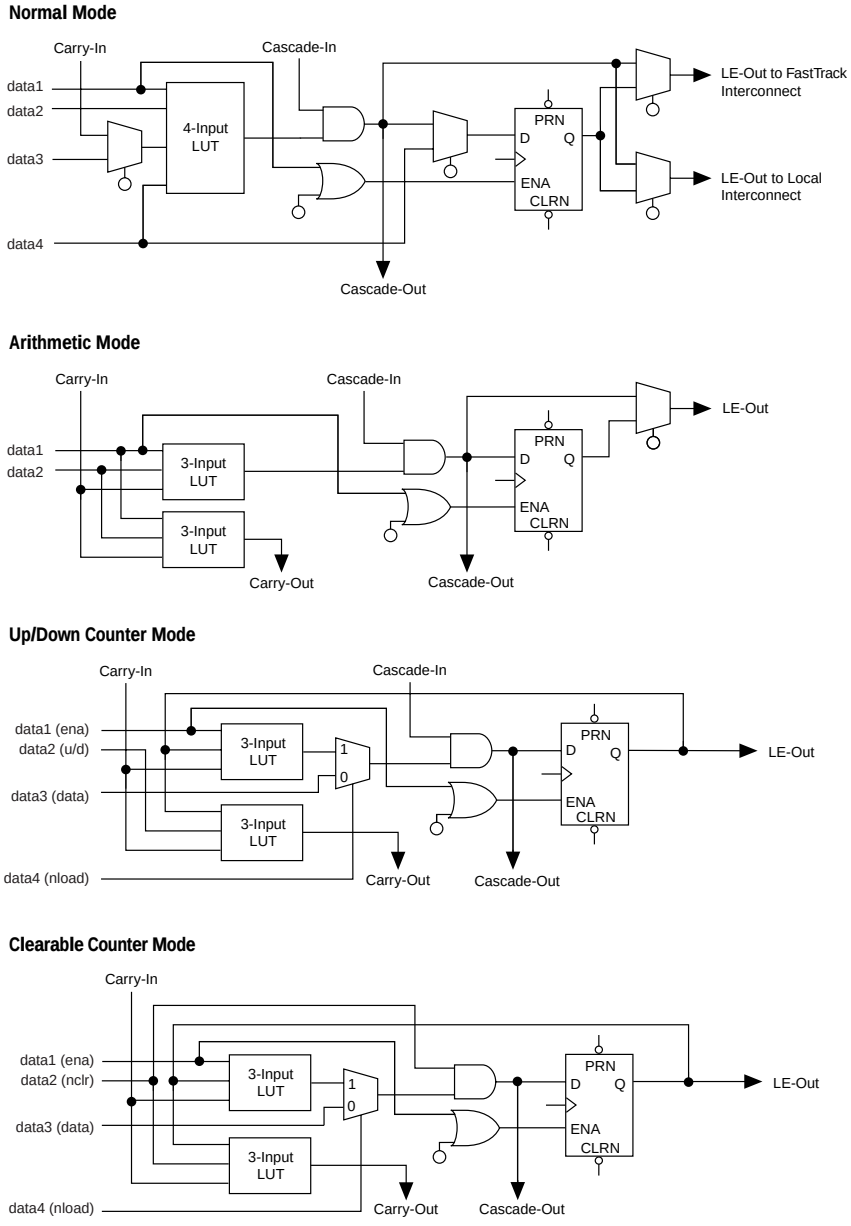

***Notes:***

(1) EPF10K30E, EPF10K50E, and EPF10K50S devices have 22 inputs to the LAB local interconnect channel from the row; EPF10K100E, EPF10K130E, EPF10K200E, and EPF10K200S devices have 26.

(2) EPF10K30E, EPF10K50E, and EPF10K50S devices have 30 LAB local interconnect channels; EPF10K100E, EPF10K130E, EPF10K200E, and EPF10K200S devices have 34.

Figure 11 shows the LE operating modes.

*Figure 11. FLEX 10KE LE Operating Modes*



### *Row-to-IOE Connections*

When an IOE is used as an input signal, it can drive two separate row channels. The signal is accessible by all LEs within that row. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the row channels. Up to eight IOEs connect to each side of each row channel (see Figure 16).

***Figure 16. FLEX 10KE Row-to-IOE Connections***

*The values for m and n are provided in Table 10.*

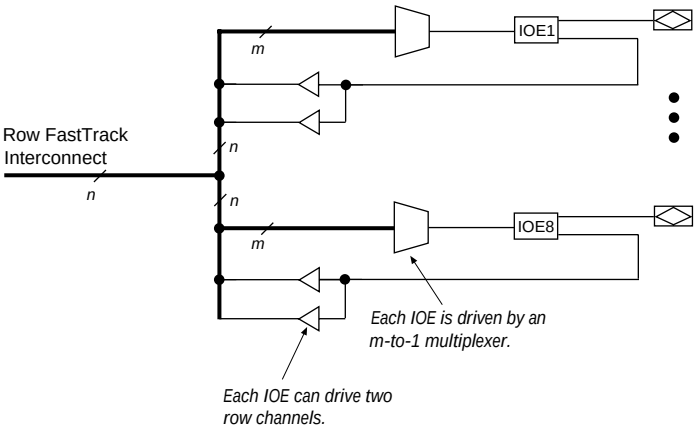



Table 10 lists the FLEX 10KE row-to-IOE interconnect resources.

***Table 10. FLEX 10KE Row-to-IOE Interconnect Resources***

| Device | Channels per Row *(n)* | Row Channels per Pin *(m)* |
|---|---|---|
| EPF10K30E | 216 | 27 |
| EPF10K50E<br>EPF10K50S | 216 | 27 |
| EPF10K100E | 312 | 39 |
| EPF10K130E | 312 | 39 |
| EPF10K200E<br>EPF10K200S | 312 | 39 |

## PCI Pull-Up Clamping Diode Option

FLEX 10KE devices have a pull-up clamping diode on every I/O, dedicated input, and dedicated clock pin. PCI clamping diodes clamp the signal to the $V_{CCIO}$ value and are required for 3.3-V PCI compliance. Clamping diodes can also be used to limit overshoot in other systems.

Clamping diodes are controlled on a pin-by-pin basis. When $V_{CCIO}$ is 3.3 V, a pin that has the clamping diode option turned on can be driven by a 2.5-V or 3.3-V signal, but not a 5.0-V signal. When $V_{CCIO}$ is 2.5 V, a pin that has the clamping diode option turned on can be driven by a 2.5-V signal, but not a 3.3-V or 5.0-V signal. Additionally, a clamping diode can be activated for a subset of pins, which would allow a device to bridge between a 3.3-V PCI bus and a 5.0-V device.

## Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces system noise and adds a maximum delay of 4.3 ns. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate pin-by-pin or assign a default slew rate to all pins on a device-wide basis. The slow slew rate setting affects the falling edge of the output.

## Open-Drain Output Option

FLEX 10KE devices provide an optional open-drain output (electrically equivalent to open-collector output) for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

## MultiVolt I/O Interface

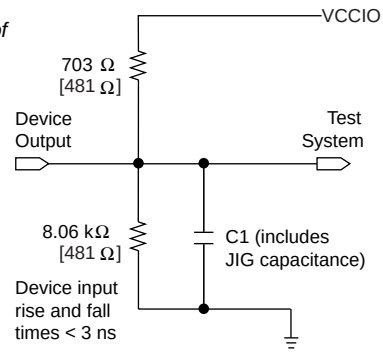
The FLEX 10KE device architecture supports the MultiVolt I/O interface feature, which allows FLEX 10KE devices in all packages to interface with systems of differing supply voltages. These devices have one set of $V_{CC}$ pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

## Generic Testing

Each FLEX 10KE device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for FLEX 10KE devices are made under conditions equivalent to those shown in Figure 21. Multiple test patterns can be used to configure devices during all stages of the production flow.

***Figure 21. FLEX 10KE AC Test Conditions***

*Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V devices or outputs. Numbers without brackets are for 3.3-V. devices or outputs.*




## Operating Conditions

Tables 19 through 23 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V FLEX 10KE devices.

***Table 19. FLEX 10KE 2.5-V Device Absolute Maximum Ratings*** *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage | With respect to ground *(2)* | –0.5 | 3.6 | V |
| $V_{CCIO}$ | | | –0.5 | 4.6 | V |
| $V_I$ | DC input voltage | | –2.0 | 5.75 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | PQFP, TQFP, BGA, and FineLine BGA packages, under bias | | 135 | ° C |
| | | Ceramic PGA packages, under bias | | 150 | ° C |

*Table 20. 2.5-V EPF10K50E & EPF10K200E Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3)*, *(4)* | 2.30 (2.30) | 2.70 (2.70) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(3)*, *(4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(3)*, *(4)* | 2.30 (2.30) | 2.70 (2.70) | V |
| $V_I$ | Input voltage | *(5)* | –0.5 | 5.75 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient temperature | For commercial use | 0 | 70 | ° C |
| | | For industrial use | –40 | 85 | ° C |
| $T_J$ | Operating temperature | For commercial use | 0 | 85 | ° C |
| | | For industrial use | –40 | 100 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

*Table 21. 2.5-V EPF10K30E, EPF10K50S, EPF10K100E, EPF10K130E & EPF10K200S Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3)*, *(4)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(3)*, *(4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(3)*, *(4)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_I$ | Input voltage | *(5)* | –0.5 | 5.75 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient temperature | For commercial use | 0 | 70 | ° C |
| | | For industrial use | –40 | 85 | ° C |
| $T_J$ | Operating temperature | For commercial use | 0 | 85 | ° C |
| | | For industrial use | –40 | 100 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

**Table 22. FLEX 10KE 2.5-V Device DC Operating Conditions** *Notes (6), (7)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 1.7, 0.5 × $V_{CCIO}$ *(8)* | | 5.75 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | 0.8, 0.3 × $V_{CCIO}$ *(8)* | V |
| $V_{OH}$ | 3.3-V high-level TTL output voltage | $I_{OH}$ = –8 mA DC, $V_{CCIO}$ = 3.00 V *(9)* | 2.4 | | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(9)* | $V_{CCIO}$ – 0.2 | | | V |
| | 3.3-V high-level PCI output voltage | $I_{OH}$ = –0.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(9)* | 0.9 × $V_{CCIO}$ | | | V |
| | 2.5-V high-level output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 2.30 V *(9)* | 2.1 | | | V |
| | | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.30 V *(9)* | 2.0 | | | V |
| | | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.30 V *(9)* | 1.7 | | | V |
| $V_{OL}$ | 3.3-V low-level TTL output voltage | $I_{OL}$ = 12 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | | | 0.2 | V |
| | 3.3-V low-level PCI output voltage | $I_{OL}$ = 1.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(10)* | | | 0.1 × $V_{CCIO}$ | V |
| | 2.5-V low-level output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | | | 0.2 | V |
| | | $I_{OL}$ = 1 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | | | 0.4 | V |
| | | $I_{OL}$ = 2 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | | | 0.7 | V |
| $I_I$ | Input pin leakage current | $V_I$ = $V_{CCIOmax}$ to 0 V *(11)* | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current | $V_O$ = $V_{CCIOmax}$ to 0 V *(11)* | –10 | | 10 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) | $V_I$ = ground, no load, no toggling inputs | | 5 | | mA |
| | | $V_I$ = ground, no load, no toggling inputs *(12)* | | 10 | | mA |
| $R_{CONF}$ | Value of I/O pin pull-up resistor before and during configuration | $V_{CCIO}$ = 3.0 V *(13)* | 20 | | 50 | k¾ |
| | | $V_{CCIO}$ = 2.3 V *(13)* | 30 | | 80 | k¾ |

Figure 22 shows the required relationship between $V_{CCIO}$ and $V_{CCINT}$ for 3.3-V PCI compliance.

*Figure 22. Relationship between $V_{CCIO}$ & $V_{CCINT}$ for 3.3-V PCI Compliance*

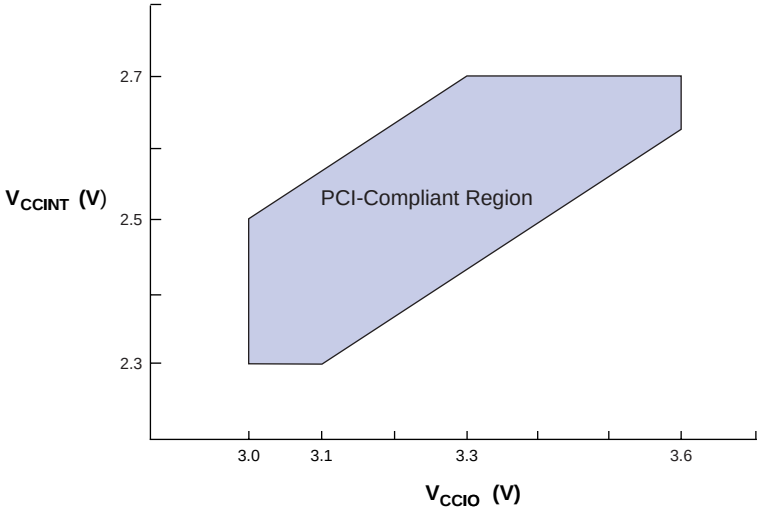
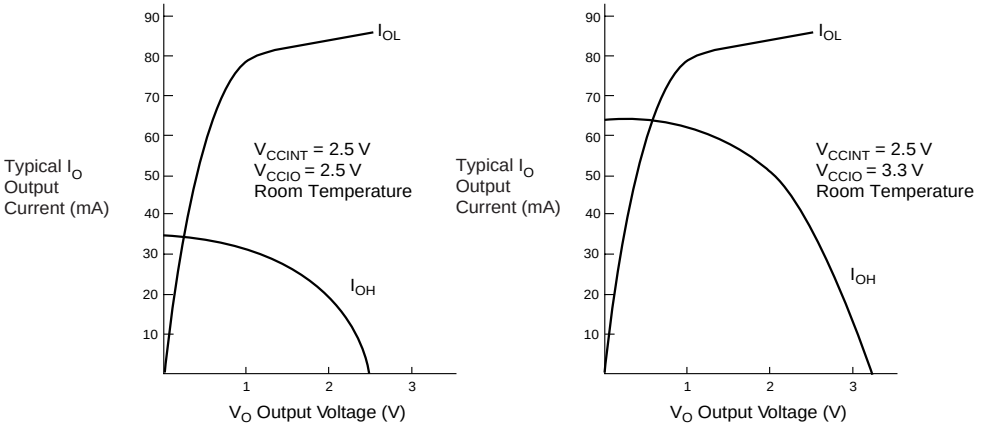



Figure 23 shows the typical output drive characteristics of FLEX 10KE devices with 3.3-V and 2.5-V $V_{CCIO}$. The output driver is compliant to the 3.3-V ***PCI Local Bus Specification, Revision 2.2*** (when VCCIO pins are connected to 3.3 V). FLEX 10KE devices with a -1 speed grade also comply with the drive strength requirements of the ***PCI Local Bus Specification, Revision 2.2*** (when VCCINT pins are powered with a minimum supply of 2.375 V, and VCCIO pins are connected to 3.3 V). Therefore, these devices can be used in open 5.0-V PCI systems.

***Figure 23. Output Drive Characteristics of FLEX 10KE Devices*** *Note (1)*




***Note:***
(1) These are transient (AC) currents.

## Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Device performance can be estimated by following the signal path from a source, through the interconnect, to the destination. For example, the registered performance between two LEs on the same row can be calculated by adding the following parameters:

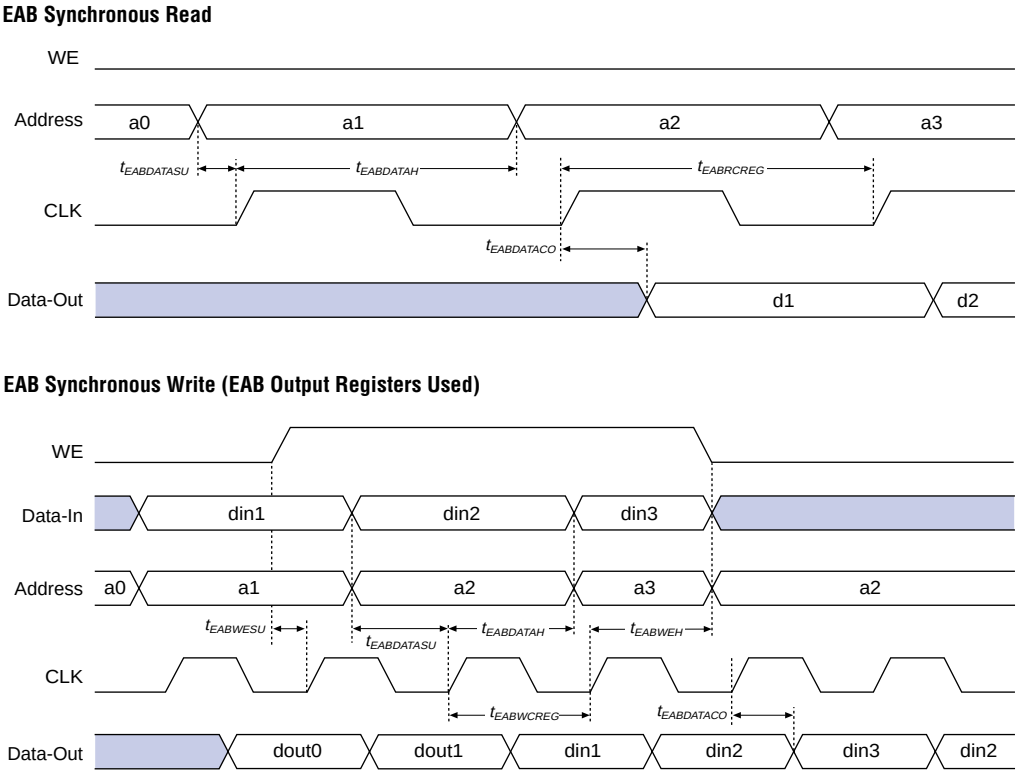
- LE register clock-to-output delay ($t_{CO}$)
- Interconnect delay ($t_{SAMEROW}$)
- LE look-up table delay ($t_{LUT}$)
- LE register setup time ($t_{SU}$)

The routing delay depends on the placement of the source and destination LEs. A more complex registered path may involve multiple combinatorial LEs between the source and destination LEs.

| *Table 28. Interconnect Timing Microparameters* *Note (1)* | | |
|---|---|---|
| **Symbol** | **Parameter** | **Conditions** |
| $t_{DIN2IOE}$ | Delay from dedicated input pin to IOE control input | *(7)* |
| $t_{DIN2LE}$ | Delay from dedicated input pin to LE or EAB control input | *(7)* |
| $t_{DCLK2IOE}$ | Delay from dedicated clock pin to IOE clock | *(7)* |
| $t_{DCLK2LE}$ | Delay from dedicated clock pin to LE or EAB clock | *(7)* |
| $t_{DIN2DATA}$ | Delay from dedicated input or clock to LE or EAB data | *(7)* |
| $t_{SAMELAB}$ | Routing delay for an LE driving another LE in the same LAB | |
| $t_{SAMEROW}$ | Routing delay for a row IOE, LE, or EAB driving a row IOE, LE, or EAB in the same row | *(7)* |
| $t_{SAMECOLUMN}$ | Routing delay for an LE driving an IOE in the same column | *(7)* |
| $t_{DIFFROW}$ | Routing delay for a column IOE, LE, or EAB driving an LE or EAB in a different row | *(7)* |
| $t_{TWOROWS}$ | Routing delay for a row IOE or EAB driving an LE or EAB in a different row | *(7)* |
| $t_{LEPERIPH}$ | Routing delay for an LE driving a control signal of an IOE via the peripheral control bus | *(7)* |
| $t_{LABCARRY}$ | Routing delay for the carry-out signal of an LE driving the carry-in signal of a different LE in a different LAB | |
| $t_{LABCASC}$ | Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB | |

| *Table 29. External Timing Parameters* | | |
|---|---|---|
| **Symbol** | **Parameter** | **Conditions** |
| $\mathbf{t_{DRR}}$ | Register-to-register delay via four LEs, three row interconnects, and four local interconnects | *(8)* |
| $\mathbf{t_{INSU}}$ | Setup time with global clock at IOE register | *(9)* |
| $\mathbf{t_{INH}}$ | Hold time with global clock at IOE register | *(9)* |
| $\mathbf{t_{OUTCO}}$ | Clock-to-output delay with global clock at IOE register | *(9)* |
| $\mathbf{t_{PCISU}}$ | Setup time with global clock for registers used in PCI designs | *(9)*,*(10)* |
| $\mathbf{t_{PCIH}}$ | Hold time with global clock for registers used in PCI designs | *(9)*,*(10)* |
| $\mathbf{t_{PCICO}}$ | Clock-to-output delay with global clock for registers used in PCI designs | *(9)*,*(10)* |

*Figure 30. EAB Synchronous Timing Waveforms*




Tables 31 through 37 show EPF10K30E device internal and external timing parameters.

*Table 31. EPF10K30E Device LE Timing Microparameters (Part 1 of 2)* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{CLUT}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{RLUT}$ | | 0.6 | | 0.7 | | 1.0 | ns |
| $t_{PACKED}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{EN}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{CICO}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.5 | | 0.7 | ns |

**Table 35. EPF10K30E Device Interconnect Timing Microparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DIN2IOE}$ | | 1.8 | | 2.4 | | 2.9 | ns |
| $t_{DIN2LE}$ | | 1.5 | | 1.8 | | 2.4 | ns |
| $t_{DIN2DATA}$ | | 1.5 | | 1.8 | | 2.2 | ns |
| $t_{DCLK2IOE}$ | | 2.2 | | 2.6 | | 3.0 | ns |
| $t_{DCLK2LE}$ | | 1.5 | | 1.8 | | 2.4 | ns |
| $t_{SAMELAB}$ | | 0.1 | | 0.2 | | 0.3 | ns |
| $t_{SAMEROW}$ | | 2.0 | | 2.4 | | 2.7 | ns |
| $t_{SAMECOLUMN}$ | | 0.7 | | 1.0 | | 0.8 | ns |
| $t_{DIFFROW}$ | | 2.7 | | 3.4 | | 3.5 | ns |
| $t_{TWOROWS}$ | | 4.7 | | 5.8 | | 6.2 | ns |
| $t_{LEPERIPH}$ | | 2.7 | | 3.4 | | 3.8 | ns |
| $t_{LABCARRY}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{LABCASC}$ | | 0.8 | | 0.8 | | 1.1 | ns |

**Table 36. EPF10K30E External Timing Parameters** *Notes (1), (2)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 8.0 | | 9.5 | | 12.5 | ns |
| $t_{INSU}$ *(3)* | 2.1 | | 2.5 | | 3.9 | | ns |
| $t_{INH}$ *(3)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(3)* | 2.0 | 4.9 | 2.0 | 5.9 | 2.0 | 7.6 | ns |
| $t_{INSU}$ *(4)* | 1.1 | | 1.5 | | – | | ns |
| $t_{INH}$ *(4)* | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCO}$ *(4)* | 0.5 | 3.9 | 0.5 | 4.9 | – | – | ns |
| $t_{PCISU}$ | 3.0 | | 4.2 | | – | | ns |
| $t_{PCIH}$ | 0.0 | | 0.0 | | – | | ns |
| $t_{PCICO}$ | 2.0 | 6.0 | 2.0 | 7.5 | – | – | ns |

*Table 45. EPF10K100E Device LE Timing Microparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CGENR}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CASC}$ | | 0.6 | | 0.9 | | 1.2 | ns |
| $t_{C}$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{CO}$ | | 0.6 | | 0.8 | | 1.1 | ns |
| $t_{COMB}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{SU}$ | 0.4 | | 0.6 | | 0.7 | | ns |
| $t_{H}$ | 0.5 | | 0.7 | | 0.9 | | ns |
| $t_{PRE}$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{CLR}$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{CH}$ | 1.5 | | 2.0 | | 2.5 | | ns |
| $t_{CL}$ | 1.5 | | 2.0 | | 2.5 | | ns |

*Table 46. EPF10K100E Device IOE Timing Microparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 1.7 | | 2.0 | | 2.6 | ns |
| $t_{IOC}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{IOCO}$ | | 1.4 | | 1.6 | | 2.1 | ns |
| $t_{IOCOMB}$ | | 0.5 | | 0.7 | | 0.9 | ns |
| $t_{IOSU}$ | 0.8 | | 1.0 | | 1.3 | | ns |
| $t_{IOH}$ | 0.7 | | 0.9 | | 1.2 | | ns |
| $t_{IOCLR}$ | | 0.5 | | 0.7 | | 0.9 | ns |
| $t_{OD1}$ | | 3.0 | | 4.2 | | 5.6 | ns |
| $t_{OD2}$ | | 3.0 | | 4.2 | | 5.6 | ns |
| $t_{OD3}$ | | 4.0 | | 5.5 | | 7.3 | ns |
| $t_{XZ}$ | | 3.5 | | 4.6 | | 6.1 | ns |
| $t_{ZX1}$ | | 3.5 | | 4.6 | | 6.1 | ns |
| $t_{ZX2}$ | | 3.5 | | 4.6 | | 6.1 | ns |
| $t_{ZX3}$ | | 4.5 | | 5.9 | | 7.8 | ns |
| $t_{INREG}$ | | 2.0 | | 2.6 | | 3.5 | ns |
| $t_{IOFD}$ | | 0.5 | | 0.8 | | 1.2 | ns |
| $t_{INCOMB}$ | | 0.5 | | 0.8 | | 1.2 | ns |

| Table 58. EPF10K130E External Bidirectional Timing Parameters Notes (1), (2) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ (3) | 2.2 | | 2.4 | | 3.2 | | ns |
| $t_{INHBIDIR}$ (3) | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSUBIDIR}$ (4) | 2.8 | | 3.0 | | – | | ns |
| $t_{INHBIDIR}$ (4) | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCOBIDIR}$ (3) | 2.0 | 5.0 | 2.0 | 7.0 | 2.0 | 9.2 | ns |
| $t_{XZBIDIR}$ (3) | | 5.6 | | 8.1 | | 10.8 | ns |
| $t_{ZXBIDIR}$ (3) | | 5.6 | | 8.1 | | 10.8 | ns |
| $t_{OUTCOBIDIR}$ (4) | 0.5 | 4.0 | 0.5 | 6.0 | – | – | ns |
| $t_{XZBIDIR}$ (4) | | 4.6 | | 7.1 | | – | ns |
| $t_{ZXBIDIR}$ (4) | | 4.6 | | 7.1 | | – | ns |

***Notes to tables:***

(1) All timing parameters are described in Tables 24 through 30 in this data sheet.
(2) These parameters are specified by characterization.
(3) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 59 through 65 show EPF10K200E device internal and external timing parameters.

| Table 59. EPF10K200E Device LE Timing Microparameters (Part 1 of 2) Note (1) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 0.7 | | 0.8 | | 1.2 | ns |
| $t_{CLUT}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{RLUT}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{PACKED}$ | | 0.3 | | 0.5 | | 0.7 | ns |
| $t_{EN}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{CICO}$ | | 0.2 | | 0.2 | | 0.3 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.4 | | 0.6 | ns |
| $t_{CGENR}$ | | 0.2 | | 0.2 | | 0.3 | ns |
| $t_{CASC}$ | | 0.7 | | 0.8 | | 1.2 | ns |
| $t_{C}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{CO}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{COMB}$ | | 0.4 | | 0.6 | | 0.8 | ns |
| $t_{SU}$ | 0.4 | | 0.6 | | 0.7 | | ns |

*Table 69. EPF10K50S Device EAB Internal Timing Macroparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABAA}$ | | 3.7 | | 5.2 | | 7.0 | ns |
| $t_{EABRCCOMB}$ | 3.7 | | 5.2 | | 7.0 | | ns |
| $t_{EABRCREG}$ | 3.5 | | 4.9 | | 6.6 | | ns |
| $t_{EABWP}$ | 2.0 | | 2.8 | | 3.8 | | ns |
| $t_{EABWCCOMB}$ | 4.5 | | 6.3 | | 8.6 | | ns |
| $t_{EABWCREG}$ | 5.6 | | 7.8 | | 10.6 | | ns |
| $t_{EABDD}$ | | 3.8 | | 5.3 | | 7.2 | ns |
| $t_{EABDATACO}$ | | 0.8 | | 1.1 | | 1.5 | ns |
| $t_{EABDATASU}$ | 1.1 | | 1.6 | | 2.1 | | ns |
| $t_{EABDATAH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWESU}$ | 0.7 | | 1.0 | | 1.3 | | ns |
| $t_{EABWEH}$ | 0.4 | | 0.6 | | 0.8 | | ns |
| $t_{EABWDSU}$ | 1.2 | | 1.7 | | 2.2 | | ns |
| $t_{EABWDH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWASU}$ | 1.6 | | 2.3 | | 3.0 | | ns |
| $t_{EABWAH}$ | 0.9 | | 1.2 | | 1.8 | | ns |
| $t_{EABWO}$ | | 3.1 | | 4.3 | | 5.9 | ns |

*Table 70. EPF10K50S Device Interconnect Timing Microparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DIN2IOE}$ | | 3.1 | | 3.7 | | 4.6 | ns |
| $t_{DIN2LE}$ | | 1.7 | | 2.1 | | 2.7 | ns |
| $t_{DIN2DATA}$ | | 2.7 | | 3.1 | | 5.1 | ns |
| $t_{DCLK2IOE}$ | | 1.6 | | 1.9 | | 2.6 | ns |
| $t_{DCLK2LE}$ | | 1.7 | | 2.1 | | 2.7 | ns |
| $t_{SAMELAB}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{SAMEROW}$ | | 1.5 | | 1.7 | | 2.4 | ns |
| $t_{SAMECOLUMN}$ | | 1.0 | | 1.3 | | 2.1 | ns |
| $t_{DIFFROW}$ | | 2.5 | | 3.0 | | 4.5 | ns |
| $t_{TWOROWS}$ | | 4.0 | | 4.7 | | 6.9 | ns |
| $t_{LEPERIPH}$ | | 2.6 | | 2.9 | | 3.4 | ns |
| $t_{LABCARRY}$ | | 0.1 | | 0.2 | | 0.2 | ns |
| $t_{LABCASC}$ | | 0.8 | | 1.0 | | 1.3 | ns |

**Table 77. EPF10K200S Device Interconnect Timing Microparameters (Part 2 of 2)** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{LABCASC}$ | | 0.5 | | 1.0 | | 1.4 | ns |

**Table 78. EPF10K200S External Timing Parameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 9.0 | | 12.0 | | 16.0 | ns |
| $t_{INSU}$ *(2)* | 3.1 | | 3.7 | | 4.7 | | ns |
| $t_{INH}$ *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(2)* | 2.0 | 3.7 | 2.0 | 4.4 | 2.0 | 6.3 | ns |
| $t_{INSU}$*(3)* | 2.1 | | 2.7 | | – | | ns |
| $t_{INH}$ *(3)* | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCO}$*(3)* | 0.5 | 2.7 | 0.5 | 3.4 | – | – | ns |
| $t_{PCISU}$ | 3.0 | | 4.2 | | – | | ns |
| $t_{PCIH}$ | 0.0 | | 0.0 | | – | | ns |
| $t_{PCICO}$ | 2.0 | 6.0 | 2.0 | 8.9 | – | – | ns |

**Table 79. EPF10K200S External Bidirectional Timing Parameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ *(2)* | 2.3 | | 3.4 | | 4.4 | | ns |
| $t_{INHBIDIR}$ *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSUBIDIR}$ *(3)* | 3.3 | | 4.4 | | – | | ns |
| $t_{INHBIDIR}$ *(3)* | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCOBIDIR}$ *(2)* | 2.0 | 3.7 | 2.0 | 4.4 | 2.0 | 6.3 | ns |
| $t_{XZBIDIR}$ *(2)* | | 6.9 | | 7.6 | | 9.2 | ns |
| $t_{ZXBIDIR}$ *(2)* | | 5.9 | | 6.6 | | – | ns |
| $t_{OUTCOBIDIR}$ *(3)* | 0.5 | 2.7 | 0.5 | 3.4 | – | – | ns |
| $t_{XZBIDIR}$ *(3)* | | 6.9 | | 7.6 | | 9.2 | ns |
| $t_{ZXBIDIR}$ *(3)* | | 5.9 | | 6.6 | | – | ns |

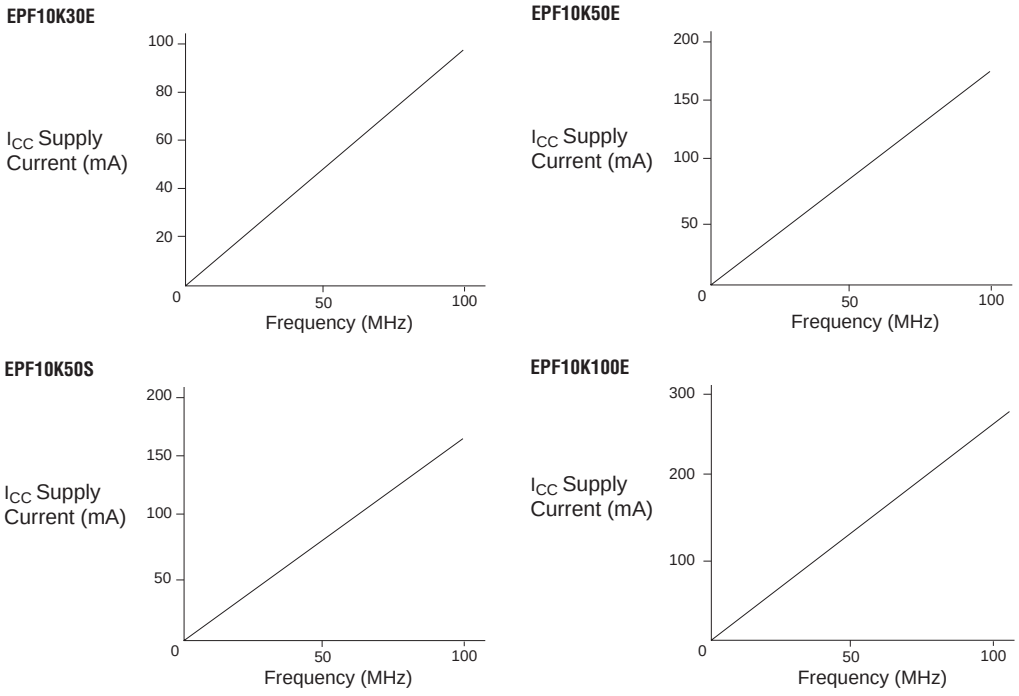
***Notes to tables:***

(1) All timing parameters are described in Tables 24 through 30 in this data sheet.
(2) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(3) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

To better reflect actual designs, the power model (and the constant K in the power calculation equations) for continuous interconnect FLEX devices assumes that LEs drive FastTrack Interconnect channels. In contrast, the power model of segmented FPGAs assumes that all LEs drive only one short interconnect segment. This assumption may lead to inaccurate results when compared to measured power consumption for actual designs in segmented FPGAs.

Figure 31 shows the relationship between the current and operating frequency of FLEX 10KE devices.

*Figure 31. FLEX 10KE $I_{CCACTIVE}$ vs. Operating Frequency (Part 1 of 2)*



## Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the Altera Digital Library for pin-out information.

## Revision History

The information contained in the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.5 supersedes information published in previous versions.

### Version 2.5

The following changes were made to the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.5:

- *Note (1)* added to Figure 23.
- Text added to "I/O Element" section on page 34.
- Updated Table 22.

### Version 2.4

The following changes were made to the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.4: updated text on page 34 and page 63.