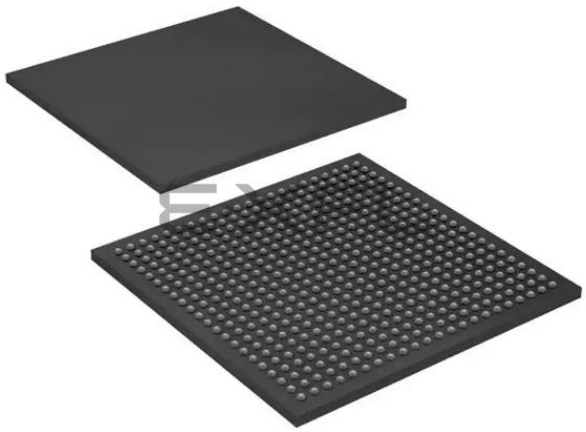


Welcome to E-XFL.COM

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 360 |
| Number of Logic Elements/Cells | 2880 |
| Total RAM Bits | 40960 |
| Number of I/O | 220 |
| Number of Gates | 199000 |
| Voltage - Supply | 2.3V ~ 2.7V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 484-BBGA |
| Supplier Device Package | 484-FBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epf10k50efi484-3 |

Similar to the FLEX 10KE architecture, embedded gate arrays are the fastest-growing segment of the gate array market. As with standard gate arrays, embedded gate arrays implement general logic in a conventional "sea-of-gates" architecture. Additionally, embedded gate arrays have dedicated die areas for implementing large, specialized functions. By embedding functions in silicon, embedded gate arrays reduce die area and increase speed when compared to standard gate arrays. While embedded megafunctions typically cannot be customized, FLEX 10KE devices are programmable, providing the designer with full control over embedded megafunctions and general logic, while facilitating iterative design changes during debugging.

Each FLEX 10KE device contains an embedded array and a logic array. The embedded array is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), wide data-path manipulation, microcontroller applications, and data-transformation functions. The logic array performs the same function as the sea-of-gates in the gate array and is used to implement general logic such as counters, adders, state machines, and multiplexers. The combination of embedded and logic arrays provides the high performance and high density of embedded gate arrays, enabling designers to implement an entire system on a single device.

FLEX 10KE devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers the EPC1, EPC2, and EPC16 configuration devices, which configure FLEX 10KE devices via a serial data stream. Configuration data can also be downloaded from system RAM or via the Altera BitBlaster™, ByteBlasterMV™, or MasterBlaster download cables. After a FLEX 10KE device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 85 ms, real-time changes can be made during system operation.

FLEX 10KE devices contain an interface that permits microprocessors to configure FLEX 10KE devices serially or in-parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat a FLEX 10KE device as memory and configure it by writing to a virtual memory location, making it easy to reconfigure the device.

## Functional Description

Each FLEX 10KE device contains an enhanced embedded array to implement memory and specialized logic functions, and a logic array to implement general logic.

The embedded array consists of a series of EABs. When implementing memory functions, each EAB provides 4,096 bits, which can be used to create RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. When implementing logic, each EAB can contribute 100 to 600 gates towards complex logic functions, such as multipliers, microcontrollers, state machines, and DSP functions. EABs can be used independently, or multiple EABs can be combined to implement larger functions.

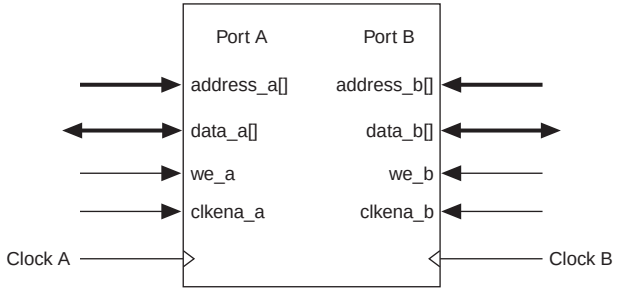
The logic array consists of logic array blocks (LABs). Each LAB contains eight LEs and a local interconnect. An LE consists of a four-input look-up table (LUT), a programmable flipflop, and dedicated signal paths for carry and cascade functions. The eight LEs can be used to create medium-sized blocks of logic—such as 8-bit counters, address decoders, or state machines—or combined across LABs to create larger logic blocks. Each LAB represents about 96 usable gates of logic.

Signal interconnections within FLEX 10KE devices (as well as to and from device pins) are provided by the FastTrack Interconnect routing structure, which is a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect routing structure. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an output or input register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. As inputs, they provide setup times as low as 0.9 ns and hold times of 0 ns. As outputs, these registers provide clock-to-output times as low as 3.0 ns. IOEs provide a variety of features, such as JTAG BST support, slew-rate control, tri-state buffers, and open-drain outputs.

The EAB can also use Altera megafunctions to implement dual-port RAM applications where both ports can read or write, as shown in Figure 3.

*Figure 3. FLEX 10KE EAB in Dual-Port RAM Mode*




The FLEX 10KE EAB can be used in a single-port mode, which is useful for backward-compatibility with FLEX 10K designs (see Figure 4).

EABs provide flexible options for driving and controlling clock signals. Different clocks and clock enables can be used for reading and writing to the EAB. Registers can be independently inserted on the data input, EAB output, write address, write enable signals, read address, and read enable signals. The global signals and the EAB local interconnect can drive write enable, read enable, and clock enable signals. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control write enable, read enable, clear, clock, and clock enable signals.

An EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs (see Figures 2 and 4). The column interconnect, which is adjacent to the EAB, has twice as many channels as other columns in the device.

## Logic Array Block

An LAB consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure to the FLEX 10KE architecture, facilitating efficient routing with optimum device utilization and high performance (see Figure 7).

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks, the other two can be used for clear / preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I / O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I / O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LE in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated from LE outputs.

## Logic Element

The LE, the smallest unit of logic in the FLEX 10KE architecture, has a compact size that provides efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous clock enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect routing structure (see Figure 8).

*Figure 8. FLEX 10KE Logic Element*

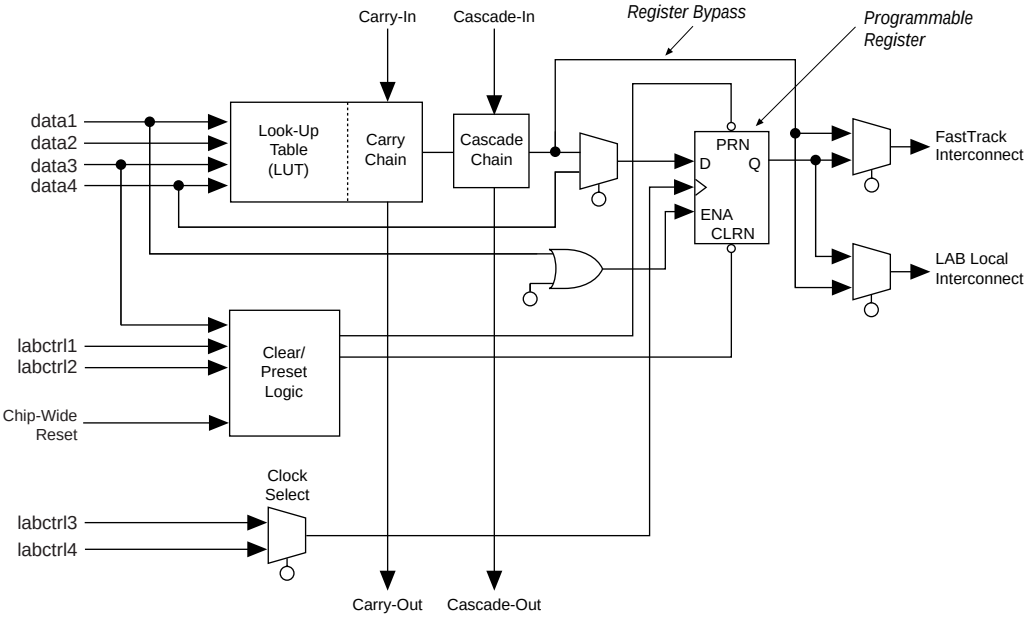
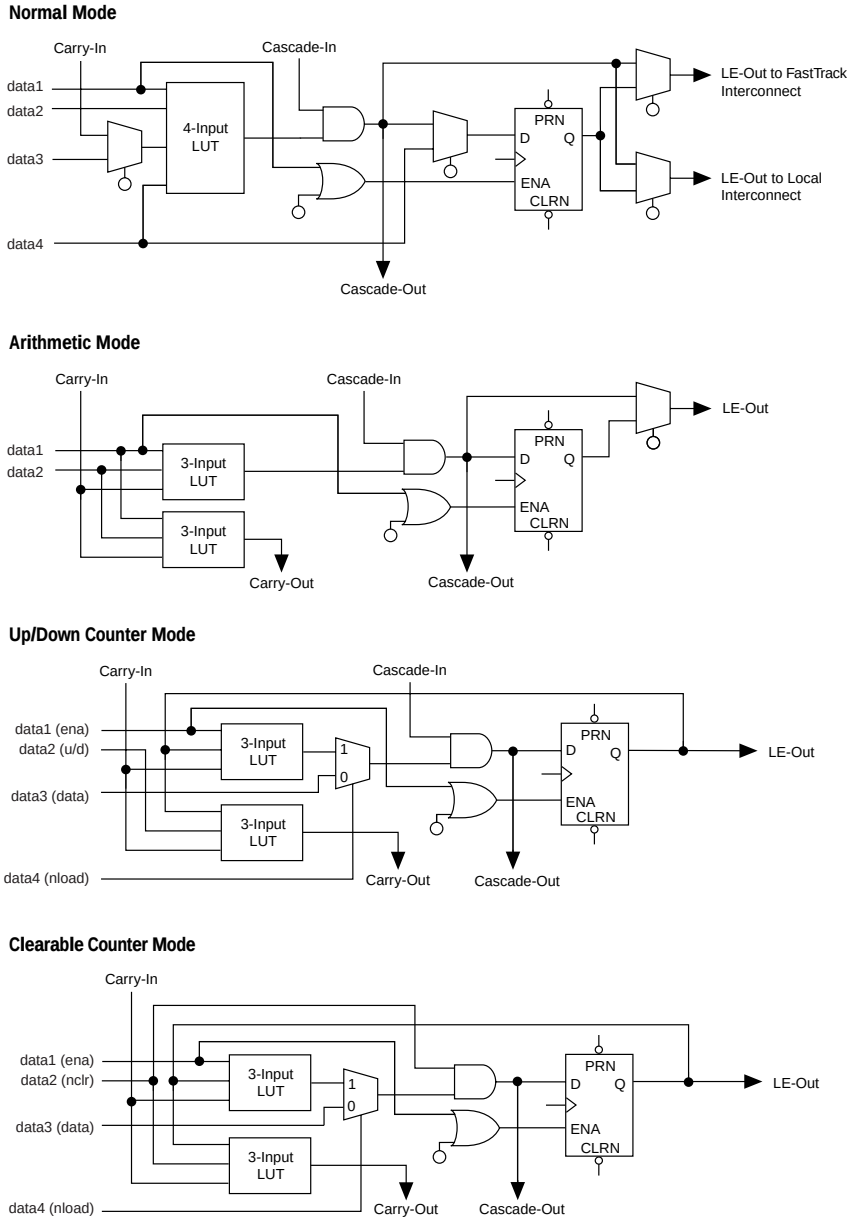


Figure 11 shows the LE operating modes.

*Figure 11. FLEX 10KE LE Operating Modes*



### Clearable Counter Mode

The clearable counter mode is similar to the up / down counter mode, but supports a synchronous clear instead of the up / down control. The clear function is substituted for the cascade-in signal in the up / down counter mode. Use 2 three-input LUTs: one generates the counter data, and the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer. The output of this multiplexer is ANDed with a synchronous clear signal.

#### *Internal Tri-State Emulation*

Internal tri-state emulation provides internal tri-states without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable (OE) signals select which signal drives the bus. However, if multiple OE signals are active, contending signals can be driven onto the bus. Conversely, if no OE signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The Altera software automatically implements tri-state bus functionality with a multiplexer.

#### *Clear & Preset Logic Control*

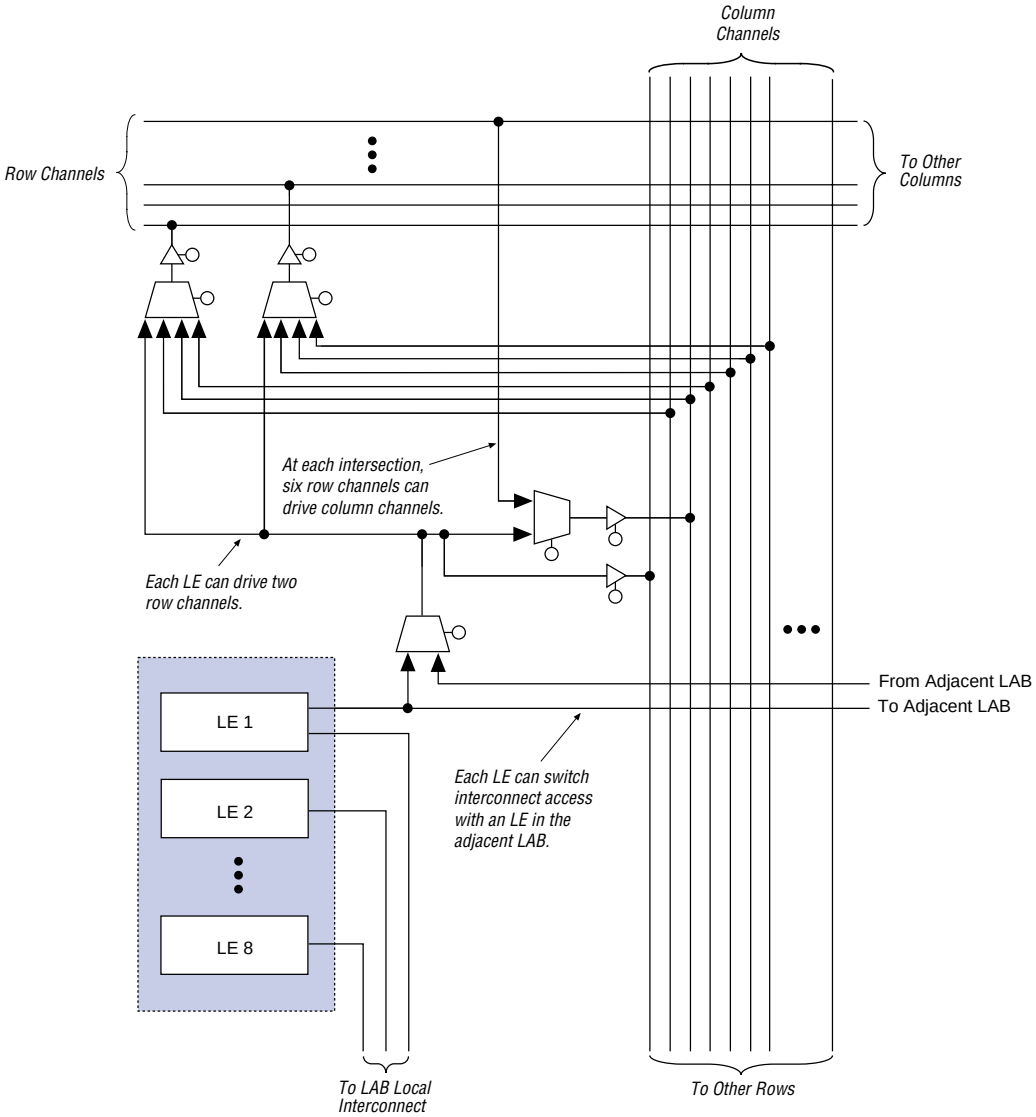
Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. The clear and preset control structure of the LE asynchronously loads signals into a register. Either LABCTRL1 or LABCTRL2 can control the asynchronous clear. Alternatively, the register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

During compilation, the Altera Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six modes chosen during design entry:

- Asynchronous clear
- Asynchronous preset
- Asynchronous clear and preset
- Asynchronous load with clear
- Asynchronous load with preset
- Asynchronous load without clear or preset

*Figure 13. FLEX 10KE LAB Connections to Row & Column Interconnect*



When dedicated inputs drive non-inverted and inverted peripheral clears, clock enables, and output enables, two signals on the peripheral control bus will be used.

Tables 8 and 9 list the sources for each peripheral control signal, and show how the output enable, clock enable, clock, and clear signals share 12 peripheral control signals. The tables also show the rows that can drive global signals.

*Table 8. Peripheral Bus Sources for EPF10K30E, EPF10K50E & EPF10K50S Devices*

| Peripheral Control Signal | EPF10K30E | EPF10K50E EPF10K50S |
|---|---|---|
| OE0 | Row A | Row A |
| OE1 | Row B | Row B |
| OE2 | Row C | Row D |
| OE3 | Row D | Row F |
| OE4 | Row E | Row H |
| OE5 | Row F | Row J |
| CLKENA0/CLK0/GLOBAL0 | Row A | Row A |
| CLKENA1/OE6/GLOBAL1 | Row B | Row C |
| CLKENA2/CLR0 | Row C | Row E |
| CLKENA3/OE7/GLOBAL2 | Row D | Row G |
| CLKENA4/CLR1 | Row E | Row I |
| CLKENA5/CLK1/GLOBAL3 | Row F | Row J |

*Table 9. Peripheral Bus Sources for EPF10K100E, EPF10K130E, EPF10K200E & EPF10K200S Devices*

| Peripheral Control Signal | EPF10K100E | EPF10K130E | EPF10K200E EPF10K200S |
|---|---|---|---|
| OE0 | Row A | Row C | Row G |
| OE1 | Row C | Row E | Row I |
| OE2 | Row E | Row G | Row K |
| OE3 | Row L | Row N | Row R |
| OE4 | Row I | Row K | Row O |
| OE5 | Row K | Row M | Row Q |
| CLKENA0/CLK0/GLOBAL0 | Row F | Row H | Row L |
| CLKENA1/OE6/GLOBAL1 | Row D | Row F | Row J |
| CLKENA2/CLR0 | Row B | Row D | Row H |
| CLKENA3/OE7/GLOBAL2 | Row H | Row J | Row N |
| CLKENA4/CLR1 | Row J | Row L | Row P |
| CLKENA5/CLK1/GLOBAL3 | Row G | Row I | Row M |

Signals on the peripheral control bus can also drive the four global signals, referred to as GLOBAL0 through GLOBAL3 in Tables 8 and 9. An internally generated signal can drive a global signal, providing the same low-skew, low-delay characteristics as a signal driven by an input pin. An LE drives the global signal by driving a row line that drives the peripheral bus, which then drives the global signal. This feature is ideal for internally generated clear or clock signals with high fan-out. However, internally driven global signals offer no advantage over the general-purpose interconnect for routing data signals. The dedicated input pin should be driven to a known logic state (such as ground) and not be allowed to float.

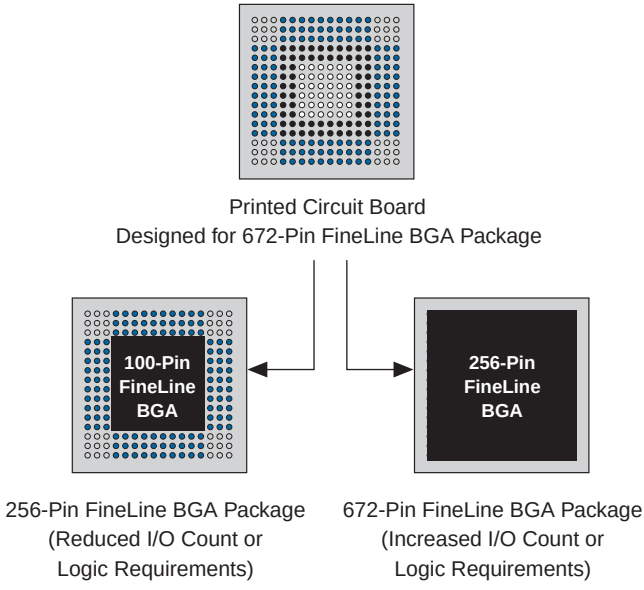
The chip-wide output enable pin is an active-high pin (DEV_OE) that can be used to tri-state all pins on the device. This option can be set in the Altera software. On EPF10K50E and EPF10K200E devices, the built-in I/O pin pull-up resistors (which are active during configuration) are active when the chip-wide output enable pin is asserted. The registers in the IOE can also be reset by the chip-wide reset pin.

## SameFrame Pin-Outs

FLEX 10KE devices support the SameFrame pin-out feature for FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. A given printed circuit board (PCB) layout can support multiple device density / package combinations. For example, a single board layout can support a range of devices from an EPF10K30E device in a 256-pin FineLine BGA package to an EPF10K200S device in a 672-pin FineLine BGA package.

The Altera software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Altera software generates pin-outs describing how to lay out a board to take advantage of this migration (see Figure 18).

*Figure 18. SameFrame Pin-Out Example*



## PCI Pull-Up Clamping Diode Option

FLEX 10KE devices have a pull-up clamping diode on every I/O, dedicated input, and dedicated clock pin. PCI clamping diodes clamp the signal to the $V_{CCIO}$ value and are required for 3.3-V PCI compliance. Clamping diodes can also be used to limit overshoot in other systems.

Clamping diodes are controlled on a pin-by-pin basis. When $V_{CCIO}$ is 3.3 V, a pin that has the clamping diode option turned on can be driven by a 2.5-V or 3.3-V signal, but not a 5.0-V signal. When $V_{CCIO}$ is 2.5 V, a pin that has the clamping diode option turned on can be driven by a 2.5-V signal, but not a 3.3-V or 5.0-V signal. Additionally, a clamping diode can be activated for a subset of pins, which would allow a device to bridge between a 3.3-V PCI bus and a 5.0-V device.

## Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces system noise and adds a maximum delay of 4.3 ns. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate pin-by-pin or assign a default slew rate to all pins on a device-wide basis. The slow slew rate setting affects the falling edge of the output.

## Open-Drain Output Option

FLEX 10KE devices provide an optional open-drain output (electrically equivalent to open-collector output) for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

## MultiVolt I/O Interface

The FLEX 10KE device architecture supports the MultiVolt I/O interface feature, which allows FLEX 10KE devices in all packages to interface with systems of differing supply voltages. These devices have one set of $V_{CC}$ pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

**Table 22. FLEX 10KE 2.5-V Device DC Operating Conditions** *Notes (6), (7)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 1.7, 0.5 × $V_{CCIO}$ *(8)* | | 5.75 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | 0.8, 0.3 × $V_{CCIO}$ *(8)* | V |
| $V_{OH}$ | 3.3-V high-level TTL output voltage | $I_{OH}$ = –8 mA DC, $V_{CCIO}$ = 3.00 V *(9)* | 2.4 | | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(9)* | $V_{CCIO}$ – 0.2 | | | V |
| | 3.3-V high-level PCI output voltage | $I_{OH}$ = –0.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(9)* | 0.9 × $V_{CCIO}$ | | | V |
| | 2.5-V high-level output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 2.30 V *(9)* | 2.1 | | | V |
| | | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.30 V *(9)* | 2.0 | | | V |
| | | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.30 V *(9)* | 1.7 | | | V |
| $V_{OL}$ | 3.3-V low-level TTL output voltage | $I_{OL}$ = 12 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | | | 0.2 | V |
| | 3.3-V low-level PCI output voltage | $I_{OL}$ = 1.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(10)* | | | 0.1 × $V_{CCIO}$ | V |
| | 2.5-V low-level output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | | | 0.2 | V |
| | | $I_{OL}$ = 1 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | | | 0.4 | V |
| | | $I_{OL}$ = 2 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | | | 0.7 | V |
| $I_I$ | Input pin leakage current | $V_I$ = $V_{CCIOmax}$ to 0 V *(11)* | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current | $V_O$ = $V_{CCIOmax}$ to 0 V *(11)* | –10 | | 10 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) | $V_I$ = ground, no load, no toggling inputs | | 5 | | mA |
| | | $V_I$ = ground, no load, no toggling inputs *(12)* | | 10 | | mA |
| $R_{CONF}$ | Value of I/O pin pull-up resistor before and during configuration | $V_{CCIO}$ = 3.0 V *(13)* | 20 | | 50 | k¾ |
| | | $V_{CCIO}$ = 2.3 V *(13)* | 30 | | 80 | k¾ |

Figure 22 shows the required relationship between $V_{CCIO}$ and $V_{CCINT}$ for 3.3-V PCI compliance.

*Figure 22. Relationship between $V_{CCIO}$ & $V_{CCINT}$ for 3.3-V PCI Compliance*

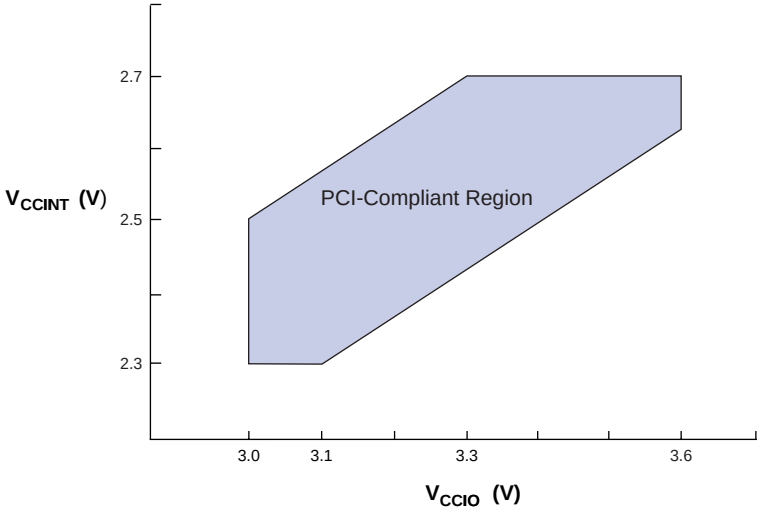
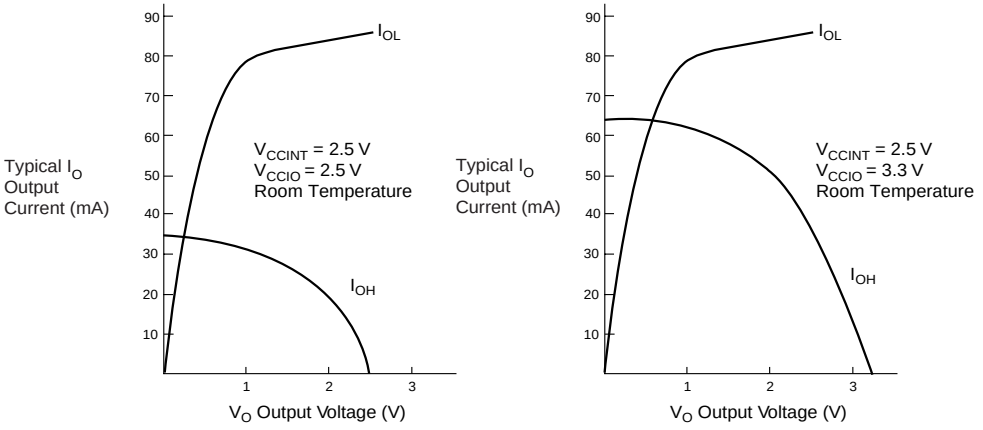



Figure 23 shows the typical output drive characteristics of FLEX 10KE devices with 3.3-V and 2.5-V $V_{CCIO}$. The output driver is compliant to the 3.3-V ***PCI Local Bus Specification, Revision 2.2*** (when VCCIO pins are connected to 3.3 V). FLEX 10KE devices with a -1 speed grade also comply with the drive strength requirements of the ***PCI Local Bus Specification, Revision 2.2*** (when VCCINT pins are powered with a minimum supply of 2.375 V, and VCCIO pins are connected to 3.3 V). Therefore, these devices can be used in open 5.0-V PCI systems.

***Figure 23. Output Drive Characteristics of FLEX 10KE Devices*** *Note (1)*




***Note:***
(1) These are transient (AC) currents.

## Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

Device performance can be estimated by following the signal path from a source, through the interconnect, to the destination. For example, the registered performance between two LEs on the same row can be calculated by adding the following parameters:

- LE register clock-to-output delay ($t_{CO}$)
- Interconnect delay ($t_{SAMEROW}$)
- LE look-up table delay ($t_{LUT}$)
- LE register setup time ($t_{SU}$)

The routing delay depends on the placement of the source and destination LEs. A more complex registered path may involve multiple combinatorial LEs between the source and destination LEs.

**Table 26. EAB Timing Microparameters** *Note (1)*

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{EABDATA1}$ | Data or address delay to EAB for combinatorial input | |
| $t_{EABDATA2}$ | Data or address delay to EAB for registered input | |
| $t_{EABWE1}$ | Write enable delay to EAB for combinatorial input | |
| $t_{EABWE2}$ | Write enable delay to EAB for registered input | |
| $t_{EABRE1}$ | Read enable delay to EAB for combinatorial input | |
| $t_{EABRE2}$ | Read enable delay to EAB for registered input | |
| $t_{EABCLK}$ | EAB register clock delay | |
| $t_{EABCO}$ | EAB register clock-to-output delay | |
| $t_{EABBYPASS}$ | Bypass register delay | |
| $t_{EABSU}$ | EAB register setup time before clock | |
| $t_{EABH}$ | EAB register hold time after clock | |
| $t_{EABCLR}$ | EAB register asynchronous clear time to output delay | |
| $t_{AA}$ | Address access delay (including the read enable to output delay) | |
| $t_{WP}$ | Write pulse width | |
| $t_{RP}$ | Read pulse width | |
| $t_{WDSU}$ | Data setup time before falling edge of write pulse | *(5)* |
| $t_{WDH}$ | Data hold time after falling edge of write pulse | *(5)* |
| $t_{WASU}$ | Address setup time before rising edge of write pulse | *(5)* |
| $t_{WAH}$ | Address hold time after falling edge of write pulse | *(5)* |
| $t_{RASU}$ | Address setup time with respect to the falling edge of the read enable | |
| $t_{RAH}$ | Address hold time with respect to the falling edge of the read enable | |
| $t_{WO}$ | Write enable to data output valid delay | |
| $t_{DD}$ | Data-in to data-out valid delay | |
| $t_{EABOUT}$ | Data-out delay | |
| $t_{EABCH}$ | Clock high time | |
| $t_{EABCL}$ | Clock low time | |

| *Table 30. External Bidirectional Timing Parameters* *Note (9)* | | |
|---|---|---|
| **Symbol** | **Parameter** | **Conditions** |
| $t_{INSUBIDIR}$ | Setup time for bi-directional pins with global clock at same-row or same-column LE register | |
| $t_{INHBIDIR}$ | Hold time for bidirectional pins with global clock at same-row or same-column LE register | |
| $t_{INH}$ | Hold time with global clock at IOE register | |
| $t_{OUTCOBIDIR}$ | Clock-to-output delay for bidirectional pins with global clock at IOE register | C1 = 35 pF |
| $t_{XZBIDIR}$ | Synchronous IOE output buffer disable delay | C1 = 35 pF |
| $t_{ZXBIDIR}$ | Synchronous IOE output buffer enable delay, slow slew rate= off | C1 = 35 pF |

***Notes to tables:***

(1) Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.
(2) Operating conditions: VCCIO = 3.3 V ±10% for commercial or industrial use.
(3) Operating conditions: VCCIO = 2.5 V ±5% for commercial or industrial use in EPF10K30E, EPF10K50S, EPF10K100E, EPF10K130E, and EPF10K200S devices.
(4) Operating conditions: VCCIO = 3.3 V.
(5) Because the RAM in the EAB is self-timed, this parameter can be ignored when the WE signal is registered.
(6) EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.
(7) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.
(8) Contact Altera Applications for test circuit specifications and test conditions.
(9) This timing parameter is sample-tested only.
(10) This parameter is measured with the measurement and test conditions, including load, specified in the PCI Local Bus Specification, revision 2.2.

*Table 37. EPF10K30E External Bidirectional Timing Parameters* *Notes (1), (2)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ (3) | 2.8 | | 3.9 | | 5.2 | | ns |
| $t_{INHBIDIR}$ (3) | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSUBIDIR}$ (4) | 3.8 | | 4.9 | | – | | ns |
| $t_{INHBIDIR}$ (4) | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCOBIDIR}$ (3) | 2.0 | 4.9 | 2.0 | 5.9 | 2.0 | 7.6 | ns |
| $t_{XZBIDIR}$ (3) | | 6.1 | | 7.5 | | 9.7 | ns |
| $t_{ZXBIDIR}$ (3) | | 6.1 | | 7.5 | | 9.7 | ns |
| $t_{OUTCOBIDIR}$ (4) | 0.5 | 3.9 | 0.5 | 4.9 | – | – | ns |
| $t_{XZBIDIR}$ (4) | | 5.1 | | 6.5 | | – | ns |
| $t_{ZXBIDIR}$ (4) | | 5.1 | | 6.5 | | – | ns |

***Notes to tables:***

(1) All timing parameters are described in Tables 24 through 30 in this data sheet.
(2) These parameters are specified by characterization.
(3) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 38 through 44 show EPF10K50E device internal and external timing parameters.

*Table 38. EPF10K50E Device LE Timing Microparameters (Part 1 of 2)* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 0.6 | | 0.9 | | 1.3 | ns |
| $t_{CLUT}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{RLUT}$ | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{PACKED}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{EN}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{CICO}$ | | 0.2 | | 0.2 | | 0.3 | ns |
| $t_{CGEN}$ | | 0.5 | | 0.5 | | 0.8 | ns |
| $t_{CGENR}$ | | 0.2 | | 0.2 | | 0.3 | ns |
| $t_{CASC}$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{C}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{CO}$ | | 0.7 | | 0.7 | | 0.9 | ns |
| $t_{COMB}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{SU}$ | 0.7 | | 0.7 | | 0.8 | | ns |

*Table 71. EPF10K50S External Timing Parameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 8.0 | | 9.5 | | 12.5 | ns |
| $t_{INSU}$ *(2)* | 2.4 | | 2.9 | | 3.9 | | ns |
| $t_{INH}$ *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(2)* | 2.0 | 4.3 | 2.0 | 5.2 | 2.0 | 7.3 | ns |
| $t_{INSU}$ *(3)* | 2.4 | | 2.9 | | | | ns |
| $t_{INH}$ *(3)* | 0.0 | | 0.0 | | | | ns |
| $t_{OUTCO}$ *(3)* | 0.5 | 3.3 | 0.5 | 4.1 | | | ns |
| $t_{PCISU}$ | 2.4 | | 2.9 | | – | | ns |
| $t_{PCIH}$ | 0.0 | | 0.0 | | – | | ns |
| $t_{PCICO}$ | 2.0 | 6.0 | 2.0 | 7.7 | – | – | ns |

*Table 72. EPF10K50S External Bidirectional Timing Parameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ *(2)* | 2.7 | | 3.2 | | 4.3 | | ns |
| $t_{INHBIDIR}$ *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INHBIDIR}$ *(3)* | 0.0 | | 0.0 | | – | | ns |
| $t_{INSUBIDIR}$ *(3)* | 3.7 | | 4.2 | | – | | ns |
| $t_{OUTCOBIDIR}$ *(2)* | 2.0 | 4.5 | 2.0 | 5.2 | 2.0 | 7.3 | ns |
| $t_{XZBIDIR}$ *(2)* | | 6.8 | | 7.8 | | 10.1 | ns |
| $t_{ZXBIDIR}$ *(2)* | | 6.8 | | 7.8 | | 10.1 | ns |
| $t_{OUTCOBIDIR}$ *(3)* | 0.5 | 3.5 | 0.5 | 4.2 | – | – | |
| $t_{XZBIDIR}$ *(3)* | | 6.8 | | 8.4 | | – | ns |
| $t_{ZXBIDIR}$ *(3)* | | 6.8 | | 8.4 | | – | ns |

***Notes to tables:***

(1) All timing parameters are described in Tables 24 through 30.
(2) This parameter is measured without use of the ClockLock or ClockBoost circuits.
(3) This parameter is measured with use of the ClockLock or ClockBoost circuits

*Table 73. EPF10K200S Device Internal & External Timing Parameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 0.7 | | 0.8 | | 1.2 | ns |
| $t_{CLUT}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{RLUT}$ | | 0.5 | | 0.7 | | 0.9 | ns |
| $t_{PACKED}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{EN}$ | | 0.6 | | 0.5 | | 0.6 | ns |
| $t_{CICO}$ | | 0.1 | | 0.2 | | 0.3 | ns |
| $t_{CGEN}$ | | 0.3 | | 0.4 | | 0.6 | ns |
| $t_{CGENR}$ | | 0.1 | | 0.2 | | 0.3 | ns |
| $t_{CASC}$ | | 0.7 | | 0.8 | | 1.2 | ns |
| $t_{C}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{CO}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{COMB}$ | | 0.3 | | 0.6 | | 0.8 | ns |
| $t_{SU}$ | 0.4 | | 0.6 | | 0.7 | | ns |
| $t_{H}$ | 1.0 | | 1.1 | | 1.5 | | ns |
| $t_{PRE}$ | | 0.4 | | 0.6 | | 0.8 | ns |
| $t_{CLR}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 3.0 | | ns |

*Table 74. EPF10K200S Device IOE Timing Microparameters (Part 1 of 2)* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 1.8 | | 1.9 | | 2.6 | ns |
| $t_{IOC}$ | | 0.3 | | 0.3 | | 0.5 | ns |
| $t_{IOCO}$ | | 1.7 | | 1.9 | | 2.6 | ns |
| $t_{IOCOMB}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{IOSU}$ | 0.8 | | 0.9 | | 1.2 | | ns |
| $t_{IOH}$ | 0.4 | | 0.8 | | 1.1 | | ns |
| $t_{IOCLR}$ | | 0.2 | | 0.2 | | 0.3 | ns |
| $t_{OD1}$ | | 1.3 | | 0.7 | | 0.9 | ns |
| $t_{OD2}$ | | 0.8 | | 0.2 | | 0.4 | ns |
| $t_{OD3}$ | | 2.9 | | 3.0 | | 3.9 | ns |
| $t_{XZ}$ | | 5.0 | | 5.3 | | 7.1 | ns |
| $t_{ZX1}$ | | 5.0 | | 5.3 | | 7.1 | ns |