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### **Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### **Details**

Product Status	Active
Number of LABs/CLBs	360
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	147
Number of Gates	-
Voltage - Supply	2.3V ~ 2.7V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=epf10k50eqc208-3">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=epf10k50eqc208-3</a>

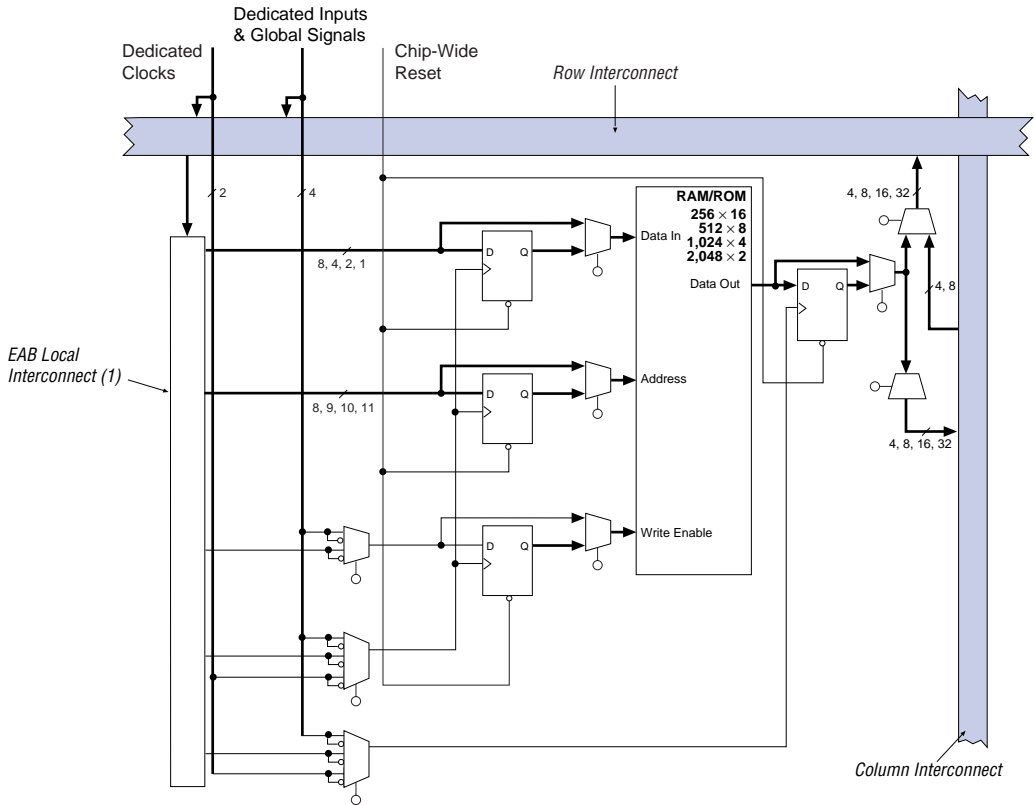
Similar to the FLEX 10KE architecture, embedded gate arrays are the fastest-growing segment of the gate array market. As with standard gate arrays, embedded gate arrays implement general logic in a conventional “sea-of-gates” architecture. Additionally, embedded gate arrays have dedicated die areas for implementing large, specialized functions. By embedding functions in silicon, embedded gate arrays reduce die area and increase speed when compared to standard gate arrays. While embedded megafunctions typically cannot be customized, FLEX 10KE devices are programmable, providing the designer with full control over embedded megafunctions and general logic, while facilitating iterative design changes during debugging.

Each FLEX 10KE device contains an embedded array and a logic array. The embedded array is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), wide data-path manipulation, microcontroller applications, and data-transformation functions. The logic array performs the same function as the sea-of-gates in the gate array and is used to implement general logic such as counters, adders, state machines, and multiplexers. The combination of embedded and logic arrays provides the high performance and high density of embedded gate arrays, enabling designers to implement an entire system on a single device.

FLEX 10KE devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers the EPC1, EPC2, and EPC16 configuration devices, which configure FLEX 10KE devices via a serial data stream. Configuration data can also be downloaded from system RAM or via the Altera BitBlaster™, ByteBlasterMV™, or MasterBlaster download cables. After a FLEX 10KE device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 85 ms, real-time changes can be made during system operation.

FLEX 10KE devices contain an interface that permits microprocessors to configure FLEX 10KE devices serially or in-parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat a FLEX 10KE device as memory and configure it by writing to a virtual memory location, making it easy to reconfigure the device.

Figure 4. FLEX 10KE Device in Single-Port RAM Mode



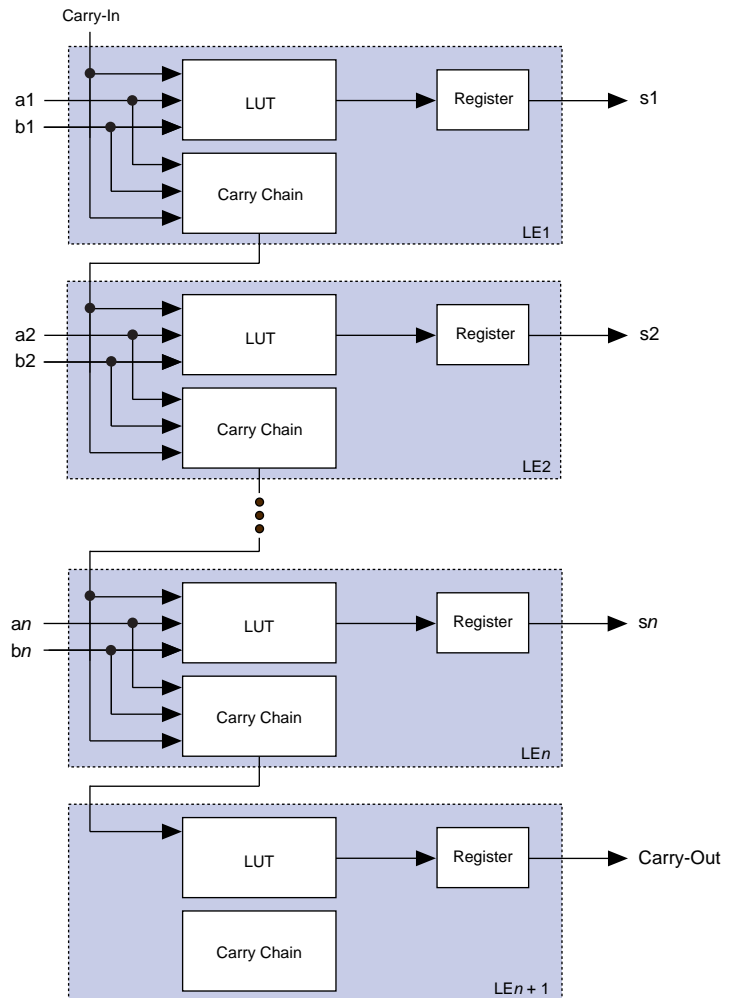
**Note:**

- (1) EPF10K30E, EPF10K50E, and EPF10K50S devices have 88 EAB local interconnect channels; EPF10K100E, EPF10K130E, EPF10K200E, and EPF10K200S devices have 104 EAB local interconnect channels.

EABs can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the write enable signal. In contrast, the EAB's synchronous RAM generates its own write enable signal and is self-timed with respect to the input or write clock. A circuit using the EAB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

Figure 9 shows how an  $n$ -bit full adder can be implemented in  $n + 1$  LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for an accumulator function. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal.

Figure 9. FLEX 10KE Carry Chain Operation ( $n$ -Bit Full Adder)



### Clearable Counter Mode

The clearable counter mode is similar to the up/down counter mode, but supports a synchronous clear instead of the up/down control. The clear function is substituted for the cascade-in signal in the up/down counter mode. Use 2 three-input LUTs: one generates the counter data, and the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer. The output of this multiplexer is ANDed with a synchronous clear signal.

### *Internal Tri-State Emulation*

Internal tri-state emulation provides internal tri-states without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable (OE) signals select which signal drives the bus. However, if multiple OE signals are active, contending signals can be driven onto the bus. Conversely, if no OE signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The Altera software automatically implements tri-state bus functionality with a multiplexer.

### *Clear & Preset Logic Control*

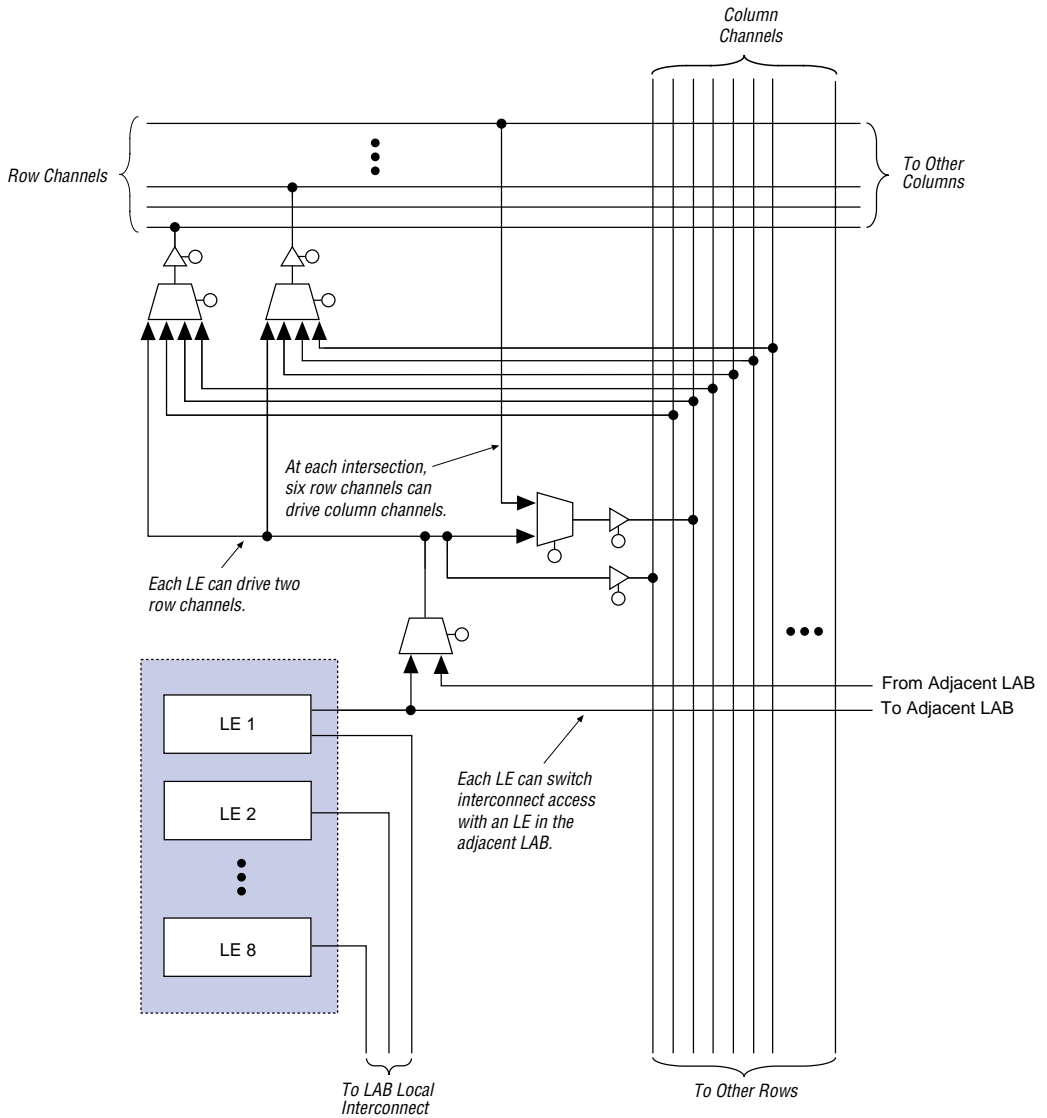
Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. The clear and preset control structure of the LE asynchronously loads signals into a register. Either LABCTRL1 or LABCTRL2 can control the asynchronous clear. Alternatively, the register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

During compilation, the Altera Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six modes chosen during design entry:

- Asynchronous clear
- Asynchronous preset
- Asynchronous clear and preset
- Asynchronous load with clear
- Asynchronous load with preset
- Asynchronous load without clear or preset

Figure 13. FLEX 10KE LAB Connections to Row & Column Interconnect



*Row-to-IOE Connections*

When an IOE is used as an input signal, it can drive two separate row channels. The signal is accessible by all LEs within that row. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the row channels. Up to eight IOEs connect to each side of each row channel (see Figure 16).

**Figure 16. FLEX 10KE Row-to-IOE Connections**

The values for  $m$  and  $n$  are provided in Table 10.

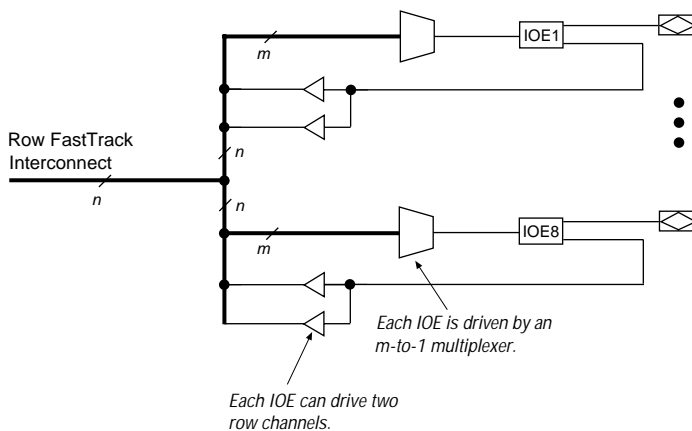


Table 10 lists the FLEX 10KE row-to-IOE interconnect resources.

<i>Table 10. FLEX 10KE Row-to-IOE Interconnect Resources</i>		
Device	Channels per Row ( $n$ )	Row Channels per Pin ( $m$ )
EPF10K30E	216	27
EPF10K50E EPF10K50S	216	27
EPF10K100E	312	39
EPF10K130E	312	39
EPF10K200E EPF10K200S	312	39

Tables 12 and 13 summarize the ClockLock and ClockBoost parameters for -1 and -2 speed-grade devices, respectively.

*Table 12. ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices*

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_R$	Input rise time				5	ns
$t_F$	Input fall time				5	ns
$t_{INDUTY}$	Input duty cycle		40		60	%
$f_{CLK1}$	Input clock frequency (ClockBoost clock multiplication factor equals 1)		25		180	MHz
$f_{CLK2}$	Input clock frequency (ClockBoost clock multiplication factor equals 2)		16		90	MHz
$f_{CLKDEV}$	Input deviation from user specification in the MAX+PLUS II software (1)				25,000 (2)	PPM
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)				100	ps
$t_{LOCK}$	Time required for ClockLock or ClockBoost to acquire lock (3)				10	$\mu$ s
$t_{JITTER}$	Jitter on ClockLock or ClockBoost-generated clock (4)	$t_{INCLKSTB} < 100$			250	ps
		$t_{INCLKSTB} < 50$			200 (4)	ps
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		40	50	60	%



The  $V_{CCINT}$  pins must always be connected to a 2.5-V power supply. With a 2.5-V  $V_{CCINT}$  level, input voltages are compatible with 2.5-V, 3.3-V, and 5.0-V inputs. The  $V_{CCIO}$  pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When the  $V_{CCIO}$  pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the  $V_{CCIO}$  pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with  $V_{CCIO}$  levels higher than 3.0 V achieve a faster timing delay of  $t_{OD2}$  instead of  $t_{OD1}$ .

Table 14 summarizes FLEX 10KE MultiVolt I/O support.

$V_{CCIO}$ (V)	Input Signal (V)			Output Signal (V)		
	2.5	3.3	5.0	2.5	3.3	5.0
2.5	✓	✓ (1)	✓ (1)	✓		
3.3	✓	✓	✓ (1)	✓ (2)	✓	✓

**Notes:**

- (1) The PCI clamping diode must be disabled to drive an input with voltages higher than  $V_{CCIO}$ .
- (2) When  $V_{CCIO} = 3.3$  V, a FLEX 10KE device can drive a 2.5-V device that has 3.3-V tolerant inputs.

Open-drain output pins on FLEX 10KE devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a  $V_{IH}$  of 3.5 V. When the open-drain pin is active, it will drive low. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The  $I_{OL}$  current specification should be considered when selecting a pull-up resistor.

### Power Sequencing & Hot-Socketing

Because FLEX 10KE devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The  $V_{CCIO}$  and  $V_{CCINT}$  power planes can be powered in any order.

Signals can be driven into FLEX 10KE devices before and during power up without damaging the device. Additionally, FLEX 10KE devices do not drive out during power up. Once operating conditions are reached, FLEX 10KE devices operate as specified by the user.

*Table 17. 32-Bit IDCODE for FLEX 10KE Devices Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) (2)
EPF10K30E	0001	0001 0000 0011 0000	00001101110	1
EPF10K50E EPF10K50S	0001	0001 0000 0101 0000	00001101110	1
EPF10K100E	0010	0000 0001 0000 0000	00001101110	1
EPF10K130E	0001	0000 0001 0011 0000	00001101110	1
EPF10K200E EPF10K200S	0001	0000 0010 0000 0000	00001101110	1

**Notes:**

- (1) The most significant bit (MSB) is on the left.
- (2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

FLEX 10KE devices include weak pull-up resistors on the JTAG pins.



For more information, see the following documents:

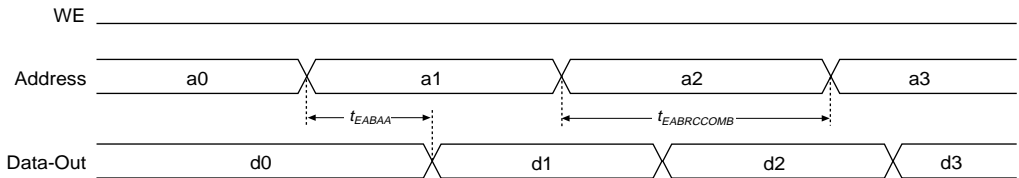
- [\*Application Note 39 \(IEEE Std. 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices\)\*](#)
- [\*BitBlaster Serial Download Cable Data Sheet\*](#)
- [\*ByteBlasterMV Parallel Port Download Cable Data Sheet\*](#)
- [\*Jam Programming & Test Language Specification\*](#)

Table 26. EAB Timing Microparameters <i>Note (1)</i>		
Symbol	Parameter	Conditions
$t_{EABDATA1}$	Data or address delay to EAB for combinatorial input	
$t_{EABDATA2}$	Data or address delay to EAB for registered input	
$t_{EABWE1}$	Write enable delay to EAB for combinatorial input	
$t_{EABWE2}$	Write enable delay to EAB for registered input	
$t_{EABRE1}$	Read enable delay to EAB for combinatorial input	
$t_{EABRE2}$	Read enable delay to EAB for registered input	
$t_{EABCLK}$	EAB register clock delay	
$t_{EABCO}$	EAB register clock-to-output delay	
$t_{EABYPASS}$	Bypass register delay	
$t_{EABSU}$	EAB register setup time before clock	
$t_{EABH}$	EAB register hold time after clock	
$t_{EABCLR}$	EAB register asynchronous clear time to output delay	
$t_{AA}$	Address access delay (including the read enable to output delay)	
$t_{WP}$	Write pulse width	
$t_{RP}$	Read pulse width	
$t_{WDSU}$	Data setup time before falling edge of write pulse	(5)
$t_{WDH}$	Data hold time after falling edge of write pulse	(5)
$t_{WASU}$	Address setup time before rising edge of write pulse	(5)
$t_{WAH}$	Address hold time after falling edge of write pulse	(5)
$t_{RASU}$	Address setup time with respect to the falling edge of the read enable	
$t_{RAH}$	Address hold time with respect to the falling edge of the read enable	
$t_{WO}$	Write enable to data output valid delay	
$t_{DD}$	Data-in to data-out valid delay	
$t_{EABOUT}$	Data-out delay	
$t_{EABCH}$	Clock high time	
$t_{EABCL}$	Clock low time	

Figures 29 and 30 show the asynchronous and synchronous timing waveforms, respectively, or the EAB macroparameters in Tables 26 and 27.

Figure 29. EAB Asynchronous Timing Waveforms

**EAB Asynchronous Read**



**EAB Asynchronous Write**

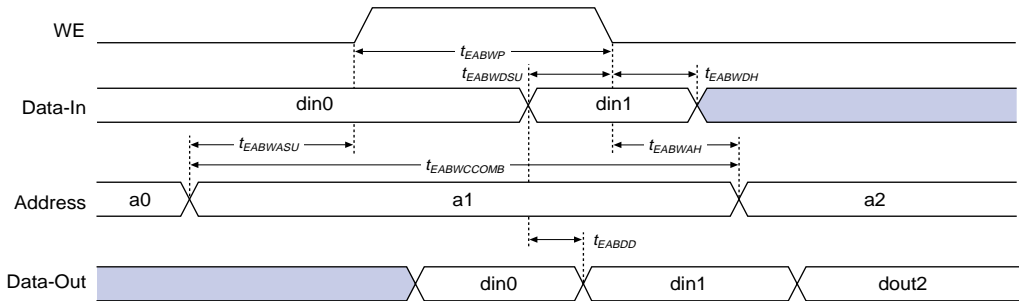
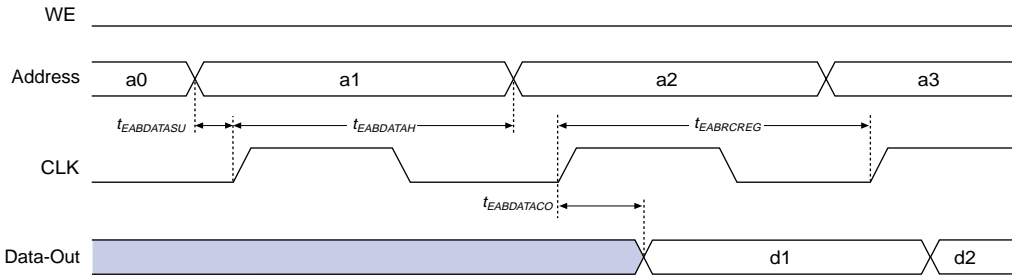
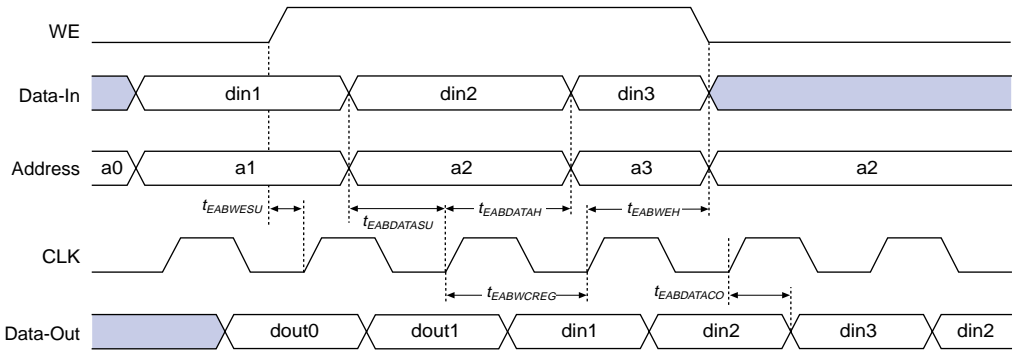


Figure 30. EAB Synchronous Timing Waveforms

**EAB Synchronous Read**



**EAB Synchronous Write (EAB Output Registers Used)**



Tables 31 through 37 show EPF10K30E device internal and external timing parameters.

**Table 31. EPF10K30E Device LE Timing Microparameters (Part 1 of 2) Note (1)**

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{LUT}$		0.7		0.8		1.1	ns
$t_{CLUT}$		0.5		0.6		0.8	ns
$t_{RLUT}$		0.6		0.7		1.0	ns
$t_{PACKED}$		0.3		0.4		0.5	ns
$t_{EN}$		0.6		0.8		1.0	ns
$t_{CICO}$		0.1		0.1		0.2	ns
$t_{CGEN}$		0.4		0.5		0.7	ns

**Table 31. EPF10K30E Device LE Timing Microparameters (Part 2 of 2)** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CGENR}$		0.1		0.1		0.2	ns
$t_{CASC}$		0.6		0.8		1.0	ns
$t_C$		0.0		0.0		0.0	ns
$t_{CO}$		0.3		0.4		0.5	ns
$t_{COMB}$		0.4		0.4		0.6	ns
$t_{SU}$	0.4		0.6		0.6		ns
$t_H$	0.7		1.0		1.3		ns
$t_{PRE}$		0.8		0.9		1.2	ns
$t_{CLR}$		0.8		0.9		1.2	ns
$t_{CH}$	2.0		2.5		2.5		ns
$t_{CL}$	2.0		2.5		2.5		ns

**Table 32. EPF10K30E Device IOE Timing Microparameters** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{IOD}$		2.4		2.8		3.8	ns
$t_{IOC}$		0.3		0.4		0.5	ns
$t_{IOCO}$		1.0		1.1		1.6	ns
$t_{IOCOMB}$		0.0		0.0		0.0	ns
$t_{IOSU}$	1.2		1.4		1.9		ns
$t_{IOH}$	0.3		0.4		0.5		ns
$t_{IOCLR}$		1.0		1.1		1.6	ns
$t_{OD1}$		1.9		2.3		3.0	ns
$t_{OD2}$		1.4		1.8		2.5	ns
$t_{OD3}$		4.4		5.2		7.0	ns
$t_{XZ}$		2.7		3.1		4.3	ns
$t_{ZX1}$		2.7		3.1		4.3	ns
$t_{ZX2}$		2.2		2.6		3.8	ns
$t_{ZX3}$		5.2		6.0		8.3	ns
$t_{INREG}$		3.4		4.1		5.5	ns
$t_{IOFD}$		0.8		1.3		2.4	ns
$t_{INCOMB}$		0.8		1.3		2.4	ns

Table 35. EPF10K30E Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		1.8		2.4		2.9	ns
$t_{DIN2LE}$		1.5		1.8		2.4	ns
$t_{DIN2DATA}$		1.5		1.8		2.2	ns
$t_{DCLK2IOE}$		2.2		2.6		3.0	ns
$t_{DCLK2LE}$		1.5		1.8		2.4	ns
$t_{SAMELAB}$		0.1		0.2		0.3	ns
$t_{SAMEROW}$		2.0		2.4		2.7	ns
$t_{SAMECOLUMN}$		0.7		1.0		0.8	ns
$t_{DIFFROW}$		2.7		3.4		3.5	ns
$t_{TROWROWS}$		4.7		5.8		6.2	ns
$t_{LEPERIPH}$		2.7		3.4		3.8	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.8		0.8		1.1	ns

Table 36. EPF10K30E External Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DRR}$		8.0		9.5		12.5	ns
$t_{INSU}^{(3)}$	2.1		2.5		3.9		ns
$t_{INH}^{(3)}$	0.0		0.0		0.0		ns
$t_{OUTCO}^{(3)}$	2.0	4.9	2.0	5.9	2.0	7.6	ns
$t_{INSU}^{(4)}$	1.1		1.5		–		ns
$t_{INH}^{(4)}$	0.0		0.0		–		ns
$t_{OUTCO}^{(4)}$	0.5	3.9	0.5	4.9	–	–	ns
$t_{PCISU}$	3.0		4.2		–		ns
$t_{PCIH}$	0.0		0.0		–		ns
$t_{PCICO}$	2.0	6.0	2.0	7.5	–	–	ns

**Table 37. EPF10K30E External Bidirectional Timing Parameters** *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$ (3)	2.8		3.9		5.2		ns
$t_{\text{INHBIDIR}}$ (3)	0.0		0.0		0.0		ns
$t_{\text{INSUBIDIR}}$ (4)	3.8		4.9		–		ns
$t_{\text{INHBIDIR}}$ (4)	0.0		0.0		–		ns
$t_{\text{OUTCOBIDIR}}$ (3)	2.0	4.9	2.0	5.9	2.0	7.6	ns
$t_{\text{XZBIDIR}}$ (3)		6.1		7.5		9.7	ns
$t_{\text{ZXBIDIR}}$ (3)		6.1		7.5		9.7	ns
$t_{\text{OUTCOBIDIR}}$ (4)	0.5	3.9	0.5	4.9	–	–	ns
$t_{\text{XZBIDIR}}$ (4)		5.1		6.5		–	ns
$t_{\text{ZXBIDIR}}$ (4)		5.1		6.5		–	ns

**Notes to tables:**

- (1) All timing parameters are described in Tables 24 through 30 in this data sheet.
- (2) These parameters are specified by characterization.
- (3) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
- (4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 38 through 44 show EPF10K50E device internal and external timing parameters.

**Table 38. EPF10K50E Device LE Timing Microparameters (Part 1 of 2)** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{LUT}}$		0.6		0.9		1.3	ns
$t_{\text{CLUT}}$		0.5		0.6		0.8	ns
$t_{\text{RLUT}}$		0.7		0.8		1.1	ns
$t_{\text{PACKED}}$		0.4		0.5		0.6	ns
$t_{\text{EN}}$		0.6		0.7		0.9	ns
$t_{\text{CICO}}$		0.2		0.2		0.3	ns
$t_{\text{CGEN}}$		0.5		0.5		0.8	ns
$t_{\text{CGENR}}$		0.2		0.2		0.3	ns
$t_{\text{CASC}}$		0.8		1.0		1.4	ns
$t_{\text{C}}$		0.5		0.6		0.8	ns
$t_{\text{CO}}$		0.7		0.7		0.9	ns
$t_{\text{COMB}}$		0.5		0.6		0.8	ns
$t_{\text{SU}}$	0.7		0.7		0.8		ns



*Table 50. EPF10K100E External Timing Parameters*    *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{DRR}}$		9.0		12.0		16.0	ns
$t_{\text{INSU}}^{(3)}$	2.0		2.5		3.3		ns
$t_{\text{INH}}^{(3)}$	0.0		0.0		0.0		ns
$t_{\text{OUTCO}}^{(3)}$	2.0	5.2	2.0	6.9	2.0	9.1	ns
$t_{\text{INSU}}^{(4)}$	2.0		2.2		–		ns
$t_{\text{INH}}^{(4)}$	0.0		0.0		–		ns
$t_{\text{OUTCO}}^{(4)}$	0.5	3.0	0.5	4.6	–	–	ns
$t_{\text{PCISU}}$	3.0		6.2		–		ns
$t_{\text{PCIH}}$	0.0		0.0		–		ns
$t_{\text{PCICO}}$	2.0	6.0	2.0	6.9	–	–	ns

*Table 51. EPF10K100E External Bidirectional Timing Parameters*    *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}^{(3)}$	1.7		2.5		3.3		ns
$t_{\text{INHBIDIR}}^{(3)}$	0.0		0.0		0.0		ns
$t_{\text{INSUBIDIR}}^{(4)}$	2.0		2.8		–		ns
$t_{\text{INHBIDIR}}^{(4)}$	0.0		0.0		–		ns
$t_{\text{OUTCOBIDIR}}^{(3)}$	2.0	5.2	2.0	6.9	2.0	9.1	ns
$t_{\text{XZBIDIR}}^{(3)}$		5.6		7.5		10.1	ns
$t_{\text{ZXBIDIR}}^{(3)}$		5.6		7.5		10.1	ns
$t_{\text{OUTCOBIDIR}}^{(4)}$	0.5	3.0	0.5	4.6	–	–	ns
$t_{\text{XZBIDIR}}^{(4)}$		4.6		6.5		–	ns
$t_{\text{ZXBIDIR}}^{(4)}$		4.6		6.5		–	ns

**Notes to tables:**

- (1) All timing parameters are described in Tables 24 through 30 in this data sheet.
- (2) These parameters are specified by characterization.
- (3) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
- (4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

**Table 64. EPF10K200E External Timing Parameters** *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{DRR}}$		10.0		12.0		16.0	ns
$t_{\text{INSU}}$	2.8		3.4		4.4		ns
$t_{\text{INH}}$	0.0		0.0		0.0		ns
$t_{\text{OUTCO}}$	2.0	4.5	2.0	5.3	2.0	7.8	ns
$t_{\text{PCISU}}$	3.0		6.2		-		ns
$t_{\text{PCIH}}$	0.0		0.0		-		ns
$t_{\text{PCICO}}$	2.0	6.0	2.0	8.9	-	-	ns

**Table 65. EPF10K200E External Bidirectional Timing Parameters** *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	3.0		4.0		5.5		ns
$t_{\text{INHBIDIR}}$	0.0		0.0		0.0		ns
$t_{\text{OUTCOBIDIR}}$	2.0	4.5	2.0	5.3	2.0	7.8	ns
$t_{\text{XZBIDIR}}$		8.1		9.5		13.0	ns
$t_{\text{ZXBIDIR}}$		8.1		9.5		13.0	ns

**Notes to tables:**

- (1) All timing parameters are described in Tables 24 through 30 in this data sheet.
- (2) These parameters are specified by characterization.

Tables 66 through 79 show EPF10K50S and EPF10K200S device external timing parameters.

**Table 66. EPF10K50S Device LE Timing Microparameters (Part 1 of 2)** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{LUT}}$		0.6		0.8		1.1	ns
$t_{\text{CLUT}}$		0.5		0.6		0.8	ns
$t_{\text{RLUT}}$		0.6		0.7		0.9	ns
$t_{\text{PACKED}}$		0.2		0.3		0.4	ns
$t_{\text{EN}}$		0.6		0.7		0.9	ns
$t_{\text{CICO}}$		0.1		0.1		0.1	ns
$t_{\text{CGEN}}$		0.4		0.5		0.6	ns

**Table 69. EPF10K50S Device EAB Internal Timing Macroparameters** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABAA}$		3.7		5.2		7.0	ns
$t_{EABRCCOMB}$	3.7		5.2		7.0		ns
$t_{EABRCREG}$	3.5		4.9		6.6		ns
$t_{EABWP}$	2.0		2.8		3.8		ns
$t_{EABWCCOMB}$	4.5		6.3		8.6		ns
$t_{EABWCREG}$	5.6		7.8		10.6		ns
$t_{EABDD}$		3.8		5.3		7.2	ns
$t_{EABDATACO}$		0.8		1.1		1.5	ns
$t_{EABDATASU}$	1.1		1.6		2.1		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	0.7		1.0		1.3		ns
$t_{EABWEH}$	0.4		0.6		0.8		ns
$t_{EABWDSU}$	1.2		1.7		2.2		ns
$t_{EABWDH}$	0.0		0.0		0.0		ns
$t_{EABWASU}$	1.6		2.3		3.0		ns
$t_{EABWAH}$	0.9		1.2		1.8		ns
$t_{EABWO}$		3.1		4.3		5.9	ns

**Table 70. EPF10K50S Device Interconnect Timing Microparameters** *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		3.1		3.7		4.6	ns
$t_{DIN2LE}$		1.7		2.1		2.7	ns
$t_{DIN2DATA}$		2.7		3.1		5.1	ns
$t_{DCLK2IOE}$		1.6		1.9		2.6	ns
$t_{DCLK2LE}$		1.7		2.1		2.7	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		1.5		1.7		2.4	ns
$t_{SAMECOLUMN}$		1.0		1.3		2.1	ns
$t_{DIFFROW}$		2.5		3.0		4.5	ns
$t_{TWOROWS}$		4.0		4.7		6.9	ns
$t_{LEPERIPH}$		2.6		2.9		3.4	ns
$t_{LABCARRY}$		0.1		0.2		0.2	ns
$t_{LABCASC}$		0.8		1.0		1.3	ns

Table 73. EPF10K200S Device Internal & External Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{LUT}$		0.7		0.8		1.2	ns
$t_{CLUT}$		0.4		0.5		0.6	ns
$t_{RLUT}$		0.5		0.7		0.9	ns
$t_{PACKED}$		0.4		0.5		0.7	ns
$t_{EN}$		0.6		0.5		0.6	ns
$t_{CICO}$		0.1		0.2		0.3	ns
$t_{CGEN}$		0.3		0.4		0.6	ns
$t_{CGENR}$		0.1		0.2		0.3	ns
$t_{CASC}$		0.7		0.8		1.2	ns
$t_C$		0.5		0.6		0.8	ns
$t_{CO}$		0.5		0.6		0.8	ns
$t_{COMB}$		0.3		0.6		0.8	ns
$t_{SU}$	0.4		0.6		0.7		ns
$t_H$	1.0		1.1		1.5		ns
$t_{PRE}$		0.4		0.6		0.8	ns
$t_{CLR}$		0.5		0.6		0.8	ns
$t_{CH}$	2.0		2.5		3.0		ns
$t_{CL}$	2.0		2.5		3.0		ns

Table 74. EPF10K200S Device IOE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{IOD}$		1.8		1.9		2.6	ns
$t_{IOC}$		0.3		0.3		0.5	ns
$t_{IOCO}$		1.7		1.9		2.6	ns
$t_{IOCOMB}$		0.5		0.6		0.8	ns
$t_{IOSU}$	0.8		0.9		1.2		ns
$t_{IOH}$	0.4		0.8		1.1		ns
$t_{IOCLR}$		0.2		0.2		0.3	ns
$t_{OD1}$		1.3		0.7		0.9	ns
$t_{OD2}$		0.8		0.2		0.4	ns
$t_{OD3}$		2.9		3.0		3.9	ns
$t_{XZ}$		5.0		5.3		7.1	ns
$t_{ZX1}$		5.0		5.3		7.1	ns

## Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the Altera Digital Library for pin-out information.

## Revision History

The information contained in the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.5 supersedes information published in previous versions.

### Version 2.5

The following changes were made to the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.5:

- *Note (1)* added to **Figure 23**.
- Text added to “**I/O Element**” section on **page 34**.
- Updated **Table 22**.

### Version 2.4

The following changes were made to the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.4: updated text on **page 34** and **page 63**.