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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 360 |
| Number of Logic Elements/Cells | 2880 |
| Total RAM Bits | 40960 |
| Number of I/O | 220 |
| Number of Gates | 199000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 356-LBGA |
| Supplier Device Package | 356-BGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epf10k50sbc356-2 |

*Table 4. FLEX 10KE Package Sizes*

| Device | 144-Pin TQFP | 208-Pin PQFP | 240-Pin PQFP RQFP | 256-Pin FineLine BGA | 356-Pin BGA | 484-Pin FineLine BGA | 599-Pin PGA | 600-Pin BGA | 672-Pin FineLine BGA |
|---|---|---|---|---|---|---|---|---|---|
| Pitch (mm) | 0.50 | 0.50 | 0.50 | 1.0 | 1.27 | 1.0 | – | 1.27 | 1.0 |
| Area ($mm^2$) | 484 | 936 | 1,197 | 289 | 1,225 | 529 | 3,904 | 2,025 | 729 |
| Length × width (mm × mm) | 22 × 22 | 30.6 × 30.6 | 34.6 × 34.6 | 17 × 17 | 35 × 35 | 23 × 23 | 62.5 × 62.5 | 45 × 45 | 27 × 27 |

# General Description

Altera FLEX 10KE devices are enhanced versions of FLEX 10K devices. Based on reconfigurable CMOS SRAM elements, the FLEX architecture incorporates all features necessary to implement common gate array megafunctions. With up to 200,000 typical gates, FLEX 10KE devices provide the density, speed, and features to integrate entire systems, including multiple 32-bit buses, into a single device.

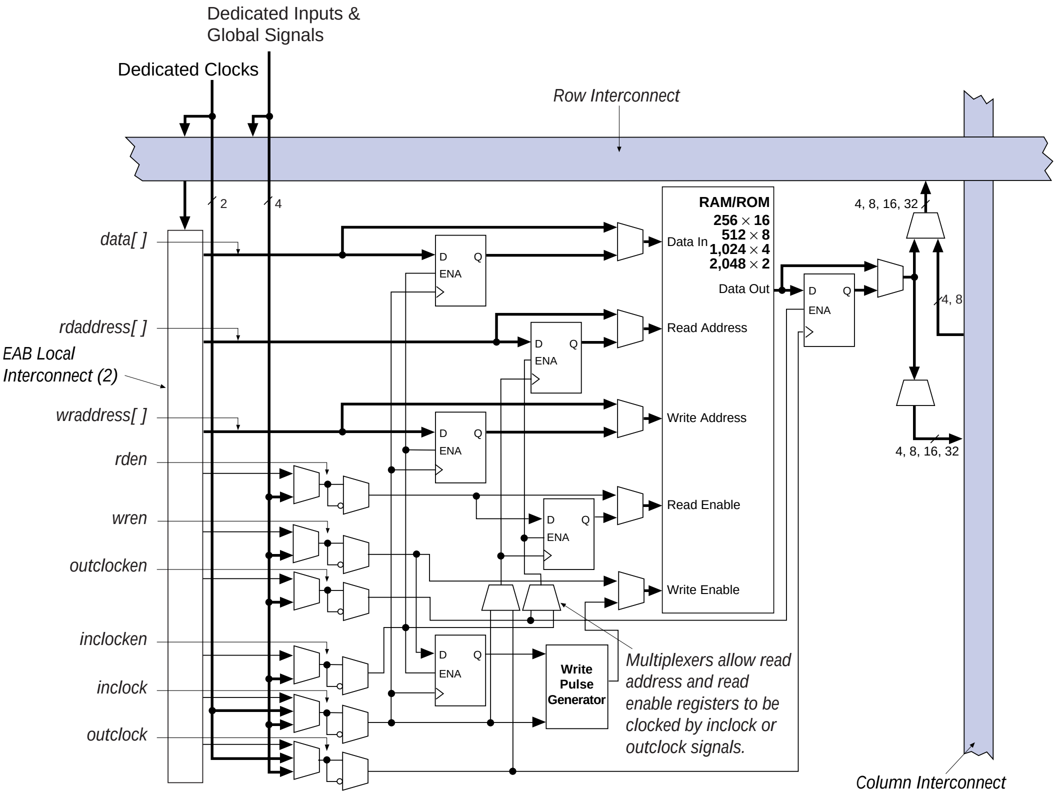
The ability to reconfigure FLEX 10KE devices enables 100% testing prior to shipment and allows the designer to focus on simulation and design verification. FLEX 10KE reconfigurability eliminates inventory management for gate array designs and generation of test vectors for fault coverage.

Table 5 shows FLEX 10KE performance for some common designs. All performance values were obtained with Synopsys DesignWare or LPM functions. Special design techniques are not required to implement the applications; the designer simply infers or instantiates a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

The EAB can also be used for bidirectional, dual-port memory applications where two ports read or write simultaneously. To implement this type of dual-port memory, two EABs are used to support two simultaneous read or writes.

Alternatively, one clock and clock enable can be used to control the input registers of the EAB, while a different clock and clock enable control the output registers (see Figure 2).

**Figure 2. FLEX 10KE Device in Dual-Port RAM Mode** *Notes (1)*

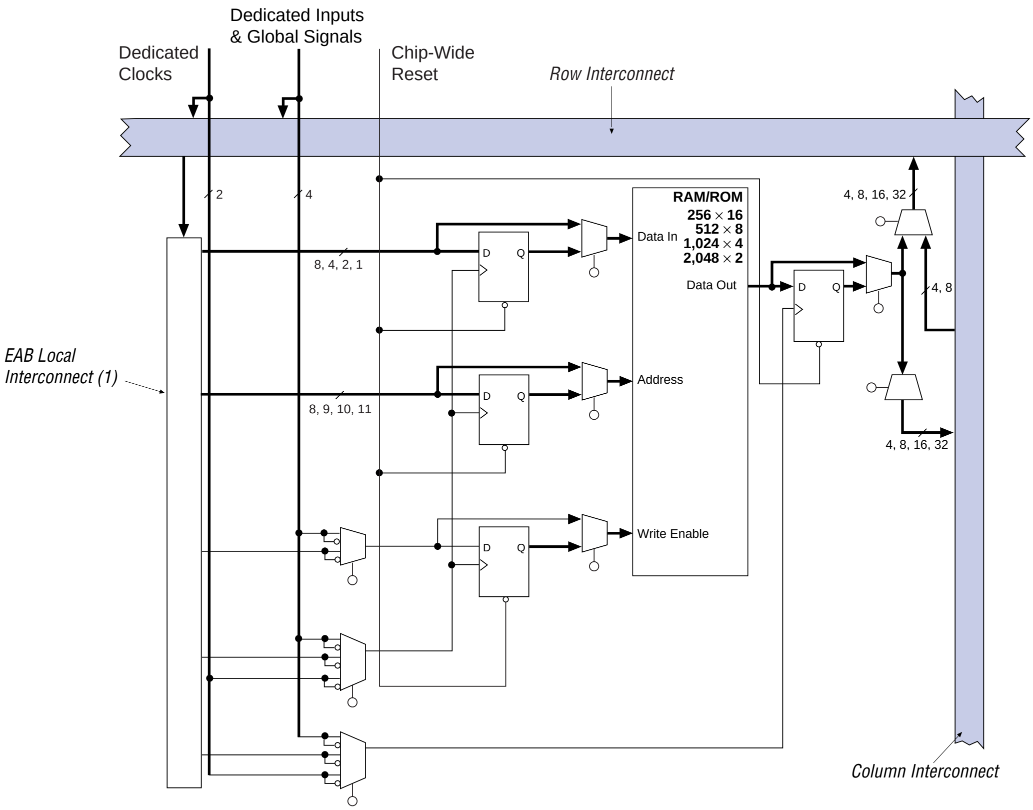



***Notes:***

(1) All registers can be asynchronously cleared by EAB local interconnect signals, global signals, or the chip-wide reset.

(2) EPF10K30E and EPF10K50E devices have 88 EAB local interconnect channels; EPF10K100E, EPF10K130E, and EPF10K200E devices have 104 EAB local interconnect channels.

***Figure 4. FLEX 10KE Device in Single-Port RAM Mode***




**Note:**

(1) EPF10K30E, EPF10K50E, and EPF10K50S devices have 88 EAB local interconnect channels; EPF10K100E, EPF10K130E, EPF10K200E, and EPF10K200S devices have 104 EAB local interconnect channels.

EABs can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the write enable signal. In contrast, the EAB's synchronous RAM generates its own write enable signal and is self-timed with respect to the input or write clock. A circuit using the EAB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

### Asynchronous Clear

The flipflop can be cleared by either LABCTRL1 or LABCTRL2. In this mode, the preset signal is tied to VCC to deactivate it.

### Asynchronous Preset

An asynchronous preset is implemented as an asynchronous load, or with an asynchronous clear. If DATA3 is tied to VCC, asserting LABCTRL1 asynchronously loads a one into the register. Alternatively, the Altera software can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used for one of the LE operating modes.

### Asynchronous Preset & Clear

When implementing asynchronous clear and preset, LABCTRL1 controls the preset and LABCTRL2 controls the clear. DATA3 is tied to VCC, so that asserting LABCTRL1 asynchronously loads a one into the register, effectively presetting the register. Asserting LABCTRL2 clears the register.

### Asynchronous Load with Clear

When implementing an asynchronous load in conjunction with the clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear. LABCTRL2 implements the clear by controlling the register clear; LABCTRL2 does not have to feed the preset circuits.

### Asynchronous Load with Preset

When implementing an asynchronous load in conjunction with preset, the Altera software provides preset control by using the clear and inverting the input and output of the register. Asserting LABCTRL2 presets the register, while asserting LABCTRL1 loads the register. The Altera software inverts the signal that drives DATA3 to account for the inversion of the register's output.

### Asynchronous Load without Preset or Clear

When implementing an asynchronous load without preset or clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear.

## FastTrack Interconnect Routing Structure

In the FLEX 10KE architecture, connections between LEs, EABs, and device I/O pins are provided by the FastTrack Interconnect routing structure, which is a series of continuous horizontal and vertical routing channels that traverses the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect routing structure consists of row and column interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect. The row interconnect can drive I/O pins and feed other LABs in the row. The column interconnect routes signals between rows and can drive I/O pins.

Row channels drive into the LAB or EAB local interconnect. The row signal is buffered at every LAB or EAB to reduce the effect of fan-out on delay. A row channel can be driven by an LE or by one of three column channels. These four signals feed dual 4-to-1 multiplexers that connect to two specific row channels. These multiplexers, which are connected to each LE, allow column channels to drive row channels even when all eight LEs in a LAB drive the row interconnect.

Each column of LABs or EABs is served by a dedicated column interconnect. The column interconnect that serves the EABs has twice as many channels as other column interconnects. The column interconnect can then drive I/O pins or another row's interconnect to route the signals to other LABs or EABs in the device. A signal from the column interconnect, which can be either the output of a LE or an input from an I/O pin, must be routed to the row interconnect before it can enter a LAB or EAB. Each row channel that is driven by an IOE or EAB can drive one specific column channel.

Access to row and column channels can be switched between LEs in adjacent pairs of LABs. For example, a LE in one LAB can drive the row and column channels normally driven by a particular LE in the adjacent LAB in the same row, and vice versa. This flexibility enables routing resources to be used more efficiently (see Figure 13).

For improved routing, the row interconnect consists of a combination of full-length and half-length channels. The full-length channels connect to all LABs in a row; the half-length channels connect to the LABs in half of the row. The EAB can be driven by the half-length channels in the left half of the row and by the full-length channels. The EAB drives out to the full-length channels. In addition to providing a predictable, row-wide interconnect, this architecture provides increased routing resources. Two neighboring LABs can be connected using a half-row channel, thereby saving the other half of the channel for the other half of the row.

Table 7 summarizes the FastTrack Interconnect routing structure resources available in each FLEX 10KE device.

***Table 7. FLEX 10KE FastTrack Interconnect Resources***

| Device | Rows | Channels per Row | Columns | Channels per Column |
|---|---|---|---|---|
| EPF10K30E | 6 | 216 | 36 | 24 |
| EPF10K50E<br>EPF10K50S | 10 | 216 | 36 | 24 |
| EPF10K100E | 12 | 312 | 52 | 24 |
| EPF10K130E | 16 | 312 | 52 | 32 |
| EPF10K200E<br>EPF10K200S | 24 | 312 | 52 | 48 |

In addition to general-purpose I/O pins, FLEX 10KE devices have six dedicated input pins that provide low-skew signal distribution across the device. These six inputs can be used for global clock, clear, preset, and peripheral output enable and clock enable control signals. These signals are available as control signals for all LABs and IOEs in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device.

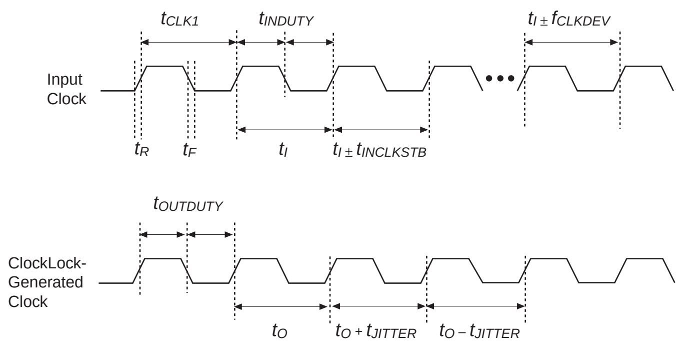
Figure 14 shows the interconnection of adjacent LABs and EABs, with row, column, and local interconnects, as well as the associated cascade and carry chains. Each LAB is labeled according to its location: a letter represents the row and a number represents the column. For example, LAB B3 is in row B, column 3.

## ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. Figure 19 shows the incoming and generated clock specifications.

***Figure 19. Specifications for Incoming & Generated Clocks***

*The $t_I$ parameter refers to the nominal input clock period; the $t_O$ parameter refers to the nominal output clock period.*



Tables 12 and 13 summarize the ClockLock and ClockBoost parameters for -1 and -2 speed-grade devices, respectively.

**Table 12. ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_R$ | Input rise time | | | | 5 | ns |
| $t_F$ | Input fall time | | | | 5 | ns |
| $t_{INDUTY}$ | Input duty cycle | | 40 | | 60 | % |
| $f_{CLK1}$ | Input clock frequency (ClockBoost clock multiplication factor equals 1) | | 25 | | 180 | MHz |
| $f_{CLK2}$ | Input clock frequency (ClockBoost clock multiplication factor equals 2) | | 16 | | 90 | MHz |
| $f_{CLKDEV}$ | Input deviation from user specification in the MAX+PLUS II software *(1)* | | | | 25,000 *(2)* | PPM |
| $t_{INCLKSTB}$ | Input clock stability (measured between adjacent clocks) | | | | 100 | ps |
| $t_{LOCK}$ | Time required for ClockLock or ClockBoost to acquire lock *(3)* | | | | 10 | µs |
| $t_{JITTER}$ | Jitter on ClockLock or ClockBoost-generated clock *(4)* | $t_{INCLKSTB} < 100$ | | | 250 | ps |
| | | $t_{INCLKSTB} < 50$ | | | 200 *(4)* | ps |
| $t_{OUTDUTY}$ | Duty cycle for ClockLock or ClockBoost-generated clock | | 40 | 50 | 60 | % |

*Table 13. ClockLock & ClockBoost Parameters for -2 Speed-Grade Devices*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_R$ | Input rise time | | | | 5 | ns |
| $t_F$ | Input fall time | | | | 5 | ns |
| $t_{INDUTY}$ | Input duty cycle | | 40 | | 60 | % |
| $f_{CLK1}$ | Input clock frequency (ClockBoost clock multiplication factor equals 1) | | 25 | | 75 | MHz |
| $f_{CLK2}$ | Input clock frequency (ClockBoost clock multiplication factor equals 2) | | 16 | | 37.5 | MHz |
| $f_{CLKDEV}$ | Input deviation from user specification in the MAX+PLUS II software *(1)* | | | | 25,000 *(2)* | PPM |
| $t_{INCLKSTB}$ | Input clock stability (measured between adjacent clocks) | | | | 100 | ps |
| $t_{LOCK}$ | Time required for ClockLock or ClockBoost to acquire lock *(3)* | | | | 10 | µs |
| $t_{JITTER}$ | Jitter on ClockLock or ClockBoost-generated clock *(4)* | $t_{INCLKSTB}$ < 100 | | | 250 | ps |
| | | $t_{INCLKSTB}$ < 50 | | | 200 *(4)* | ps |
| $t_{OUTDUTY}$ | Duty cycle for ClockLock or ClockBoost-generated clock | | 40 | 50 | 60 | % |

***Notes to tables:***

(1) To implement the ClockLock and ClockBoost circuitry with the MAX+PLUS II software, designers must specify the input frequency. The Altera software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The $f_{CLKDEV}$ parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.

(2) Twenty-five thousand parts per million (PPM) equates to 2.5% of input clock period.

(3) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration because the $t_{LOCK}$ value is less than the time required for configuration.

(4) The $t_{JITTER}$ specification is measured under long-term observation. The maximum value for $t_{JITTER}$ is 200 ps if $t_{INCLKSTB}$ is lower than 50 ps.

## I/O Configuration

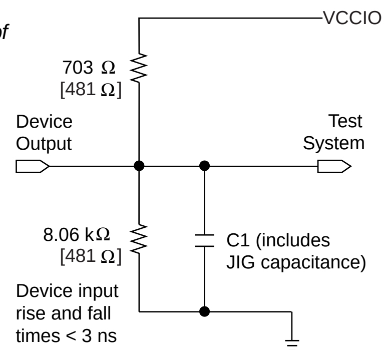
This section discusses the peripheral component interconnect (PCI) pull-up clamping diode option, slew-rate control, open-drain output option, and MultiVolt I/O interface for FLEX 10KE devices. The PCI pull-up clamping diode, slew-rate control, and open-drain output options are controlled pin-by-pin via Altera software logic options. The MultiVolt I/O interface is controlled by connecting $V_{CCIO}$ to a different voltage than $V_{CCINT}$. Its effect can be simulated in the Altera software via the **Global Project Device Options** dialog box (Assign menu).

## Generic Testing

Each FLEX 10KE device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for FLEX 10KE devices are made under conditions equivalent to those shown in Figure 21. Multiple test patterns can be used to configure devices during all stages of the production flow.

***Figure 21. FLEX 10KE AC Test Conditions***

*Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V devices or outputs. Numbers without brackets are for 3.3-V. devices or outputs.*




## Operating Conditions

Tables 19 through 23 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V FLEX 10KE devices.

***Table 19. FLEX 10KE 2.5-V Device Absolute Maximum Ratings*** *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage | With respect to ground *(2)* | –0.5 | 3.6 | V |
| $V_{CCIO}$ | | | –0.5 | 4.6 | V |
| $V_I$ | DC input voltage | | –2.0 | 5.75 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | PQFP, TQFP, BGA, and FineLine BGA packages, under bias | | 135 | ° C |
| | | Ceramic PGA packages, under bias | | 150 | ° C |

| Table 22. FLEX 10KE 2.5-V Device DC Operating Conditions *Notes (6), (7)* | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| $V_{IH}$ | High-level input voltage | | 1.7, 0.5 × $V_{CCIO}$ *(8)* | | 5.75 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | 0.8, 0.3 × $V_{CCIO}$ *(8)* | V |
| $V_{OH}$ | 3.3-V high-level TTL output voltage | $I_{OH}$ = –8 mA DC, $V_{CCIO}$ = 3.00 V *(9)* | 2.4 | | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(9)* | $V_{CCIO}$ – 0.2 | | | V |
| | 3.3-V high-level PCI output voltage | $I_{OH}$ = –0.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(9)* | 0.9 × $V_{CCIO}$ | | | V |
| | 2.5-V high-level output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 2.30 V *(9)* | 2.1 | | | V |
| | | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.30 V *(9)* | 2.0 | | | V |
| | | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.30 V *(9)* | 1.7 | | | V |
| $V_{OL}$ | 3.3-V low-level TTL output voltage | $I_{OL}$ = 12 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | | | 0.2 | V |
| | 3.3-V low-level PCI output voltage | $I_{OL}$ = 1.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(10)* | | | 0.1 × $V_{CCIO}$ | V |
| | 2.5-V low-level output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | | | 0.2 | V |
| | | $I_{OL}$ = 1 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | | | 0.4 | V |
| | | $I_{OL}$ = 2 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | | | 0.7 | V |
| $I_I$ | Input pin leakage current | $V_I$ = $V_{CCIOmax}$ to 0 V *(11)* | –10 | | 10 | μA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current | $V_O$ = $V_{CCIOmax}$ to 0 V *(11)* | –10 | | 10 | μA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) | $V_I$ = ground, no load, no toggling inputs | | 5 | | mA |
| | | $V_I$ = ground, no load, no toggling inputs *(12)* | | 10 | | mA |
| $R_{CONF}$ | Value of I/O pin pull-up resistor before and during configuration | $V_{CCIO}$ = 3.0 V *(13)* | 20 | | 50 | k¾ |
| | | $V_{CCIO}$ = 2.3 V *(13)* | 30 | | 80 | k¾ |

**Table 24. LE Timing Microparameters (Part 2 of 2)** *Note (1)*

| Symbol | Parameter | Condition |
|---|---|---|
| $t_{CLR}$ | LE register clear delay | |
| $t_{CH}$ | Minimum clock high time from clock pin | |
| $t_{CL}$ | Minimum clock low time from clock pin | |

**Table 25. IOE Timing Microparameters** *Note (1)*

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{IOD}$ | IOE data delay | |
| $t_{IOC}$ | IOE register control signal delay | |
| $t_{IOCO}$ | IOE register clock-to-output delay | |
| $t_{IOCOMB}$ | IOE combinatorial delay | |
| $t_{IOSU}$ | IOE register setup time for data and enable signals before clock; IOE register recovery time after asynchronous clear | |
| $t_{IOH}$ | IOE register hold time for data and enable signals after clock | |
| $t_{IOCLR}$ | IOE register clear time | |
| $t_{OD1}$ | Output buffer and pad delay, slow slew rate = off, $V_{CCIO}$ = 3.3 V | C1 = 35 pF *(2)* |
| $t_{OD2}$ | Output buffer and pad delay, slow slew rate = off, $V_{CCIO}$ = 2.5 V | C1 = 35 pF *(3)* |
| $t_{OD3}$ | Output buffer and pad delay, slow slew rate = on | C1 = 35 pF *(4)* |
| $t_{XZ}$ | IOE output buffer disable delay | |
| $t_{ZX1}$ | IOE output buffer enable delay, slow slew rate = off, $V_{CCIO}$ = 3.3 V | C1 = 35 pF *(2)* |
| $t_{ZX2}$ | IOE output buffer enable delay, slow slew rate = off, $V_{CCIO}$ = 2.5 V | C1 = 35 pF *(3)* |
| $t_{ZX3}$ | IOE output buffer enable delay, slow slew rate = on | C1 = 35 pF *(4)* |
| $t_{INREG}$ | IOE input pad and buffer to IOE register delay | |
| $t_{IOFD}$ | IOE register feedback delay | |
| $t_{INCOMB}$ | IOE input pad and buffer to FastTrack Interconnect delay | |

| *Table 33. EPF10K30E Device EAB Internal Microparameters* *Note (1)* | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **-1 Speed Grade** | | **-2 Speed Grade** | | **-3 Speed Grade** | | **Unit** |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{EABDATA1}$ | | 1.7 | | 2.0 | | 2.3 | ns |
| $t_{EABDATA1}$ | | 0.6 | | 0.7 | | 0.8 | ns |
| $t_{EABWE1}$ | | 1.1 | | 1.3 | | 1.4 | ns |
| $t_{EABWE2}$ | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{EABRE1}$ | | 0.8 | | 0.9 | | 1.0 | ns |
| $t_{EABRE2}$ | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{EABCLK}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCO}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{EABBYPASS}$ | | 0.5 | | 0.6 | | 0.7 | ns |
| $t_{EABSU}$ | 0.9 | | 1.0 | | 1.2 | | ns |
| $t_{EABH}$ | 0.4 | | 0.4 | | 0.5 | | ns |
| $t_{EABCLR}$ | 0.3 | | 0.3 | | 0.3 | | ns |
| $t_{AA}$ | | 3.2 | | 3.8 | | 4.4 | ns |
| $t_{WP}$ | 2.5 | | 2.9 | | 3.3 | | ns |
| $t_{RP}$ | 0.9 | | 1.1 | | 1.2 | | ns |
| $t_{WDSU}$ | 0.9 | | 1.0 | | 1.1 | | ns |
| $t_{WDH}$ | 0.1 | | 0.1 | | 0.1 | | ns |
| $t_{WASU}$ | 1.7 | | 2.0 | | 2.3 | | ns |
| $t_{WAH}$ | 1.8 | | 2.1 | | 2.4 | | ns |
| $t_{RASU}$ | 3.1 | | 3.7 | | 4.2 | | ns |
| $t_{RAH}$ | 0.2 | | 0.2 | | 0.2 | | ns |
| $t_{WO}$ | | 2.5 | | 2.9 | | 3.3 | ns |
| $t_{DD}$ | | 2.5 | | 2.9 | | 3.3 | ns |
| $t_{EABOUT}$ | | 0.5 | | 0.6 | | 0.7 | ns |
| $t_{EABCH}$ | 1.5 | | 2.0 | | 2.3 | | ns |
| $t_{EABCL}$ | 2.5 | | 2.9 | | 3.3 | | ns |

**Table 41. EPF10K50E Device EAB Internal Timing Macroparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABAA}$ | | 6.4 | | 7.6 | | 10.2 | ns |
| $t_{EABRCOMB}$ | 6.4 | | 7.6 | | 10.2 | | ns |
| $t_{EABRCREG}$ | 4.4 | | 5.1 | | 7.0 | | ns |
| $t_{EABWP}$ | 2.5 | | 2.9 | | 3.9 | | ns |
| $t_{EABWCOMB}$ | 6.0 | | 7.0 | | 9.5 | | ns |
| $t_{EABWCREG}$ | 6.8 | | 7.8 | | 10.6 | | ns |
| $t_{EABDD}$ | | 5.7 | | 6.7 | | 9.0 | ns |
| $t_{EABDATACO}$ | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{EABDATASU}$ | 1.5 | | 1.7 | | 2.3 | | ns |
| $t_{EABDATAH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWESU}$ | 1.3 | | 1.4 | | 2.0 | | ns |
| $t_{EABWEH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWDSU}$ | 1.5 | | 1.7 | | 2.3 | | ns |
| $t_{EABWDH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWASU}$ | 3.0 | | 3.6 | | 4.8 | | ns |
| $t_{EABWAH}$ | 0.5 | | 0.5 | | 0.8 | | ns |
| $t_{EABWO}$ | | 5.1 | | 6.0 | | 8.1 | ns |

**Table 42. EPF10K50E Device Interconnect Timing Microparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DIN2IOE}$ | | 3.5 | | 4.3 | | 5.6 | ns |
| $t_{DIN2LE}$ | | 2.1 | | 2.5 | | 3.4 | ns |
| $t_{DIN2DATA}$ | | 2.2 | | 2.4 | | 3.1 | ns |
| $t_{DCLK2IOE}$ | | 2.9 | | 3.5 | | 4.7 | ns |
| $t_{DCLK2LE}$ | | 2.1 | | 2.5 | | 3.4 | ns |
| $t_{SAMELAB}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{SAMEROW}$ | | 1.1 | | 1.1 | | 1.5 | ns |
| $t_{SAMECOLUMN}$ | | 0.8 | | 1.0 | | 1.3 | ns |
| $t_{DIFFROW}$ | | 1.9 | | 2.1 | | 2.8 | ns |
| $t_{TWOROWS}$ | | 3.0 | | 3.2 | | 4.3 | ns |
| $t_{LEPERIPH}$ | | 3.1 | | 3.3 | | 3.7 | ns |
| $t_{LABCARRY}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{LABCASC}$ | | 0.3 | | 0.3 | | 0.5 | ns |

| *Table 45. EPF10K100E Device LE Timing Microparameters* *Note (1)* | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **-1 Speed Grade** | | **-2 Speed Grade** | | **-3 Speed Grade** | | **Unit** |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{CGENR}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CASC}$ | | 0.6 | | 0.9 | | 1.2 | ns |
| $t_C$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{CO}$ | | 0.6 | | 0.8 | | 1.1 | ns |
| $t_{COMB}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{SU}$ | 0.4 | | 0.6 | | 0.7 | | ns |
| $t_H$ | 0.5 | | 0.7 | | 0.9 | | ns |
| $t_{PRE}$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{CLR}$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{CH}$ | 1.5 | | 2.0 | | 2.5 | | ns |
| $t_{CL}$ | 1.5 | | 2.0 | | 2.5 | | ns |

| *Table 46. EPF10K100E Device IOE Timing Microparameters* *Note (1)* | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **-1 Speed Grade** | | **-2 Speed Grade** | | **-3 Speed Grade** | | **Unit** |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{IOD}$ | | 1.7 | | 2.0 | | 2.6 | ns |
| $t_{IOC}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{IOCO}$ | | 1.4 | | 1.6 | | 2.1 | ns |
| $t_{IOCOMB}$ | | 0.5 | | 0.7 | | 0.9 | ns |
| $t_{IOSU}$ | 0.8 | | 1.0 | | 1.3 | | ns |
| $t_{IOH}$ | 0.7 | | 0.9 | | 1.2 | | ns |
| $t_{IOCLR}$ | | 0.5 | | 0.7 | | 0.9 | ns |
| $t_{OD1}$ | | 3.0 | | 4.2 | | 5.6 | ns |
| $t_{OD2}$ | | 3.0 | | 4.2 | | 5.6 | ns |
| $t_{OD3}$ | | 4.0 | | 5.5 | | 7.3 | ns |
| $t_{XZ}$ | | 3.5 | | 4.6 | | 6.1 | ns |
| $t_{ZX1}$ | | 3.5 | | 4.6 | | 6.1 | ns |
| $t_{ZX2}$ | | 3.5 | | 4.6 | | 6.1 | ns |
| $t_{ZX3}$ | | 4.5 | | 5.9 | | 7.8 | ns |
| $t_{INREG}$ | | 2.0 | | 2.6 | | 3.5 | ns |
| $t_{IOFD}$ | | 0.5 | | 0.8 | | 1.2 | ns |
| $t_{INCOMB}$ | | 0.5 | | 0.8 | | 1.2 | ns |

Tables 52 through 58 show EPF10K130E device internal and external timing parameters.

**Table 52. EPF10K130E Device LE Timing Microparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 0.6 | | 0.9 | | 1.3 | ns |
| $t_{CLUT}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{RLUT}$ | | 0.7 | | 0.9 | | 0.2 | ns |
| $t_{PACKED}$ | | 0.3 | | 0.5 | | 0.6 | ns |
| $t_{EN}$ | | 0.2 | | 0.3 | | 0.4 | ns |
| $t_{CICO}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.6 | | 0.8 | ns |
| $t_{CGENR}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CASC}$ | | 0.6 | | 0.9 | | 1.2 | ns |
| $t_{C}$ | | 0.3 | | 0.5 | | 0.6 | ns |
| $t_{CO}$ | | 0.5 | | 0.7 | | 0.8 | ns |
| $t_{COMB}$ | | 0.3 | | 0.5 | | 0.6 | ns |
| $t_{SU}$ | 0.5 | | 0.7 | | 0.8 | | ns |
| $t_{H}$ | 0.6 | | 0.7 | | 1.0 | | ns |
| $t_{PRE}$ | | 0.9 | | 1.2 | | 1.6 | ns |
| $t_{CLR}$ | | 0.9 | | 1.2 | | 1.6 | ns |
| $t_{CH}$ | 1.5 | | 1.5 | | 2.5 | | ns |
| $t_{CL}$ | 1.5 | | 1.5 | | 2.5 | | ns |

**Table 53. EPF10K130E Device IOE Timing Microparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 1.3 | | 1.5 | | 2.0 | ns |
| $t_{IOC}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{IOCO}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{IOCOMB}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{IOSU}$ | 1.0 | | 1.2 | | 1.6 | | ns |
| $t_{IOH}$ | 0.9 | | 0.9 | | 1.4 | | ns |
| $t_{IOCLR}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{OD1}$ | | 2.8 | | 4.1 | | 5.5 | ns |
| $t_{OD2}$ | | 2.8 | | 4.1 | | 5.5 | ns |

**Table 71. EPF10K50S External Timing Parameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 8.0 | | 9.5 | | 12.5 | ns |
| $t_{INSU}$ *(2)* | 2.4 | | 2.9 | | 3.9 | | ns |
| $t_{INH}$ *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(2)* | 2.0 | 4.3 | 2.0 | 5.2 | 2.0 | 7.3 | ns |
| $t_{INSU}$ *(3)* | 2.4 | | 2.9 | | | | ns |
| $t_{INH}$ *(3)* | 0.0 | | 0.0 | | | | ns |
| $t_{OUTCO}$ *(3)* | 0.5 | 3.3 | 0.5 | 4.1 | | | ns |
| $t_{PCISU}$ | 2.4 | | 2.9 | | – | | ns |
| $t_{PCIH}$ | 0.0 | | 0.0 | | – | | ns |
| $t_{PCICO}$ | 2.0 | 6.0 | 2.0 | 7.7 | – | – | ns |

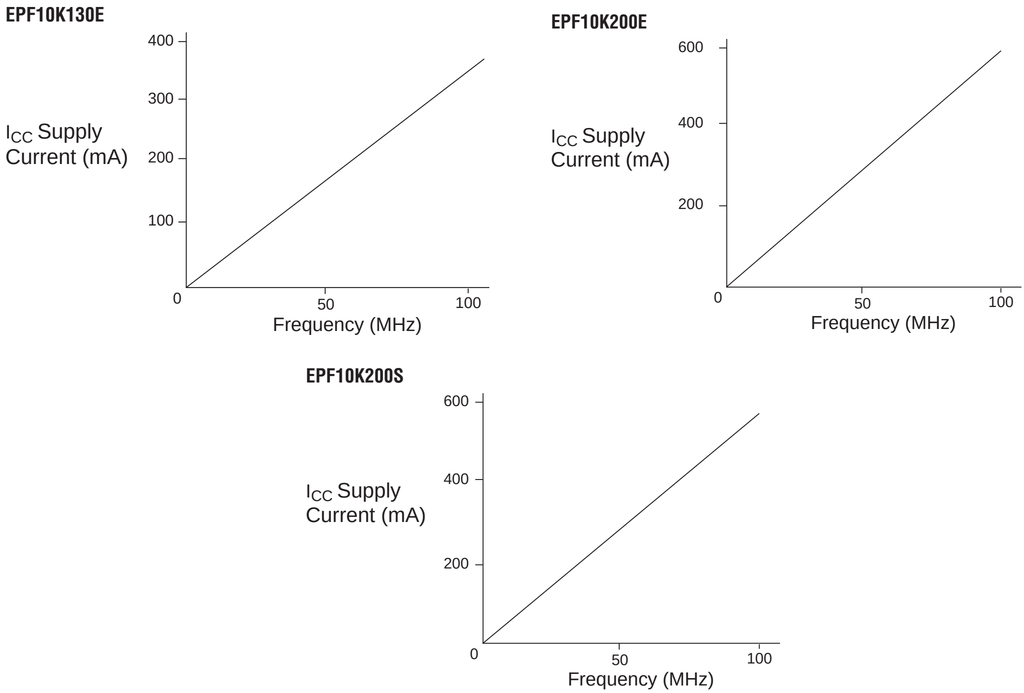
**Table 72. EPF10K50S External Bidirectional Timing Parameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ *(2)* | 2.7 | | 3.2 | | 4.3 | | ns |
| $t_{INHBIDIR}$ *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INHBIDIR}$ *(3)* | 0.0 | | 0.0 | | – | | ns |
| $t_{INSUBIDIR}$ *(3)* | 3.7 | | 4.2 | | – | | ns |
| $t_{OUTCOBIDIR}$ *(2)* | 2.0 | 4.5 | 2.0 | 5.2 | 2.0 | 7.3 | ns |
| $t_{XZBIDIR}$ *(2)* | | 6.8 | | 7.8 | | 10.1 | ns |
| $t_{ZXBIDIR}$ *(2)* | | 6.8 | | 7.8 | | 10.1 | ns |
| $t_{OUTCOBIDIR}$ *(3)* | 0.5 | 3.5 | 0.5 | 4.2 | – | – | |
| $t_{XZBIDIR}$ *(3)* | | 6.8 | | 8.4 | | – | ns |
| $t_{ZXBIDIR}$ *(3)* | | 6.8 | | 8.4 | | – | ns |

***Notes to tables:***

(1) All timing parameters are described in Tables 24 through 30.
(2) This parameter is measured without use of the ClockLock or ClockBoost circuits.
(3) This parameter is measured with use of the ClockLock or ClockBoost circuits

*Figure 31. FLEX 10KE $I_{CCACTIVE}$ vs. Operating Frequency (Part 2 of 2)*




# Configuration & Operation

The FLEX 10KE architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

## Operating Modes

The FLEX 10KE architecture uses SRAM configuration elements that require configuration data to be loaded every time the circuit powers up. The process of physically loading the SRAM data into the device is called *configuration*. Before configuration, as $V_{CC}$ rises, the device initiates a Power-On Reset (POR). This POR event clears the device and prepares it for configuration. The FLEX 10KE POR time does not exceed 50 µs.

When configuring with a configuration device, refer to the respective configuration device data sheet for POR timing information.

Additionally, the Altera software offers several features that help plan for future device migration by preventing the use of conflicting I/O pins.

*Table 81. I/O Counts for FLEX 10KA & FLEX 10KE Devices*

| FLEX 10KA | | FLEX 10KE | |
|---|---|---|---|
| **Device** | **I/O Count** | **Device** | **I/O Count** |
| EPF10K30AF256 | 191 | EPF10K30EF256 | 176 |
| EPF10K30AF484 | 246 | EPF10K30EF484 | 220 |
| EPF10K50VB356 | 274 | EPF10K50SB356 | 220 |
| EPF10K50VF484 | 291 | EPF10K50EF484 | 254 |
| EPF10K50VF484 | 291 | EPF10K50SF484 | 254 |
| EPF10K100AF484 | 369 | EPF10K100EF484 | 338 |

## Configuration Schemes

The configuration data for a FLEX 10KE device can be loaded with one of five configuration schemes (see Table 82), chosen on the basis of the target application. An EPC1, EPC2, or EPC16 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of a FLEX 10KE device, allowing automatic configuration on system power-up.

Multiple FLEX 10KE devices can be configured in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device. Additional FLEX 10K, FLEX 10KA, FLEX 10KE, and FLEX 6000 devices can be configured in the same serial chain.

*Table 82. Data Sources for FLEX 10KE Configuration*

| Configuration Scheme | Data Source |
|---|---|
| Configuration device | EPC1, EPC2, or EPC16 configuration device |
| Passive serial (PS) | BitBlaster, ByteBlasterMV, or MasterBlaster download cables, or serial data source |
| Passive parallel asynchronous (PPA) | Parallel data source |
| Passive parallel synchronous (PPS) | Parallel data source |
| JTAG | BitBlaster or ByteBlasterMV download cables, or microprocessor with a Jam STAPL file or JBC file |

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