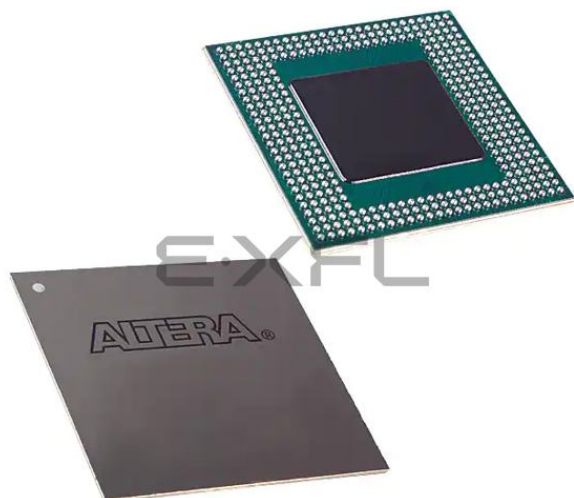




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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                         |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Obsolete                                                                                                                                |
| Number of LABs/CLBs            | 360                                                                                                                                     |
| Number of Logic Elements/Cells | 2880                                                                                                                                    |
| Total RAM Bits                 | 40960                                                                                                                                   |
| Number of I/O                  | 220                                                                                                                                     |
| Number of Gates                | 199000                                                                                                                                  |
| Voltage - Supply               | 2.375V ~ 2.625V                                                                                                                         |
| Mounting Type                  | Surface Mount                                                                                                                           |
| Operating Temperature          | 0°C ~ 70°C (TA)                                                                                                                         |
| Package / Case                 | 356-LBGA                                                                                                                                |
| Supplier Device Package        | 356-BGA (35x35)                                                                                                                         |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/intel/epf10k50sbc356-2x">https://www.e-xfl.com/product-detail/intel/epf10k50sbc356-2x</a> |

- Software design support and automatic place-and-route provided by Altera's development systems for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800
- Flexible package options
  - Available in a variety of packages with 144 to 672 pins, including the innovative FineLine BGA™ packages (see [Tables 3 and 4](#))
  - SameFrame™ pin-out compatibility between FLEX 10KA and FLEX 10KE devices across a range of device densities and pin counts
- Additional design entry and simulation support provided by EDIF 2.0.0 and 3.0.0 netlist files, library of parameterized modules (LPM), DesignWare components, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, VeriBest, and Viewlogic

**Table 3. FLEX 10KE Package Options & I/O Pin Count** *Notes (1), (2)*

| Device     | 144-Pin<br>TQFP | 208-Pin<br>PQFP | 240-Pin<br>PQFP<br>RQFP | 256-Pin<br>FineLine<br>BGA | 356-Pin<br>BGA | 484-Pin<br>FineLine<br>BGA | 599-Pin<br>PGA | 600-Pin<br>BGA | 672-Pin<br>FineLine<br>BGA |
|------------|-----------------|-----------------|-------------------------|----------------------------|----------------|----------------------------|----------------|----------------|----------------------------|
| EPF10K30E  | 102             | 147             |                         | 176                        |                | 220                        |                |                | 220 (3)                    |
| EPF10K50E  | 102             | 147             | 189                     | 191                        |                | 254                        |                |                | 254 (3)                    |
| EPF10K50S  | 102             | 147             | 189                     | 191                        | 220            | 254                        |                |                | 254 (3)                    |
| EPF10K100E |                 | 147             | 189                     | 191                        | 274            | 338                        |                |                | 338 (3)                    |
| EPF10K130E |                 |                 | 186                     |                            | 274            | 369                        |                | 424            | 413                        |
| EPF10K200E |                 |                 |                         |                            |                |                            | 470            | 470            | 470                        |
| EPF10K200S |                 |                 | 182                     |                            | 274            | 369                        | 470            | 470            | 470                        |

**Notes:**

- (1) FLEX 10KE device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), pin-grid array (PGA), and ball-grid array (BGA) packages.
- (2) Devices in the same package are pin-compatible, although some devices have more I/O pins than others. When planning device migration, use the I/O pins that are common to all devices.
- (3) This option is supported with a 484-pin FineLine BGA package. By using SameFrame pin migration, all FineLine BGA packages are pin-compatible. For example, a board can be designed to support 256-pin, 484-pin, and 672-pin FineLine BGA packages. The Altera software automatically avoids conflicting pins when future migration is set.

**Table 4. FLEX 10KE Package Sizes**

| Device                      | 144-Pin<br>TQFP | 208-Pin<br>PQFP | 240-Pin<br>PQFP<br>RQFP | 256-Pin<br>FineLine<br>BGA | 356-Pin<br>BGA | 484-Pin<br>FineLine<br>BGA | 599-Pin<br>PGA | 600-Pin<br>BGA | 672-Pin<br>FineLine<br>BGA |
|-----------------------------|-----------------|-----------------|-------------------------|----------------------------|----------------|----------------------------|----------------|----------------|----------------------------|
| Pitch (mm)                  | 0.50            | 0.50            | 0.50                    | 1.0                        | 1.27           | 1.0                        | —              | 1.27           | 1.0                        |
| Area (mm <sup>2</sup> )     | 484             | 936             | 1,197                   | 289                        | 1,225          | 529                        | 3,904          | 2,025          | 729                        |
| Length × width<br>(mm × mm) | 22 × 22         | 30.6 × 30.6     | 34.6 × 34.6             | 17 × 17                    | 35 × 35        | 23 × 23                    | 62.5 × 62.5    | 45 × 45        | 27 × 27                    |

## General Description

Altera FLEX 10KE devices are enhanced versions of FLEX 10K devices. Based on reconfigurable CMOS SRAM elements, the FLEX architecture incorporates all features necessary to implement common gate array megafunctions. With up to 200,000 typical gates, FLEX 10KE devices provide the density, speed, and features to integrate entire systems, including multiple 32-bit buses, into a single device.

The ability to reconfigure FLEX 10KE devices enables 100% testing prior to shipment and allows the designer to focus on simulation and design verification. FLEX 10KE reconfigurability eliminates inventory management for gate array designs and generation of test vectors for fault coverage.

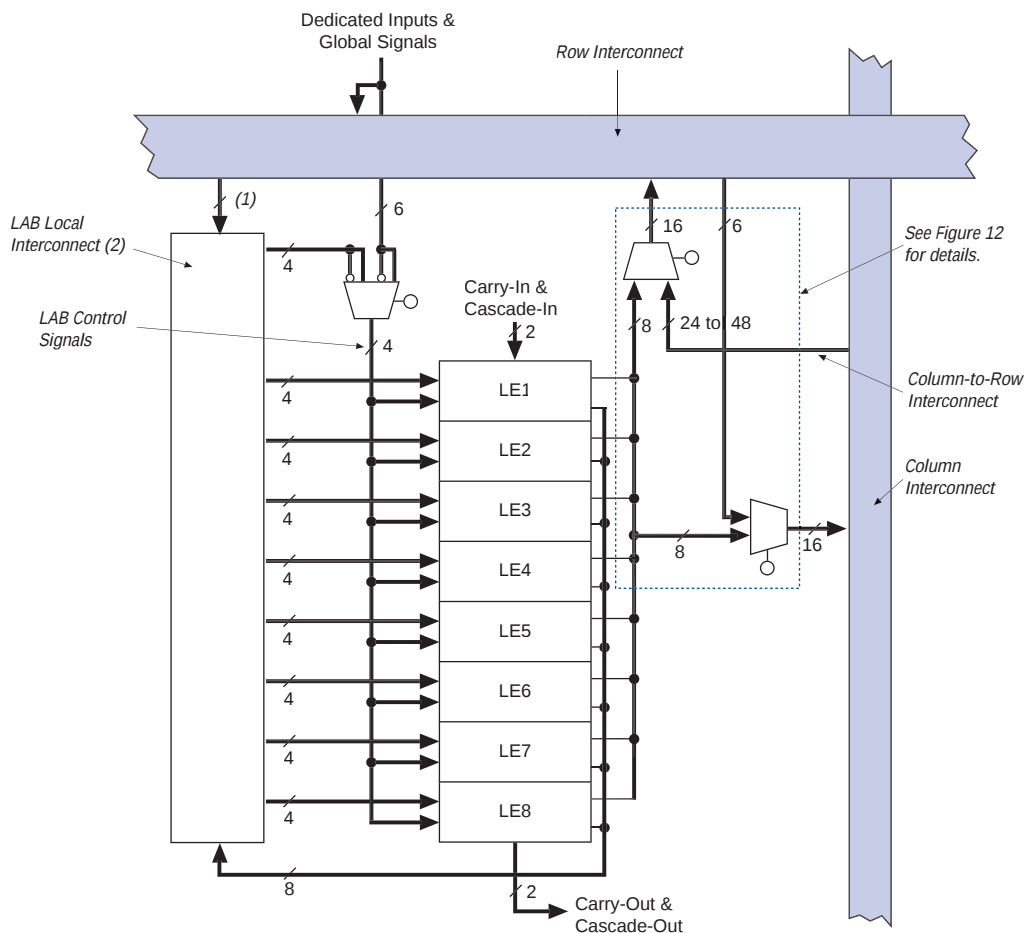
Table 5 shows FLEX 10KE performance for some common designs. All performance values were obtained with Synopsys DesignWare or LPM functions. Special design techniques are not required to implement the applications; the designer simply infers or instantiates a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

EABs provide flexible options for driving and controlling clock signals. Different clocks and clock enables can be used for reading and writing to the EAB. Registers can be independently inserted on the data input, EAB output, write address, write enable signals, read address, and read enable signals. The global signals and the EAB local interconnect can drive write enable, read enable, and clock enable signals. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control write enable, read enable, clear, clock, and clock enable signals.

An EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs (see [Figures 2 and 4](#)). The column interconnect, which is adjacent to the EAB, has twice as many channels as other columns in the device.

### Logic Array Block

An LAB consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure to the FLEX 10KE architecture, facilitating efficient routing with optimum device utilization and high performance (see [Figure 7](#)).

**Figure 7. FLEX 10KE LAB**

**Notes:**

- (1) EPF10K30E, EPF10K50E, and EPF10K50S devices have 22 inputs to the LAB local interconnect channel from the row; EPF10K100E, EPF10K130E, EPF10K200E, and EPF10K200S devices have 26.
- (2) EPF10K30E, EPF10K50E, and EPF10K50S devices have 30 LAB local interconnect channels; EPF10K100E, EPF10K130E, EPF10K200E, and EPF10K200S devices have 34.

The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the flipflop is bypassed and the output of the LUT drives the output of the LE.

The LE has two outputs that drive the interconnect: one drives the local interconnect and the other drives either the row or column FastTrack Interconnect routing structure. The two outputs can be controlled independently. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, can improve LE utilization because the register and the LUT can be used for unrelated functions.

The FLEX 10KE architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. The carry chain supports high-speed counters and adders and the cascade chain implements wide-input functions with minimum delay. Carry and cascade chains connect all LEs in a LAB as well as all LABs in the same row. Intensive use of carry and cascade chains can reduce routing flexibility. Therefore, the use of these chains should be limited to speed-critical portions of a design.

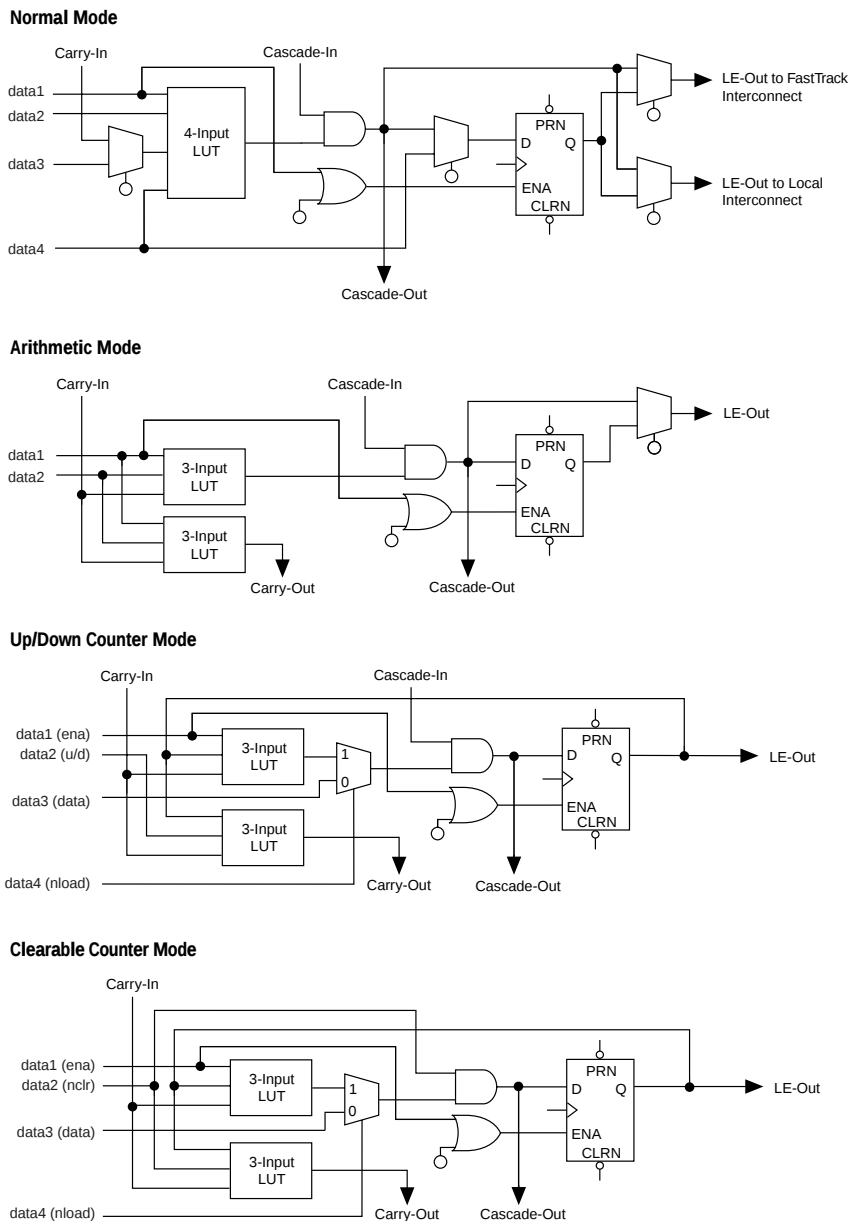
### *Carry Chain*

The carry chain provides a very fast (as low as 0.2 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 10KE architecture to implement high-speed counters, adders, and comparators of arbitrary width efficiently. Carry chain logic can be created automatically by the Altera Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as LPM and DesignWare functions automatically take advantage of carry chains.

Carry chains longer than eight LEs are automatically implemented by linking LABs together. For enhanced fitting, a long carry chain skips alternate LABs in a row. A carry chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB. For example, the last LE of the first LAB in a row carries to the first LE of the third LAB in the row. The carry chain does not cross the EAB at the middle of the row. For instance, in the EPF10K50E device, the carry chain stops at the eighteenth LAB and a new one begins at the nineteenth LAB.

Figure 11 shows the LE operating modes.

**Figure 11. FLEX 10KE LE Operating Modes**



### **Clearable Counter Mode**

The clearable counter mode is similar to the up / down counter mode, but supports a synchronous clear instead of the up / down control. The clear function is substituted for the cascade-in signal in the up / down counter mode. Use 2 three-input LUTs: one generates the counter data, and the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer. The output of this multiplexer is ANDed with a synchronous clear signal.

### *Internal Tri-State Emulation*

Internal tri-state emulation provides internal tri-states without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable (OE) signals select which signal drives the bus. However, if multiple OE signals are active, contending signals can be driven onto the bus. Conversely, if no OE signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The Altera software automatically implements tri-state bus functionality with a multiplexer.

### *Clear & Preset Logic Control*

Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. The clear and preset control structure of the LE asynchronously loads signals into a register. Either LABCTRL1 or LABCTRL2 can control the asynchronous clear. Alternatively, the register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

During compilation, the Altera Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six modes chosen during design entry:

- Asynchronous clear
- Asynchronous preset
- Asynchronous clear and preset
- Asynchronous load with clear
- Asynchronous load with preset
- Asynchronous load without clear or preset

**Asynchronous Clear**

The flipflop can be cleared by either LABCTRL1 or LABCTRL2. In this mode, the preset signal is tied to VCC to deactivate it.

**Asynchronous Preset**

An asynchronous preset is implemented as an asynchronous load, or with an asynchronous clear. If DATA3 is tied to VCC, asserting LABCTRL1 asynchronously loads a one into the register. Alternatively, the Altera software can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used for one of the LE operating modes.

**Asynchronous Preset & Clear**

When implementing asynchronous clear and preset, LABCTRL1 controls the preset and LABCTRL2 controls the clear. DATA3 is tied to VCC, so that asserting LABCTRL1 asynchronously loads a one into the register, effectively presetting the register. Asserting LABCTRL2 clears the register.

**Asynchronous Load with Clear**

When implementing an asynchronous load in conjunction with the clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear. LABCTRL2 implements the clear by controlling the register clear; LABCTRL2 does not have to feed the preset circuits.

**Asynchronous Load with Preset**

When implementing an asynchronous load in conjunction with preset, the Altera software provides preset control by using the clear and inverting the input and output of the register. Asserting LABCTRL2 presets the register, while asserting LABCTRL1 loads the register. The Altera software inverts the signal that drives DATA3 to account for the inversion of the register's output.

**Asynchronous Load without Preset or Clear**

When implementing an asynchronous load without preset or clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear.

The VCCINT pins must always be connected to a 2.5-V power supply. With a 2.5-V  $V_{CCINT}$  level, input voltages are compatible with 2.5-V, 3.3-V, and 5.0-V inputs. The VCCIO pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with  $V_{CCIO}$  levels higher than 3.0 V achieve a faster timing delay of  $t_{OD2}$  instead of  $t_{OD1}$ .

Table 14 summarizes FLEX 10KE MultiVolt I/O support.

| <b>Table 14. FLEX 10KE MultiVolt I/O Support</b> |                  |      |      |                   |     |     |
|--------------------------------------------------|------------------|------|------|-------------------|-----|-----|
| $V_{CCIO}$ (V)                                   | Input Signal (V) |      |      | Output Signal (V) |     |     |
|                                                  | 2.5              | 3.3  | 5.0  | 2.5               | 3.3 | 5.0 |
| 2.5                                              | ✓                | ✓(1) | ✓(1) | ✓                 |     |     |
| 3.3                                              | ✓                | ✓    | ✓(1) | ✓(2)              | ✓   | ✓   |

**Notes:**

- (1) The PCI clamping diode must be disabled to drive an input with voltages higher than  $V_{CCIO}$ .
- (2) When  $V_{CCIO} = 3.3$  V, a FLEX 10KE device can drive a 2.5-V device that has 3.3-V tolerant inputs.

Open-drain output pins on FLEX 10KE devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a  $V_{IH}$  of 3.5 V. When the open-drain pin is active, it will drive low. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The  $I_{OL}$  current specification should be considered when selecting a pull-up resistor.

## Power Sequencing & Hot-Socketing

Because FLEX 10KE devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The  $V_{CCIO}$  and  $V_{CCINT}$  power planes can be powered in any order.

Signals can be driven into FLEX 10KE devices before and during power up without damaging the device. Additionally, FLEX 10KE devices do not drive out during power up. Once operating conditions are reached, FLEX 10KE devices operate as specified by the user.

**Table 20. 2.5-V EPF10K50E & EPF10K200E Device Recommended Operating Conditions**

| Symbol             | Parameter                                           | Conditions         | Min         | Max               | Unit |
|--------------------|-----------------------------------------------------|--------------------|-------------|-------------------|------|
| V <sub>CCINT</sub> | Supply voltage for internal logic and input buffers | (3), (4)           | 2.30 (2.30) | 2.70 (2.70)       | V    |
| V <sub>CCIO</sub>  | Supply voltage for output buffers, 3.3-V operation  | (3), (4)           | 3.00 (3.00) | 3.60 (3.60)       | V    |
|                    | Supply voltage for output buffers, 2.5-V operation  | (3), (4)           | 2.30 (2.30) | 2.70 (2.70)       | V    |
| V <sub>I</sub>     | Input voltage                                       | (5)                | −0.5        | 5.75              | V    |
| V <sub>O</sub>     | Output voltage                                      |                    | 0           | V <sub>CCIO</sub> | V    |
| T <sub>A</sub>     | Ambient temperature                                 | For commercial use | 0           | 70                | ° C  |
|                    |                                                     | For industrial use | −40         | 85                | ° C  |
| T <sub>J</sub>     | Operating temperature                               | For commercial use | 0           | 85                | ° C  |
|                    |                                                     | For industrial use | −40         | 100               | ° C  |
| t <sub>R</sub>     | Input rise time                                     |                    |             | 40                | ns   |
| t <sub>F</sub>     | Input fall time                                     |                    |             | 40                | ns   |

**Table 21. 2.5-V EPF10K30E, EPF10K50S, EPF10K100E, EPF10K130E & EPF10K200S Device Recommended Operating Conditions**

| Symbol             | Parameter                                           | Conditions         | Min              | Max               | Unit |
|--------------------|-----------------------------------------------------|--------------------|------------------|-------------------|------|
| V <sub>CCINT</sub> | Supply voltage for internal logic and input buffers | (3), (4)           | 2.375<br>(2.375) | 2.625<br>(2.625)  | V    |
| V <sub>CCIO</sub>  | Supply voltage for output buffers, 3.3-V operation  | (3), (4)           | 3.00 (3.00)      | 3.60 (3.60)       | V    |
|                    | Supply voltage for output buffers, 2.5-V operation  | (3), (4)           | 2.375<br>(2.375) | 2.625<br>(2.625)  | V    |
| V <sub>I</sub>     | Input voltage                                       | (5)                | −0.5             | 5.75              | V    |
| V <sub>O</sub>     | Output voltage                                      |                    | 0                | V <sub>CCIO</sub> | V    |
| T <sub>A</sub>     | Ambient temperature                                 | For commercial use | 0                | 70                | ° C  |
|                    |                                                     | For industrial use | −40              | 85                | ° C  |
| T <sub>J</sub>     | Operating temperature                               | For commercial use | 0                | 85                | ° C  |
|                    |                                                     | For industrial use | −40              | 100               | ° C  |
| t <sub>R</sub>     | Input rise time                                     |                    |                  | 40                | ns   |
| t <sub>F</sub>     | Input fall time                                     |                    |                  | 40                | ns   |

**Table 22. FLEX 10KE 2.5-V Device DC Operating Conditions***Notes (6), (7)*

| Symbol     | Parameter                                                         | Conditions                                                  | Min                            | Typ | Max                               | Unit      |
|------------|-------------------------------------------------------------------|-------------------------------------------------------------|--------------------------------|-----|-----------------------------------|-----------|
| $V_{IH}$   | High-level input voltage                                          |                                                             | 1.7, $0.5 \times V_{CCIO}$ (8) |     | 5.75                              | V         |
| $V_{IL}$   | Low-level input voltage                                           |                                                             | -0.5                           |     | 0.8,<br>$0.3 \times V_{CCIO}$ (8) | V         |
| $V_{OH}$   | 3.3-V high-level TTL output voltage                               | $I_{OH} = -8$ mA DC,<br>$V_{CCIO} = 3.00$ V (9)             | 2.4                            |     |                                   | V         |
|            | 3.3-V high-level CMOS output voltage                              | $I_{OH} = -0.1$ mA DC,<br>$V_{CCIO} = 3.00$ V (9)           | $V_{CCIO} - 0.2$               |     |                                   | V         |
|            | 3.3-V high-level PCI output voltage                               | $I_{OH} = -0.5$ mA DC,<br>$V_{CCIO} = 3.00$ to $3.60$ V (9) | $0.9 \times V_{CCIO}$          |     |                                   | V         |
|            | 2.5-V high-level output voltage                                   | $I_{OH} = -0.1$ mA DC,<br>$V_{CCIO} = 2.30$ V (9)           | 2.1                            |     |                                   | V         |
|            |                                                                   | $I_{OH} = -1$ mA DC,<br>$V_{CCIO} = 2.30$ V (9)             | 2.0                            |     |                                   | V         |
|            |                                                                   | $I_{OH} = -2$ mA DC,<br>$V_{CCIO} = 2.30$ V (9)             | 1.7                            |     |                                   | V         |
|            |                                                                   |                                                             |                                |     |                                   |           |
| $V_{OL}$   | 3.3-V low-level TTL output voltage                                | $I_{OL} = 12$ mA DC,<br>$V_{CCIO} = 3.00$ V (10)            |                                |     | 0.45                              | V         |
|            | 3.3-V low-level CMOS output voltage                               | $I_{OL} = 0.1$ mA DC,<br>$V_{CCIO} = 3.00$ V (10)           |                                |     | 0.2                               | V         |
|            | 3.3-V low-level PCI output voltage                                | $I_{OL} = 1.5$ mA DC,<br>$V_{CCIO} = 3.00$ to $3.60$ V (10) |                                |     | $0.1 \times V_{CCIO}$             | V         |
|            | 2.5-V low-level output voltage                                    | $I_{OL} = 0.1$ mA DC,<br>$V_{CCIO} = 2.30$ V (10)           |                                |     | 0.2                               | V         |
|            |                                                                   | $I_{OL} = 1$ mA DC,<br>$V_{CCIO} = 2.30$ V (10)             |                                |     | 0.4                               | V         |
|            |                                                                   | $I_{OL} = 2$ mA DC,<br>$V_{CCIO} = 2.30$ V (10)             |                                |     | 0.7                               | V         |
|            |                                                                   |                                                             |                                |     |                                   |           |
| $I_I$      | Input pin leakage current                                         | $V_I = V_{CCIOmax}$ to $0$ V (11)                           | -10                            |     | 10                                | $\mu$ A   |
| $I_{OZ}$   | Tri-stated I/O pin leakage current                                | $V_O = V_{CCIOmax}$ to $0$ V (11)                           | -10                            |     | 10                                | $\mu$ A   |
| $I_{CC0}$  | $V_{CC}$ supply current (standby)                                 | $V_I =$ ground, no load, no toggling inputs                 |                                | 5   |                                   | mA        |
|            |                                                                   | $V_I =$ ground, no load, no toggling inputs (12)            |                                | 10  |                                   | mA        |
| $R_{CONF}$ | Value of I/O pin pull-up resistor before and during configuration | $V_{CCIO} = 3.0$ V (13)                                     | 20                             |     | 50                                | $k\Omega$ |
|            |                                                                   | $V_{CCIO} = 2.3$ V (13)                                     | 30                             |     | 80                                | $k\Omega$ |

**Table 28. Interconnect Timing Microparameters** *Note (1)*

| Symbol           | Parameter                                                                                                            | Conditions |
|------------------|----------------------------------------------------------------------------------------------------------------------|------------|
| $t_{DIN2IOE}$    | Delay from dedicated input pin to IOE control input                                                                  | (7)        |
| $t_{DIN2LE}$     | Delay from dedicated input pin to LE or EAB control input                                                            | (7)        |
| $t_{DCLK2IOE}$   | Delay from dedicated clock pin to IOE clock                                                                          | (7)        |
| $t_{DCLK2LE}$    | Delay from dedicated clock pin to LE or EAB clock                                                                    | (7)        |
| $t_{DIN2DATA}$   | Delay from dedicated input or clock to LE or EAB data                                                                | (7)        |
| $t_{SAMELAB}$    | Routing delay for an LE driving another LE in the same LAB                                                           |            |
| $t_{SAMEROW}$    | Routing delay for a row IOE, LE, or EAB driving a row IOE, LE, or EAB in the same row                                | (7)        |
| $t_{SAMECOLUMN}$ | Routing delay for an LE driving an IOE in the same column                                                            | (7)        |
| $t_{DIFFROW}$    | Routing delay for a column IOE, LE, or EAB driving an LE or EAB in a different row                                   | (7)        |
| $t_{TROWROWS}$   | Routing delay for a row IOE or EAB driving an LE or EAB in a different row                                           | (7)        |
| $t_{LEPERIPH}$   | Routing delay for an LE driving a control signal of an IOE via the peripheral control bus                            | (7)        |
| $t_{LABCARRY}$   | Routing delay for the carry-out signal of an LE driving the carry-in signal of a different LE in a different LAB     |            |
| $t_{LABCASC}$    | Routing delay for the cascade-out signal of an LE driving the cascade-in signal of a different LE in a different LAB |            |

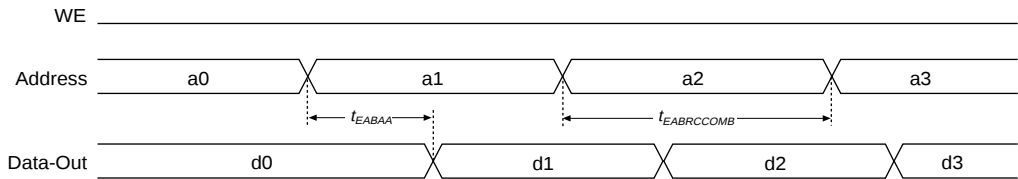
**Table 29. External Timing Parameters**

| Symbol      | Parameter                                                                                      | Conditions |
|-------------|------------------------------------------------------------------------------------------------|------------|
| $t_{DRR}$   | Register-to-register delay via four LEs, three row interconnects, and four local interconnects | (8)        |
| $t_{INSU}$  | Setup time with global clock at IOE register                                                   | (9)        |
| $t_{INH}$   | Hold time with global clock at IOE register                                                    | (9)        |
| $t_{OUTCO}$ | Clock-to-output delay with global clock at IOE register                                        | (9)        |
| $t_{PCISU}$ | Setup time with global clock for registers used in PCI designs                                 | (9),(10)   |
| $t_{PCIH}$  | Hold time with global clock for registers used in PCI designs                                  | (9),(10)   |
| $t_{PCICO}$ | Clock-to-output delay with global clock for registers used in PCI designs                      | (9),(10)   |

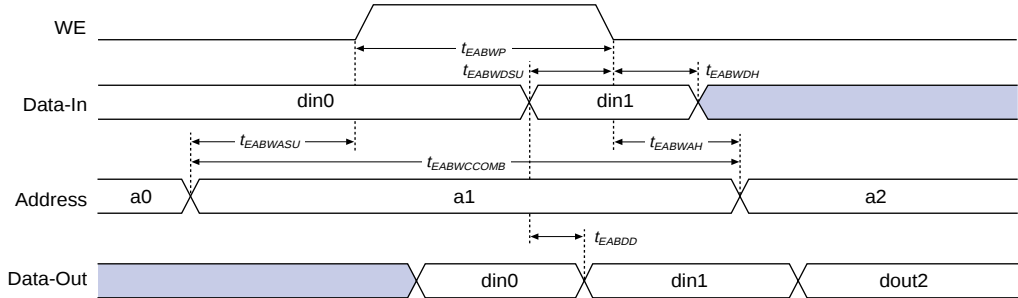
Figures 29 and 30 show the asynchronous and synchronous timing waveforms, respectively, or the EAB macroparameters in Tables 26 and 27.

Figure 29. EAB Asynchronous Timing Waveforms

EAB Asynchronous Read



EAB Asynchronous Write



**Table 43. EPF10K50E External Timing Parameters** Notes (1), (2)

| Symbol             | -1 Speed Grade |     | -2 Speed Grade |      | -3 Speed Grade |      | Unit |
|--------------------|----------------|-----|----------------|------|----------------|------|------|
|                    | Min            | Max | Min            | Max  | Min            | Max  |      |
| $t_{\text{DDR}}$   |                | 8.5 |                | 10.0 |                | 13.5 | ns   |
| $t_{\text{INSU}}$  | 2.7            |     | 3.2            |      | 4.3            |      | ns   |
| $t_{\text{INH}}$   | 0.0            |     | 0.0            |      | 0.0            |      | ns   |
| $t_{\text{OUTCO}}$ | 2.0            | 4.5 | 2.0            | 5.2  | 2.0            | 7.3  | ns   |
| $t_{\text{PCISU}}$ | 3.0            |     | 4.2            |      | -              |      | ns   |
| $t_{\text{PCIH}}$  | 0.0            |     | 0.0            |      | -              |      | ns   |
| $t_{\text{PCICO}}$ | 2.0            | 6.0 | 2.0            | 7.7  | -              | -    | ns   |

**Table 44. EPF10K50E External Bidirectional Timing Parameters** Notes (1), (2)

| Symbol                  | -1 Speed Grade |     | -2 Speed Grade |     | -3 Speed Grade |      | Unit |
|-------------------------|----------------|-----|----------------|-----|----------------|------|------|
|                         | Min            | Max | Min            | Max | Min            | Max  |      |
| $t_{\text{INSUBIDIR}}$  | 2.7            |     | 3.2            |     | 4.3            |      | ns   |
| $t_{\text{INHBIDIR}}$   | 0.0            |     | 0.0            |     | 0.0            |      | ns   |
| $t_{\text{OUTCOBIDIR}}$ | 2.0            | 4.5 | 2.0            | 5.2 | 2.0            | 7.3  | ns   |
| $t_{\text{XZBIDIR}}$    |                | 6.8 |                | 7.8 |                | 10.1 | ns   |
| $t_{\text{ZXBIDIR}}$    |                | 6.8 |                | 7.8 |                | 10.1 | ns   |

**Notes to tables:**

- (1) All timing parameters are described in Tables 24 through 30 in this data sheet.  
 (2) These parameters are specified by characterization.

Tables 45 through 51 show EPF10K100E device internal and external timing parameters.

**Table 45. EPF10K100E Device LE Timing Microparameters** Note (1)

| Symbol              | -1 Speed Grade |     | -2 Speed Grade |     | -3 Speed Grade |     | Unit |
|---------------------|----------------|-----|----------------|-----|----------------|-----|------|
|                     | Min            | Max | Min            | Max | Min            | Max |      |
| $t_{\text{LUT}}$    |                | 0.7 |                | 1.0 |                | 1.5 | ns   |
| $t_{\text{CLUT}}$   |                | 0.5 |                | 0.7 |                | 0.9 | ns   |
| $t_{\text{RLUT}}$   |                | 0.6 |                | 0.8 |                | 1.1 | ns   |
| $t_{\text{PACKED}}$ |                | 0.3 |                | 0.4 |                | 0.5 | ns   |
| $t_{\text{EN}}$     |                | 0.2 |                | 0.3 |                | 0.3 | ns   |
| $t_{\text{CICO}}$   |                | 0.1 |                | 0.1 |                | 0.2 | ns   |
| $t_{\text{CGEN}}$   |                | 0.4 |                | 0.5 |                | 0.7 | ns   |

**Table 45. EPF10K100E Device LE Timing Microparameters** *Note (1)*

| Symbol      | -1 Speed Grade |     | -2 Speed Grade |     | -3 Speed Grade |     | Unit |
|-------------|----------------|-----|----------------|-----|----------------|-----|------|
|             | Min            | Max | Min            | Max | Min            | Max |      |
| $t_{CGENR}$ |                | 0.1 |                | 0.1 |                | 0.2 | ns   |
| $t_{CASC}$  |                | 0.6 |                | 0.9 |                | 1.2 | ns   |
| $t_C$       |                | 0.8 |                | 1.0 |                | 1.4 | ns   |
| $t_{CO}$    |                | 0.6 |                | 0.8 |                | 1.1 | ns   |
| $t_{COMB}$  |                | 0.4 |                | 0.5 |                | 0.7 | ns   |
| $t_{SU}$    | 0.4            |     | 0.6            |     | 0.7            |     | ns   |
| $t_H$       | 0.5            |     | 0.7            |     | 0.9            |     | ns   |
| $t_{PRE}$   |                | 0.8 |                | 1.0 |                | 1.4 | ns   |
| $t_{CLR}$   |                | 0.8 |                | 1.0 |                | 1.4 | ns   |
| $t_{CH}$    | 1.5            |     | 2.0            |     | 2.5            |     | ns   |
| $t_{CL}$    | 1.5            |     | 2.0            |     | 2.5            |     | ns   |

**Table 46. EPF10K100E Device IOE Timing Microparameters** *Note (1)*

| Symbol       | -1 Speed Grade |     | -2 Speed Grade |     | -3 Speed Grade |     | Unit |
|--------------|----------------|-----|----------------|-----|----------------|-----|------|
|              | Min            | Max | Min            | Max | Min            | Max |      |
| $t_{IOD}$    |                | 1.7 |                | 2.0 |                | 2.6 | ns   |
| $t_{IOC}$    |                | 0.0 |                | 0.0 |                | 0.0 | ns   |
| $t_{IOCO}$   |                | 1.4 |                | 1.6 |                | 2.1 | ns   |
| $t_{IOCOMB}$ |                | 0.5 |                | 0.7 |                | 0.9 | ns   |
| $t_{IOSU}$   | 0.8            |     | 1.0            |     | 1.3            |     | ns   |
| $t_{IOH}$    | 0.7            |     | 0.9            |     | 1.2            |     | ns   |
| $t_{IOCLR}$  |                | 0.5 |                | 0.7 |                | 0.9 | ns   |
| $t_{OD1}$    |                | 3.0 |                | 4.2 |                | 5.6 | ns   |
| $t_{OD2}$    |                | 3.0 |                | 4.2 |                | 5.6 | ns   |
| $t_{OD3}$    |                | 4.0 |                | 5.5 |                | 7.3 | ns   |
| $t_{XZ}$     |                | 3.5 |                | 4.6 |                | 6.1 | ns   |
| $t_{ZX1}$    |                | 3.5 |                | 4.6 |                | 6.1 | ns   |
| $t_{ZX2}$    |                | 3.5 |                | 4.6 |                | 6.1 | ns   |
| $t_{ZX3}$    |                | 4.5 |                | 5.9 |                | 7.8 | ns   |
| $t_{INREG}$  |                | 2.0 |                | 2.6 |                | 3.5 | ns   |
| $t_{OFD}$    |                | 0.5 |                | 0.8 |                | 1.2 | ns   |
| $t_{INCOMB}$ |                | 0.5 |                | 0.8 |                | 1.2 | ns   |

**Table 47. EPF10K100E Device EAB Internal Microparameters** *Note (1)*

| Symbol         | -1 Speed Grade |     | -2 Speed Grade |     | -3 Speed Grade |     | Unit |
|----------------|----------------|-----|----------------|-----|----------------|-----|------|
|                | Min            | Max | Min            | Max | Min            | Max |      |
| $t_{EABDATA1}$ |                | 1.5 |                | 2.0 |                | 2.6 | ns   |
| $t_{EABDATA1}$ |                | 0.0 |                | 0.0 |                | 0.0 | ns   |
| $t_{EABWE1}$   |                | 1.5 |                | 2.0 |                | 2.6 | ns   |
| $t_{EABWE2}$   |                | 0.3 |                | 0.4 |                | 0.5 | ns   |
| $t_{EABRE1}$   |                | 0.3 |                | 0.4 |                | 0.5 | ns   |
| $t_{EABRE2}$   |                | 0.0 |                | 0.0 |                | 0.0 | ns   |
| $t_{EABCLK}$   |                | 0.0 |                | 0.0 |                | 0.0 | ns   |
| $t_{EABCO}$    |                | 0.3 |                | 0.4 |                | 0.5 | ns   |
| $t_{EABYPASS}$ |                | 0.1 |                | 0.1 |                | 0.2 | ns   |
| $t_{EABSU}$    | 0.8            |     | 1.0            |     | 1.4            |     | ns   |
| $t_{EABH}$     | 0.1            |     | 0.1            |     | 0.2            |     | ns   |
| $t_{EABCLR}$   | 0.3            |     | 0.4            |     | 0.5            |     | ns   |
| $t_{AA}$       |                | 4.0 |                | 5.1 |                | 6.6 | ns   |
| $t_{WP}$       | 2.7            |     | 3.5            |     | 4.7            |     | ns   |
| $t_{RP}$       | 1.0            |     | 1.3            |     | 1.7            |     | ns   |
| $t_{WDSU}$     | 1.0            |     | 1.3            |     | 1.7            |     | ns   |
| $t_{WDH}$      | 0.2            |     | 0.2            |     | 0.3            |     | ns   |
| $t_{WASU}$     | 1.6            |     | 2.1            |     | 2.8            |     | ns   |
| $t_{WAH}$      | 1.6            |     | 2.1            |     | 2.8            |     | ns   |
| $t_{RASU}$     | 3.0            |     | 3.9            |     | 5.2            |     | ns   |
| $t_{RAH}$      | 0.1            |     | 0.1            |     | 0.2            |     | ns   |
| $t_{WO}$       |                | 1.5 |                | 2.0 |                | 2.6 | ns   |
| $t_{DD}$       |                | 1.5 |                | 2.0 |                | 2.6 | ns   |
| $t_{EABOUT}$   |                | 0.2 |                | 0.3 |                | 0.3 | ns   |
| $t_{EABCH}$    | 1.5            |     | 2.0            |     | 2.5            |     | ns   |
| $t_{EABCL}$    | 2.7            |     | 3.5            |     | 4.7            |     | ns   |

**Table 48. EPF10K100E Device EAB Internal Timing Macroparameters** (Part 1 of 2) *Note (1)*

| Symbol         | -1 Speed Grade |     | -2 Speed Grade |     | -3 Speed Grade |     | Unit |
|----------------|----------------|-----|----------------|-----|----------------|-----|------|
|                | Min            | Max | Min            | Max | Min            | Max |      |
| $t_{EABAA}$    |                | 5.9 |                | 7.6 |                | 9.9 | ns   |
| $t_{EABRCOMB}$ | 5.9            |     | 7.6            |     | 9.9            |     | ns   |
| $t_{EABRCREG}$ | 5.1            |     | 6.5            |     | 8.5            |     | ns   |
| $t_{EABWP}$    | 2.7            |     | 3.5            |     | 4.7            |     | ns   |

Tables 52 through 58 show EPF10K130E device internal and external timing parameters.

**Table 52. EPF10K130E Device LE Timing Microparameters** *Note (1)*

| Symbol       | -1 Speed Grade |     | -2 Speed Grade |     | -3 Speed Grade |     | Unit |
|--------------|----------------|-----|----------------|-----|----------------|-----|------|
|              | Min            | Max | Min            | Max | Min            | Max |      |
| $t_{LUT}$    |                | 0.6 |                | 0.9 |                | 1.3 | ns   |
| $t_{CLUT}$   |                | 0.6 |                | 0.8 |                | 1.0 | ns   |
| $t_{RLUT}$   |                | 0.7 |                | 0.9 |                | 0.2 | ns   |
| $t_{PACKED}$ |                | 0.3 |                | 0.5 |                | 0.6 | ns   |
| $t_{EN}$     |                | 0.2 |                | 0.3 |                | 0.4 | ns   |
| $t_{CICO}$   |                | 0.1 |                | 0.1 |                | 0.2 | ns   |
| $t_{CGEN}$   |                | 0.4 |                | 0.6 |                | 0.8 | ns   |
| $t_{CGENR}$  |                | 0.1 |                | 0.1 |                | 0.2 | ns   |
| $t_{CASC}$   |                | 0.6 |                | 0.9 |                | 1.2 | ns   |
| $t_C$        |                | 0.3 |                | 0.5 |                | 0.6 | ns   |
| $t_{CO}$     |                | 0.5 |                | 0.7 |                | 0.8 | ns   |
| $t_{COMB}$   |                | 0.3 |                | 0.5 |                | 0.6 | ns   |
| $t_{SU}$     | 0.5            |     | 0.7            |     | 0.8            |     | ns   |
| $t_H$        | 0.6            |     | 0.7            |     | 1.0            |     | ns   |
| $t_{PRE}$    |                | 0.9 |                | 1.2 |                | 1.6 | ns   |
| $t_{CLR}$    |                | 0.9 |                | 1.2 |                | 1.6 | ns   |
| $t_{CH}$     | 1.5            |     | 1.5            |     | 2.5            |     | ns   |
| $t_{CL}$     | 1.5            |     | 1.5            |     | 2.5            |     | ns   |

**Table 53. EPF10K130E Device IOE Timing Microparameters** *Note (1)*

| Symbol       | -1 Speed Grade |     | -2 Speed Grade |     | -3 Speed Grade |     | Unit |
|--------------|----------------|-----|----------------|-----|----------------|-----|------|
|              | Min            | Max | Min            | Max | Min            | Max |      |
| $t_{IOD}$    |                | 1.3 |                | 1.5 |                | 2.0 | ns   |
| $t_{IOC}$    |                | 0.0 |                | 0.0 |                | 0.0 | ns   |
| $t_{IOCO}$   |                | 0.6 |                | 0.8 |                | 1.0 | ns   |
| $t_{IOCOMB}$ |                | 0.6 |                | 0.8 |                | 1.0 | ns   |
| $t_{IOSU}$   | 1.0            |     | 1.2            |     | 1.6            |     | ns   |
| $t_{IOH}$    | 0.9            |     | 0.9            |     | 1.4            |     | ns   |
| $t_{IOCLR}$  |                | 0.6 |                | 0.8 |                | 1.0 | ns   |
| $t_{OD1}$    |                | 2.8 |                | 4.1 |                | 5.5 | ns   |
| $t_{OD2}$    |                | 2.8 |                | 4.1 |                | 5.5 | ns   |

**Table 71. EPF10K50S External Timing Parameters** *Note (1)*

| Symbol                   | -1 Speed Grade |     | -2 Speed Grade |     | -3 Speed Grade |      | Unit |
|--------------------------|----------------|-----|----------------|-----|----------------|------|------|
|                          | Min            | Max | Min            | Max | Min            | Max  |      |
| $t_{\text{DDR}}$         |                | 8.0 |                | 9.5 |                | 12.5 | ns   |
| $t_{\text{INSU}}^{(2)}$  | 2.4            |     | 2.9            |     | 3.9            |      | ns   |
| $t_{\text{INH}}^{(2)}$   | 0.0            |     | 0.0            |     | 0.0            |      | ns   |
| $t_{\text{OUTCO}}^{(2)}$ | 2.0            | 4.3 | 2.0            | 5.2 | 2.0            | 7.3  | ns   |
| $t_{\text{INSU}}^{(3)}$  | 2.4            |     | 2.9            |     |                |      | ns   |
| $t_{\text{INH}}^{(3)}$   | 0.0            |     | 0.0            |     |                |      | ns   |
| $t_{\text{OUTCO}}^{(3)}$ | 0.5            | 3.3 | 0.5            | 4.1 |                |      | ns   |
| $t_{\text{PCISU}}$       | 2.4            |     | 2.9            |     | —              |      | ns   |
| $t_{\text{PCIH}}$        | 0.0            |     | 0.0            |     | —              |      | ns   |
| $t_{\text{PCICO}}$       | 2.0            | 6.0 | 2.0            | 7.7 | —              | —    | ns   |

**Table 72. EPF10K50S External Bidirectional Timing Parameters** *Note (1)*

| Symbol                        | -1 Speed Grade |     | -2 Speed Grade |     | -3 Speed Grade |      | Unit |
|-------------------------------|----------------|-----|----------------|-----|----------------|------|------|
|                               | Min            | Max | Min            | Max | Min            | Max  |      |
| $t_{\text{INSUBIDIR}}^{(2)}$  | 2.7            |     | 3.2            |     | 4.3            |      | ns   |
| $t_{\text{INHBIDIR}}^{(2)}$   | 0.0            |     | 0.0            |     | 0.0            |      | ns   |
| $t_{\text{INHBIDIR}}^{(3)}$   | 0.0            |     | 0.0            |     | —              |      | ns   |
| $t_{\text{INSUBIDIR}}^{(3)}$  | 3.7            |     | 4.2            |     | —              |      | ns   |
| $t_{\text{OUTCOBIDIR}}^{(2)}$ | 2.0            | 4.5 | 2.0            | 5.2 | 2.0            | 7.3  | ns   |
| $t_{\text{XZBIDIR}}^{(2)}$    |                | 6.8 |                | 7.8 |                | 10.1 | ns   |
| $t_{\text{ZXBIDIR}}^{(2)}$    |                | 6.8 |                | 7.8 |                | 10.1 | ns   |
| $t_{\text{OUTCOBIDIR}}^{(3)}$ | 0.5            | 3.5 | 0.5            | 4.2 | —              | —    |      |
| $t_{\text{XZBIDIR}}^{(3)}$    |                | 6.8 |                | 8.4 |                | —    | ns   |
| $t_{\text{ZXBIDIR}}^{(3)}$    |                | 6.8 |                | 8.4 |                | —    | ns   |

**Notes to tables:**

- (1) All timing parameters are described in [Tables 24 through 30](#).
- (2) This parameter is measured without use of the ClockLock or ClockBoost circuits.
- (3) This parameter is measured with use of the ClockLock or ClockBoost circuits

**Table 76. EPF10K200S Device EAB Internal Timing Macroparameters** *Note (1)*

| Symbol          | -1 Speed Grade |     | -2 Speed Grade |     | -3 Speed Grade |     | Unit |
|-----------------|----------------|-----|----------------|-----|----------------|-----|------|
|                 | Min            | Max | Min            | Max | Min            | Max |      |
| $t_{EABAA}$     |                | 3.9 |                | 6.4 |                | 8.4 | ns   |
| $t_{EABRCOMB}$  | 3.9            |     | 6.4            |     | 8.4            |     | ns   |
| $t_{EABRCREG}$  | 3.6            |     | 5.7            |     | 7.6            |     | ns   |
| $t_{EABWP}$     | 2.1            |     | 4.0            |     | 5.3            |     | ns   |
| $t_{EABWCOMB}$  | 4.8            |     | 8.1            |     | 10.7           |     | ns   |
| $t_{EABWCREG}$  | 5.4            |     | 8.0            |     | 10.6           |     | ns   |
| $t_{EABDD}$     |                | 3.8 |                | 5.1 |                | 6.7 | ns   |
| $t_{EABDATAO}$  |                | 0.8 |                | 1.0 |                | 1.3 | ns   |
| $t_{EABDATASU}$ | 1.1            |     | 1.6            |     | 2.1            |     | ns   |
| $t_{EABDATAH}$  | 0.0            |     | 0.0            |     | 0.0            |     | ns   |
| $t_{EABWESU}$   | 0.7            |     | 1.1            |     | 1.5            |     | ns   |
| $t_{EABWEH}$    | 0.4            |     | 0.5            |     | 0.6            |     | ns   |
| $t_{EABWDSU}$   | 1.2            |     | 1.8            |     | 2.4            |     | ns   |
| $t_{EABWDH}$    | 0.0            |     | 0.0            |     | 0.0            |     | ns   |
| $t_{EABWASU}$   | 1.9            |     | 3.6            |     | 4.7            |     | ns   |
| $t_{EABWAH}$    | 0.8            |     | 0.5            |     | 0.7            |     | ns   |
| $t_{EABWO}$     |                | 3.1 |                | 4.4 |                | 5.8 | ns   |

**Table 77. EPF10K200S Device Interconnect Timing Microparameters (Part 1 of 2)** *Note (1)*

| Symbol           | -1 Speed Grade |     | -2 Speed Grade |      | -3 Speed Grade |      | Unit |
|------------------|----------------|-----|----------------|------|----------------|------|------|
|                  | Min            | Max | Min            | Max  | Min            | Max  |      |
| $t_{DIN2IOE}$    |                | 4.4 |                | 4.8  |                | 5.5  | ns   |
| $t_{DIN2LE}$     |                | 0.6 |                | 0.6  |                | 0.9  | ns   |
| $t_{DIN2DATA}$   |                | 1.8 |                | 2.1  |                | 2.8  | ns   |
| $t_{DCLK2IOE}$   |                | 1.7 |                | 2.0  |                | 2.8  | ns   |
| $t_{DCLK2LE}$    |                | 0.6 |                | 0.6  |                | 0.9  | ns   |
| $t_{SAMELAB}$    |                | 0.1 |                | 0.1  |                | 0.2  | ns   |
| $t_{SAMEROW}$    |                | 3.0 |                | 4.6  |                | 5.7  | ns   |
| $t_{SAMECOLUMN}$ |                | 3.5 |                | 4.9  |                | 6.4  | ns   |
| $t_{DIFFROW}$    |                | 6.5 |                | 9.5  |                | 12.1 | ns   |
| $t_{TROWROWS}$   |                | 9.5 |                | 14.1 |                | 17.8 | ns   |
| $t_{LEPERIPH}$   |                | 5.5 |                | 6.2  |                | 7.2  | ns   |
| $t_{LABCARRY}$   |                | 0.3 |                | 0.1  |                | 0.2  | ns   |

During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

SRAM configuration elements allow FLEX 10KE devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 85 ms and can be used to reconfigure an entire system dynamically. In-field upgrades can be performed by distributing new configuration files.

Before and during configuration, all I/O pins (except dedicated inputs, clock, or configuration pins) are pulled high by a weak pull-up resistor.

## Programming Files

Despite being function- and pin-compatible, FLEX 10KE devices are not programming- or configuration file-compatible with FLEX 10K or FLEX 10KA devices. A design therefore must be recompiled before it is transferred from a FLEX 10K or FLEX 10KA device to an equivalent FLEX 10KE device. This recompilation should be performed both to create a new programming or configuration file and to check design timing in FLEX 10KE devices, which has different timing characteristics than FLEX 10K or FLEX 10KA devices.

FLEX 10KE devices are generally pin-compatible with equivalent FLEX 10KA devices. In some cases, FLEX 10KE devices have fewer I/O pins than the equivalent FLEX 10KA devices. [Table 81](#) shows which FLEX 10KE devices have fewer I/O pins than equivalent FLEX 10KA devices. However, power, ground, JTAG, and configuration pins are the same on FLEX 10KA and FLEX 10KE devices, enabling migration from a FLEX 10KA design to a FLEX 10KE design.