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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	360
Number of Logic Elements/Cells	2880
Total RAM Bits	40960
Number of I/O	220
Number of Gates	199000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	356-LBGA
Supplier Device Package	356-BGA (35x35)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epf10k50sbc356-3">https://www.e-xfl.com/product-detail/intel/epf10k50sbc356-3</a>

Table 4. FLEX 10KE Package Sizes

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP RQFP	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA	599-Pin PGA	600-Pin BGA	672-Pin FineLine BGA
Pitch (mm)	0.50	0.50	0.50	1.0	1.27	1.0	—	1.27	1.0
Area (mm <sup>2</sup> )	484	936	1,197	289	1,225	529	3,904	2,025	729
Length × width (mm × mm)	22 × 22	30.6 × 30.6	34.6 × 34.6	17 × 17	35 × 35	23 × 23	62.5 × 62.5	45 × 45	27 × 27

## General Description

Altera FLEX 10KE devices are enhanced versions of FLEX 10K devices. Based on reconfigurable CMOS SRAM elements, the FLEX architecture incorporates all features necessary to implement common gate array megafunctions. With up to 200,000 typical gates, FLEX 10KE devices provide the density, speed, and features to integrate entire systems, including multiple 32-bit buses, into a single device.

The ability to reconfigure FLEX 10KE devices enables 100% testing prior to shipment and allows the designer to focus on simulation and design verification. FLEX 10KE reconfigurability eliminates inventory management for gate array designs and generation of test vectors for fault coverage.

Table 5 shows FLEX 10KE performance for some common designs. All performance values were obtained with Synopsys DesignWare or LPM functions. Special design techniques are not required to implement the applications; the designer simply infers or instantiates a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

Similar to the FLEX 10KE architecture, embedded gate arrays are the fastest-growing segment of the gate array market. As with standard gate arrays, embedded gate arrays implement general logic in a conventional “sea-of-gates” architecture. Additionally, embedded gate arrays have dedicated die areas for implementing large, specialized functions. By embedding functions in silicon, embedded gate arrays reduce die area and increase speed when compared to standard gate arrays. While embedded megafunctions typically cannot be customized, FLEX 10KE devices are programmable, providing the designer with full control over embedded megafunctions and general logic, while facilitating iterative design changes during debugging.

Each FLEX 10KE device contains an embedded array and a logic array. The embedded array is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), wide data-path manipulation, microcontroller applications, and data-transformation functions. The logic array performs the same function as the sea-of-gates in the gate array and is used to implement general logic such as counters, adders, state machines, and multiplexers. The combination of embedded and logic arrays provides the high performance and high density of embedded gate arrays, enabling designers to implement an entire system on a single device.

FLEX 10KE devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers the EPC1, EPC2, and EPC16 configuration devices, which configure FLEX 10KE devices via a serial data stream. Configuration data can also be downloaded from system RAM or via the Altera BitBlaster™, ByteBlasterMV™, or MasterBlaster download cables. After a FLEX 10KE device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 85 ms, real-time changes can be made during system operation.

FLEX 10KE devices contain an interface that permits microprocessors to configure FLEX 10KE devices serially or in-parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat a FLEX 10KE device as memory and configure it by writing to a virtual memory location, making it easy to reconfigure the device.



For more information on FLEX device configuration, see the following documents:

- *Configuration Devices for APEX & FLEX Devices Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *MasterBlaster Download Cable Data Sheet*
- *Application Note 116 (Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices)*

FLEX 10KE devices are supported by the Altera development systems, which are integrated packages that offer schematic, text (including AHDL), and waveform design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, and device configuration. The Altera software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The Altera software works easily with common gate array EDA tools for synthesis and simulation. For example, the Altera software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the Altera software contains EDA libraries that use device-specific features such as carry chains, which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the Altera development system includes DesignWare functions that are optimized for the FLEX 10KE architecture.

The Altera development system runs on Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800.



See the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet* for more information.

## Functional Description

Each FLEX 10KE device contains an enhanced embedded array to implement memory and specialized logic functions, and a logic array to implement general logic.

The embedded array consists of a series of EABs. When implementing memory functions, each EAB provides 4,096 bits, which can be used to create RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. When implementing logic, each EAB can contribute 100 to 600 gates towards complex logic functions, such as multipliers, microcontrollers, state machines, and DSP functions. EABs can be used independently, or multiple EABs can be combined to implement larger functions.

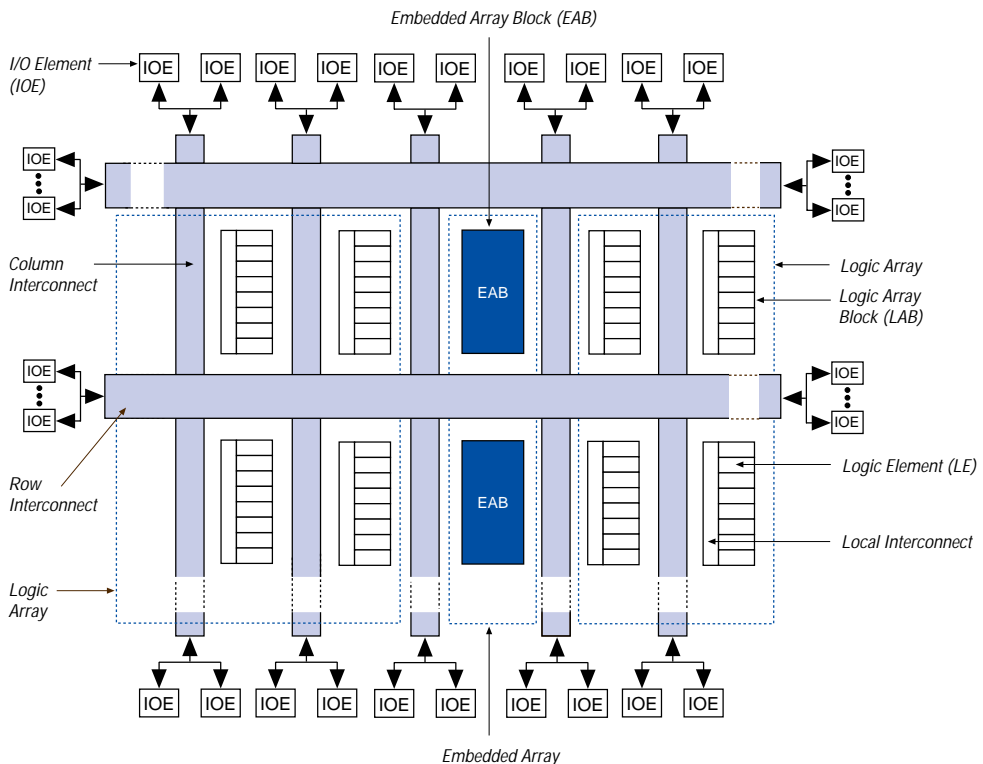
The logic array consists of logic array blocks (LABs). Each LAB contains eight LEs and a local interconnect. An LE consists of a four-input look-up table (LUT), a programmable flipflop, and dedicated signal paths for carry and cascade functions. The eight LEs can be used to create medium-sized blocks of logic—such as 8-bit counters, address decoders, or state machines—or combined across LABs to create larger logic blocks. Each LAB represents about 96 usable gates of logic.

Signal interconnections within FLEX 10KE devices (as well as to and from device pins) are provided by the FastTrack Interconnect routing structure, which is a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect routing structure. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an output or input register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. As inputs, they provide setup times as low as 0.9 ns and hold times of 0 ns. As outputs, these registers provide clock-to-output times as low as 3.0 ns. IOEs provide a variety of features, such as JTAG BST support, slew-rate control, tri-state buffers, and open-drain outputs.

Figure 1 shows a block diagram of the FLEX 10KE architecture. Each group of LEs is combined into an LAB; groups of LABs are arranged into rows and columns. Each row also contains a single EAB. The LABs and EABs are interconnected by the FastTrack Interconnect routing structure. IOEs are located at the end of each row and column of the FastTrack Interconnect routing structure.

Figure 1. FLEX 10KE Device Block Diagram

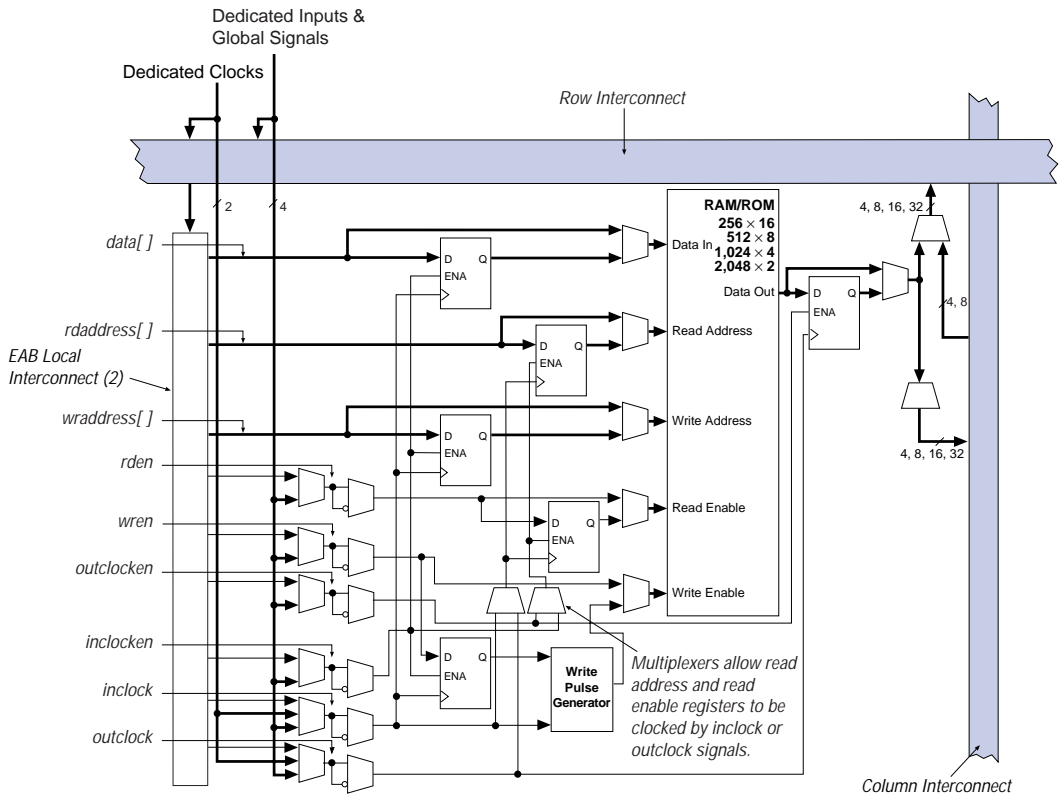


FLEX 10KE devices provide six dedicated inputs that drive the flipflops' control inputs and ensure the efficient distribution of high-speed, low-skew (less than 1.5 ns) control signals. These signals use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect routing structure. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device.

The EAB can also be used for bidirectional, dual-port memory applications where two ports read or write simultaneously. To implement this type of dual-port memory, two EABs are used to support two simultaneous read or writes.

Alternatively, one clock and clock enable can be used to control the input registers of the EAB, while a different clock and clock enable control the output registers (see Figure 2).

Figure 2. FLEX 10KE Device in Dual-Port RAM Mode *Notes (1)*

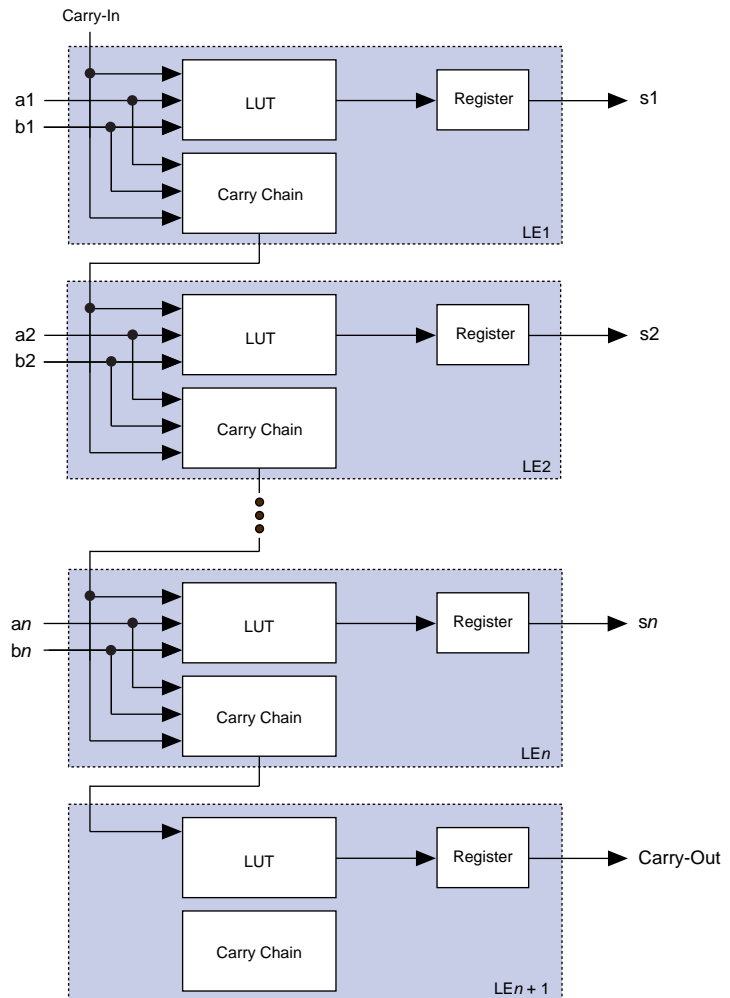


**Notes:**

- (1) All registers can be asynchronously cleared by EAB local interconnect signals, global signals, or the chip-wide reset.
- (2) EPF10K30E and EPF10K50E devices have 88 EAB local interconnect channels; EPF10K100E, EPF10K130E, and EPF10K200E devices have 104 EAB local interconnect channels.

Figure 9 shows how an  $n$ -bit full adder can be implemented in  $n + 1$  LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for an accumulator function. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal.

Figure 9. FLEX 10KE Carry Chain Operation ( $n$ -Bit Full Adder)





### **Asynchronous Clear**

The flipflop can be cleared by either LABCTRL1 or LABCTRL2. In this mode, the preset signal is tied to VCC to deactivate it.

### **Asynchronous Preset**

An asynchronous preset is implemented as an asynchronous load, or with an asynchronous clear. If DATA3 is tied to VCC, asserting LABCTRL1 asynchronously loads a one into the register. Alternatively, the Altera software can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used for one of the LE operating modes.

### **Asynchronous Preset & Clear**

When implementing asynchronous clear and preset, LABCTRL1 controls the preset and LABCTRL2 controls the clear. DATA3 is tied to VCC, so that asserting LABCTRL1 asynchronously loads a one into the register, effectively presetting the register. Asserting LABCTRL2 clears the register.

### **Asynchronous Load with Clear**

When implementing an asynchronous load in conjunction with the clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear. LABCTRL2 implements the clear by controlling the register clear; LABCTRL2 does not have to feed the preset circuits.

### **Asynchronous Load with Preset**

When implementing an asynchronous load in conjunction with preset, the Altera software provides preset control by using the clear and inverting the input and output of the register. Asserting LABCTRL2 presets the register, while asserting LABCTRL1 loads the register. The Altera software inverts the signal that drives DATA3 to account for the inversion of the register's output.

### **Asynchronous Load without Preset or Clear**

When implementing an asynchronous load without preset or clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear.

## FastTrack Interconnect Routing Structure

In the FLEX 10KE architecture, connections between LEs, EABs, and device I/O pins are provided by the FastTrack Interconnect routing structure, which is a series of continuous horizontal and vertical routing channels that traverses the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

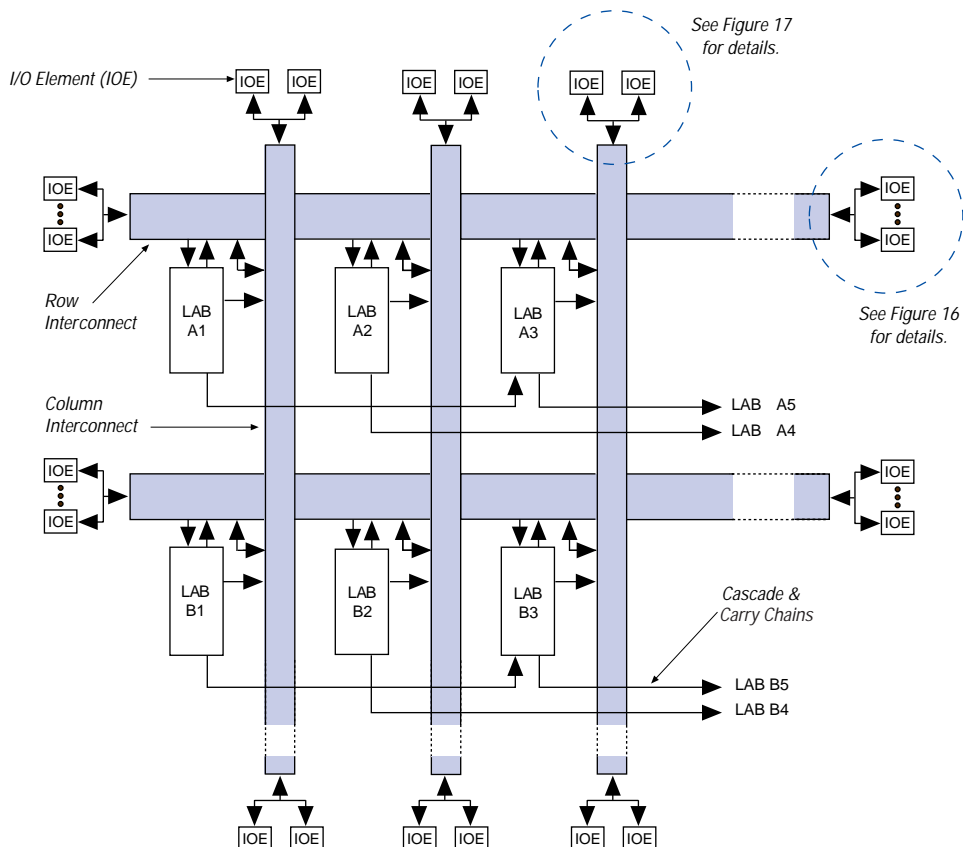
The FastTrack Interconnect routing structure consists of row and column interconnect channels that span the entire device. Each row of LABs is served by a dedicated row interconnect. The row interconnect can drive I/O pins and feed other LABs in the row. The column interconnect routes signals between rows and can drive I/O pins.

Row channels drive into the LAB or EAB local interconnect. The row signal is buffered at every LAB or EAB to reduce the effect of fan-out on delay. A row channel can be driven by an LE or by one of three column channels. These four signals feed dual 4-to-1 multiplexers that connect to two specific row channels. These multiplexers, which are connected to each LE, allow column channels to drive row channels even when all eight LEs in a LAB drive the row interconnect.

Each column of LABs or EABs is served by a dedicated column interconnect. The column interconnect that serves the EABs has twice as many channels as other column interconnects. The column interconnect can then drive I/O pins or another row's interconnect to route the signals to other LABs or EABs in the device. A signal from the column interconnect, which can be either the output of a LE or an input from an I/O pin, must be routed to the row interconnect before it can enter a LAB or EAB. Each row channel that is driven by an IOE or EAB can drive one specific column channel.

Access to row and column channels can be switched between LEs in adjacent pairs of LABs. For example, a LE in one LAB can drive the row and column channels normally driven by a particular LE in the adjacent LAB in the same row, and vice versa. This flexibility enables routing resources to be used more efficiently (see [Figure 13](#)).

Figure 14. FLEX 10KE Interconnect Resources



## I/O Element

An IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. In some cases, using an LE register for an input register will result in a faster setup time than using an IOE register. IOEs can be used as input, output, or bidirectional pins. For bidirectional registered I/O implementation, the output register should be in the IOE, and the data input and output enable registers should be LE registers placed adjacent to the bidirectional pin. The Altera Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. [Figure 15](#) shows the bidirectional I/O registers.

## ClockLock & ClockBoost Features

To support high-speed designs, FLEX 10KE devices offer optional ClockLock and ClockBoost circuitry containing a phase-locked loop (PLL) used to increase design speed and reduce resource usage. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by resource sharing within the device. The ClockBoost feature allows the designer to distribute a low-speed clock and multiply that clock on-device. Combined, the ClockLock and ClockBoost features provide significant improvements in system performance and bandwidth.

All FLEX 10KE devices, except EPF10K50E and EPF10K200E devices, support ClockLock and ClockBoost circuitry. EPF10K50S and EPF10K200S devices support this circuitry. Devices that support ClockLock and ClockBoost circuitry are distinguished with an "X" suffix in the ordering code; for instance, the EPF10K200SFC672-1X device supports this circuit.

The ClockLock and ClockBoost features in FLEX 10KE devices are enabled through the Altera software. External devices are not required to use these features. The output of the ClockLock and ClockBoost circuits is not available at any of the device pins.

The ClockLock and ClockBoost circuitry locks onto the rising edge of the incoming clock. The circuit output can drive the clock inputs of registers only; the generated clock cannot be gated or inverted.

The dedicated clock pin (`GCLK1`) supplies the clock to the ClockLock and ClockBoost circuitry. When the dedicated clock pin is driving the ClockLock or ClockBoost circuitry, it cannot drive elsewhere in the device.

For designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to the `GCLK1` pin. In the Altera software, the `GCLK1` pin can feed both the ClockLock and ClockBoost circuitry in the FLEX 10KE device. However, when both circuits are used, the other clock pin cannot be used.

## ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. Figure 19 shows the incoming and generated clock specifications.

**Figure 19. Specifications for Incoming & Generated Clocks**

The  $t_I$  parameter refers to the nominal input clock period; the  $t_O$  parameter refers to the nominal output clock period.

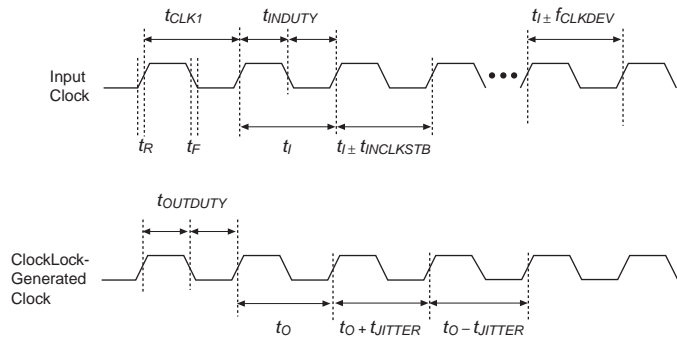


Figure 22 shows the required relationship between  $V_{CCIO}$  and  $V_{CCINT}$  for 3.3-V PCI compliance.

Figure 22. Relationship between  $V_{CCIO}$  &  $V_{CCINT}$  for 3.3-V PCI Compliance

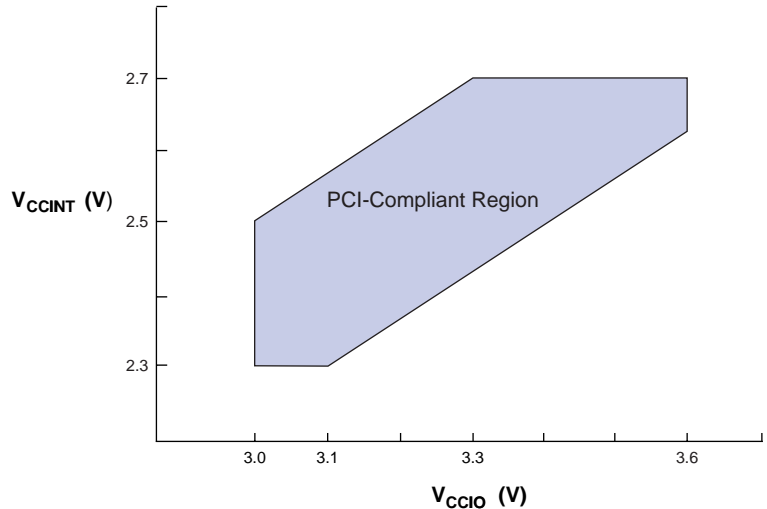


Figure 23 shows the typical output drive characteristics of FLEX 10KE devices with 3.3-V and 2.5-V  $V_{CCIO}$ . The output driver is compliant to the 3.3-V **PCI Local Bus Specification, Revision 2.2** (when  $V_{CCIO}$  pins are connected to 3.3 V). FLEX 10KE devices with a -1 speed grade also comply with the drive strength requirements of the **PCI Local Bus Specification, Revision 2.2** (when  $V_{CCINT}$  pins are powered with a minimum supply of 2.375 V, and  $V_{CCIO}$  pins are connected to 3.3 V). Therefore, these devices can be used in open 5.0-V PCI systems.

Table 33. EPF10K30E Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.7		2.0		2.3	ns
$t_{EABDATA1}$		0.6		0.7		0.8	ns
$t_{EABWE1}$		1.1		1.3		1.4	ns
$t_{EABWE2}$		0.4		0.4		0.5	ns
$t_{EABRE1}$		0.8		0.9		1.0	ns
$t_{EABRE2}$		0.4		0.4		0.5	ns
$t_{EABCLK}$		0.0		0.0		0.0	ns
$t_{EABCO}$		0.3		0.3		0.4	ns
$t_{EABYPASS}$		0.5		0.6		0.7	ns
$t_{EABSU}$	0.9		1.0		1.2		ns
$t_{EABH}$	0.4		0.4		0.5		ns
$t_{EABCLR}$	0.3		0.3		0.3		ns
$t_{AA}$		3.2		3.8		4.4	ns
$t_{WP}$	2.5		2.9		3.3		ns
$t_{RP}$	0.9		1.1		1.2		ns
$t_{WDSU}$	0.9		1.0		1.1		ns
$t_{WDH}$	0.1		0.1		0.1		ns
$t_{WASU}$	1.7		2.0		2.3		ns
$t_{WAH}$	1.8		2.1		2.4		ns
$t_{RASU}$	3.1		3.7		4.2		ns
$t_{RAH}$	0.2		0.2		0.2		ns
$t_{WO}$		2.5		2.9		3.3	ns
$t_{DD}$		2.5		2.9		3.3	ns
$t_{EABOUT}$		0.5		0.6		0.7	ns
$t_{EABCH}$	1.5		2.0		2.3		ns
$t_{EABCL}$	2.5		2.9		3.3		ns

Table 35. EPF10K30E Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		1.8		2.4		2.9	ns
$t_{DIN2LE}$		1.5		1.8		2.4	ns
$t_{DIN2DATA}$		1.5		1.8		2.2	ns
$t_{DCLK2IOE}$		2.2		2.6		3.0	ns
$t_{DCLK2LE}$		1.5		1.8		2.4	ns
$t_{SAMELAB}$		0.1		0.2		0.3	ns
$t_{SAMEROW}$		2.0		2.4		2.7	ns
$t_{SAMECOLUMN}$		0.7		1.0		0.8	ns
$t_{DIFFROW}$		2.7		3.4		3.5	ns
$t_{TWOROWS}$		4.7		5.8		6.2	ns
$t_{LEPERIPH}$		2.7		3.4		3.8	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.8		0.8		1.1	ns

Table 36. EPF10K30E External Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DDR}$		8.0		9.5		12.5	ns
$t_{INSU}$ (3)	2.1		2.5		3.9		ns
$t_{INH}$ (3)	0.0		0.0		0.0		ns
$t_{OUTCO}$ (3)	2.0	4.9	2.0	5.9	2.0	7.6	ns
$t_{INSU}$ (4)	1.1		1.5		—		ns
$t_{INH}$ (4)	0.0		0.0		—		ns
$t_{OUTCO}$ (4)	0.5	3.9	0.5	4.9	—	—	ns
$t_{PCISU}$	3.0		4.2		—		ns
$t_{PCIH}$	0.0		0.0		—		ns
$t_{PCICO}$	2.0	6.0	2.0	7.5	—	—	ns



Table 41. EPF10K50E Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABAA}$		6.4		7.6		10.2	ns
$t_{EABRCOMB}$	6.4		7.6		10.2		ns
$t_{EABRCREG}$	4.4		5.1		7.0		ns
$t_{EABWP}$	2.5		2.9		3.9		ns
$t_{EABWCOMB}$	6.0		7.0		9.5		ns
$t_{EABWCREG}$	6.8		7.8		10.6		ns
$t_{EABDD}$		5.7		6.7		9.0	ns
$t_{EABDATACO}$		0.8		0.9		1.3	ns
$t_{EABDATASU}$	1.5		1.7		2.3		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	1.3		1.4		2.0		ns
$t_{EABWEH}$	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.5		1.7		2.3		ns
$t_{EABWDH}$	0.0		0.0		0.0		ns
$t_{EABWASU}$	3.0		3.6		4.8		ns
$t_{EABWAH}$	0.5		0.5		0.8		ns
$t_{EABWO}$		5.1		6.0		8.1	ns

Table 42. EPF10K50E Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		3.5		4.3		5.6	ns
$t_{DIN2LE}$		2.1		2.5		3.4	ns
$t_{DIN2DATA}$		2.2		2.4		3.1	ns
$t_{DCLK2IOE}$		2.9		3.5		4.7	ns
$t_{DCLK2LE}$		2.1		2.5		3.4	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		1.1		1.1		1.5	ns
$t_{SAMECOLUMN}$		0.8		1.0		1.3	ns
$t_{DIFFROW}$		1.9		2.1		2.8	ns
$t_{TWOROWS}$		3.0		3.2		4.3	ns
$t_{LEPERIPH}$		3.1		3.3		3.7	ns
$t_{LABCARRY}$		0.1		0.1		0.2	ns
$t_{LABCASC}$		0.3		0.3		0.5	ns

Table 58. EPF10K130E External Bidirectional Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$ (3)	2.2		2.4		3.2		ns
$t_{\text{INHBIDIR}}$ (3)	0.0		0.0		0.0		ns
$t_{\text{INSUBIDIR}}$ (4)	2.8		3.0		—		ns
$t_{\text{INHBIDIR}}$ (4)	0.0		0.0		—		ns
$t_{\text{OUTCOBIDIR}}$ (3)	2.0	5.0	2.0	7.0	2.0	9.2	ns
$t_{\text{XZBIDIR}}$ (3)		5.6		8.1		10.8	ns
$t_{\text{XZBIDIR}}$ (3)		5.6		8.1		10.8	ns
$t_{\text{OUTCOBIDIR}}$ (4)	0.5	4.0	0.5	6.0	—	—	ns
$t_{\text{XZBIDIR}}$ (4)		4.6		7.1		—	ns
$t_{\text{XZBIDIR}}$ (4)		4.6		7.1		—	ns

**Notes to tables:**

- (1) All timing parameters are described in Tables 24 through 30 in this data sheet.
- (2) These parameters are specified by characterization.
- (3) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
- (4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 59 through 65 show EPF10K200E device internal and external timing parameters.

Table 59. EPF10K200E Device LE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{LUT}}$		0.7		0.8		1.2	ns
$t_{\text{CLUT}}$		0.4		0.5		0.6	ns
$t_{\text{RLUT}}$		0.6		0.7		0.9	ns
$t_{\text{PACKED}}$		0.3		0.5		0.7	ns
$t_{\text{EN}}$		0.4		0.5		0.6	ns
$t_{\text{CICO}}$		0.2		0.2		0.3	ns
$t_{\text{CGEN}}$		0.4		0.4		0.6	ns
$t_{\text{CGENR}}$		0.2		0.2		0.3	ns
$t_{\text{CASC}}$		0.7		0.8		1.2	ns
$t_{\text{C}}$		0.5		0.6		0.8	ns
$t_{\text{CO}}$		0.5		0.6		0.8	ns
$t_{\text{COMB}}$		0.4		0.6		0.8	ns
$t_{\text{SU}}$	0.4		0.6		0.7		ns

Table 62. EPF10K200E Device EAB Internal Timing Macroparameters (Part 2 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABWCOMB}$	6.7		8.1		10.7		ns
$t_{EABWCREG}$	6.6		8.0		10.6		ns
$t_{EABDD}$		4.0		5.1		6.7	ns
$t_{EABDATAO}$		0.8		1.0		1.3	ns
$t_{EABDATASU}$	1.3		1.6		2.1		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	0.9		1.1		1.5		ns
$t_{EABWEH}$	0.4		0.5		0.6		ns
$t_{EABWDSU}$	1.5		1.8		2.4		ns
$t_{EABWDH}$	0.0		0.0		0.0		ns
$t_{EABWASU}$	3.0		3.6		4.7		ns
$t_{EABWAH}$	0.4		0.5		0.7		ns
$t_{EABWO}$		3.4		4.4		5.8	ns

Table 63. EPF10K200E Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		4.2		4.6		5.7	ns
$t_{DIN2LE}$		1.7		1.7		2.0	ns
$t_{DIN2DATA}$		1.9		2.1		3.0	ns
$t_{DCLK2IOE}$		2.5		2.9		4.0	ns
$t_{DCLK2LE}$		1.7		1.7		2.0	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		2.3		2.6		3.6	ns
$t_{SAMECOLUMN}$		2.5		2.7		4.1	ns
$t_{DIFFROW}$		4.8		5.3		7.7	ns
$t_{TROWROWS}$		7.1		7.9		11.3	ns
$t_{LEPERIPH}$		7.0		7.6		9.0	ns
$t_{LABCARRY}$		0.1		0.1		0.2	ns
$t_{LABCASC}$		0.9		1.0		1.4	ns

Table 66. EPF10K50S Device LE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CGENR}$		0.1		0.1		0.1	ns
$t_{CASC}$		0.5		0.8		1.0	ns
$t_C$		0.5		0.6		0.8	ns
$t_{CO}$		0.6		0.6		0.7	ns
$t_{COMB}$		0.3		0.4		0.5	ns
$t_{SU}$	0.5		0.6		0.7		ns
$t_H$	0.5		0.6		0.8		ns
$t_{PRE}$		0.4		0.5		0.7	ns
$t_{CLR}$		0.8		1.0		1.2	ns
$t_{CH}$	2.0		2.5		3.0		ns
$t_{CL}$	2.0		2.5		3.0		ns

Table 67. EPF10K50S Device IOE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{IOD}$		1.3		1.3		1.9	ns
$t_{IOC}$		0.3		0.4		0.4	ns
$t_{IOCO}$		1.7		2.1		2.6	ns
$t_{IOCOMB}$		0.5		0.6		0.8	ns
$t_{IOSU}$	0.8		1.0		1.3		ns
$t_{IOH}$	0.4		0.5		0.6		ns
$t_{IOCLR}$		0.2		0.2		0.4	ns
$t_{OD1}$		1.2		1.2		1.9	ns
$t_{OD2}$		0.7		0.8		1.7	ns
$t_{OD3}$		2.7		3.0		4.3	ns
$t_{XZ}$		4.7		5.7		7.5	ns
$t_{ZX1}$		4.7		5.7		7.5	ns
$t_{ZX2}$		4.2		5.3		7.3	ns
$t_{ZX3}$		6.2		7.5		9.9	ns
$t_{INREG}$		3.5		4.2		5.6	ns
$t_{IOFD}$		1.1		1.3		1.8	ns
$t_{INCOMB}$		1.1		1.3		1.8	ns

Additionally, the Altera software offers several features that help plan for future device migration by preventing the use of conflicting I/O pins.

*Table 81. I/O Counts for FLEX 10KA & FLEX 10KE Devices*

FLEX 10KA		FLEX 10KE	
Device	I/O Count	Device	I/O Count
EPF10K30AF256	191	EPF10K30EF256	176
EPF10K30AF484	246	EPF10K30EF484	220
EPF10K50VB356	274	EPF10K50SB356	220
EPF10K50VF484	291	EPF10K50EF484	254
EPF10K50VF484	291	EPF10K50SF484	254
EPF10K100AF484	369	EPF10K100EF484	338

## Configuration Schemes

The configuration data for a FLEX 10KE device can be loaded with one of five configuration schemes (see [Table 82](#)), chosen on the basis of the target application. An EPC1, EPC2, or EPC16 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of a FLEX 10KE device, allowing automatic configuration on system power-up.

Multiple FLEX 10KE devices can be configured in any of the five configuration schemes by connecting the configuration enable ( $\overline{nCE}$ ) and configuration enable output ( $\overline{nCEO}$ ) pins on each device. Additional FLEX 10K, FLEX 10KA, FLEX 10KE, and FLEX 6000 devices can be configured in the same serial chain.

*Table 82. Data Sources for FLEX 10KE Configuration*

Configuration Scheme	Data Source
Configuration device	EPC1, EPC2, or EPC16 configuration device
Passive serial (PS)	BitBlaster, ByteBlasterMV, or MasterBlaster download cables, or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	BitBlaster or ByteBlasterMV download cables, or microprocessor with a Jam STAPL file or JBC file