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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	360
Number of Logic Elements/Cells	2880
Total RAM Bits	40960
Number of I/O	191
Number of Gates	199000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epf10k50sfc256-1">https://www.e-xfl.com/product-detail/intel/epf10k50sfc256-1</a>

Similar to the FLEX 10KE architecture, embedded gate arrays are the fastest-growing segment of the gate array market. As with standard gate arrays, embedded gate arrays implement general logic in a conventional “sea-of-gates” architecture. Additionally, embedded gate arrays have dedicated die areas for implementing large, specialized functions. By embedding functions in silicon, embedded gate arrays reduce die area and increase speed when compared to standard gate arrays. While embedded megafunctions typically cannot be customized, FLEX 10KE devices are programmable, providing the designer with full control over embedded megafunctions and general logic, while facilitating iterative design changes during debugging.

Each FLEX 10KE device contains an embedded array and a logic array. The embedded array is used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), wide data-path manipulation, microcontroller applications, and data-transformation functions. The logic array performs the same function as the sea-of-gates in the gate array and is used to implement general logic such as counters, adders, state machines, and multiplexers. The combination of embedded and logic arrays provides the high performance and high density of embedded gate arrays, enabling designers to implement an entire system on a single device.

FLEX 10KE devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers the EPC1, EPC2, and EPC16 configuration devices, which configure FLEX 10KE devices via a serial data stream. Configuration data can also be downloaded from system RAM or via the Altera BitBlaster™, ByteBlasterMV™, or MasterBlaster download cables. After a FLEX 10KE device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 85 ms, real-time changes can be made during system operation.

FLEX 10KE devices contain an interface that permits microprocessors to configure FLEX 10KE devices serially or in-parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat a FLEX 10KE device as memory and configure it by writing to a virtual memory location, making it easy to reconfigure the device.

### Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Altera Compiler automatically selects the carry-in or the `DATA3` signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. Either the register or the LUT can be used to drive both the local interconnect and the FastTrack Interconnect routing structure at the same time.

The LUT and the register in the LE can be used independently (register packing). To support register packing, the LE has two outputs; one drives the local interconnect, and the other drives the FastTrack Interconnect routing structure. The `DATA4` signal can drive the register directly, allowing the LUT to compute a function that is independent of the registered signal; a three-input function can be computed in the LUT, and a fourth independent signal can be registered. Alternatively, a four-input function can be generated, and one of the inputs to this function can be used to drive the register. The register in a packed LE can still use the clock enable, clear, and preset signals in the LE. In a packed LE, the register can drive the FastTrack Interconnect routing structure while the LUT drives the local interconnect, or vice versa.

### Arithmetic Mode

The arithmetic mode offers 2 three-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT computes a three-input function; the other generates a carry output. As shown in [Figure 11](#) on [page 22](#), the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three signals: `a`, `b`, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain.

### Up/Down Counter Mode

The up/down counter mode offers counter enable, clock enable, synchronous up/down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Use 2 three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the clear and preset register control signals without using the LUT resources.

### Clearable Counter Mode

The clearable counter mode is similar to the up/down counter mode, but supports a synchronous clear instead of the up/down control. The clear function is substituted for the cascade-in signal in the up/down counter mode. Use 2 three-input LUTs: one generates the counter data, and the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer. The output of this multiplexer is ANDed with a synchronous clear signal.

### *Internal Tri-State Emulation*

Internal tri-state emulation provides internal tri-states without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable (OE) signals select which signal drives the bus. However, if multiple OE signals are active, contending signals can be driven onto the bus. Conversely, if no OE signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The Altera software automatically implements tri-state bus functionality with a multiplexer.

### *Clear & Preset Logic Control*

Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. The clear and preset control structure of the LE asynchronously loads signals into a register. Either LABCTRL1 or LABCTRL2 can control the asynchronous clear. Alternatively, the register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

During compilation, the Altera Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six modes chosen during design entry:

- Asynchronous clear
- Asynchronous preset
- Asynchronous clear and preset
- Asynchronous load with clear
- Asynchronous load with preset
- Asynchronous load without clear or preset

For improved routing, the row interconnect consists of a combination of full-length and half-length channels. The full-length channels connect to all LABs in a row; the half-length channels connect to the LABs in half of the row. The EAB can be driven by the half-length channels in the left half of the row and by the full-length channels. The EAB drives out to the full-length channels. In addition to providing a predictable, row-wide interconnect, this architecture provides increased routing resources. Two neighboring LABs can be connected using a half-row channel, thereby saving the other half of the channel for the other half of the row.

**Table 7** summarizes the FastTrack Interconnect routing structure resources available in each FLEX 10KE device.

<i>Table 7. FLEX 10KE FastTrack Interconnect Resources</i>				
Device	Rows	Channels per Row	Columns	Channels per Column
EPF10K30E	6	216	36	24
EPF10K50E EPF10K50S	10	216	36	24
EPF10K100E	12	312	52	24
EPF10K130E	16	312	52	32
EPF10K200E EPF10K200S	24	312	52	48

In addition to general-purpose I/O pins, FLEX 10KE devices have six dedicated input pins that provide low-skew signal distribution across the device. These six inputs can be used for global clock, clear, preset, and peripheral output enable and clock enable control signals. These signals are available as control signals for all LABs and IOEs in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device.

**Figure 14** shows the interconnection of adjacent LABs and EABs, with row, column, and local interconnects, as well as the associated cascade and carry chains. Each LAB is labeled according to its location: a letter represents the row and a number represents the column. For example, LAB B3 is in row B, column 3.

When dedicated inputs drive non-inverted and inverted peripheral clears, clock enables, and output enables, two signals on the peripheral control bus will be used.

Tables 8 and 9 list the sources for each peripheral control signal, and show how the output enable, clock enable, clock, and clear signals share 12 peripheral control signals. The tables also show the rows that can drive global signals.

*Table 8. Peripheral Bus Sources for EPF10K30E, EPF10K50E & EPF10K50S Devices*

Peripheral Control Signal	EPF10K30E	EPF10K50E EPF10K50S
OE0	Row A	Row A
OE1	Row B	Row B
OE2	Row C	Row D
OE3	Row D	Row F
OE4	Row E	Row H
OE5	Row F	Row J
CLKENA0/CLK0/GLOBAL0	Row A	Row A
CLKENA1/OE6/GLOBAL1	Row B	Row C
CLKENA2/CLR0	Row C	Row E
CLKENA3/OE7/GLOBAL2	Row D	Row G
CLKENA4/CLR1	Row E	Row I
CLKENA5/CLK1/GLOBAL3	Row F	Row J

### Row-to-IOE Connections

When an IOE is used as an input signal, it can drive two separate row channels. The signal is accessible by all LEs within that row. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the row channels. Up to eight IOEs connect to each side of each row channel (see Figure 16).

**Figure 16. FLEX 10KE Row-to-IOE Connections**

The values for  $m$  and  $n$  are provided in Table 10.

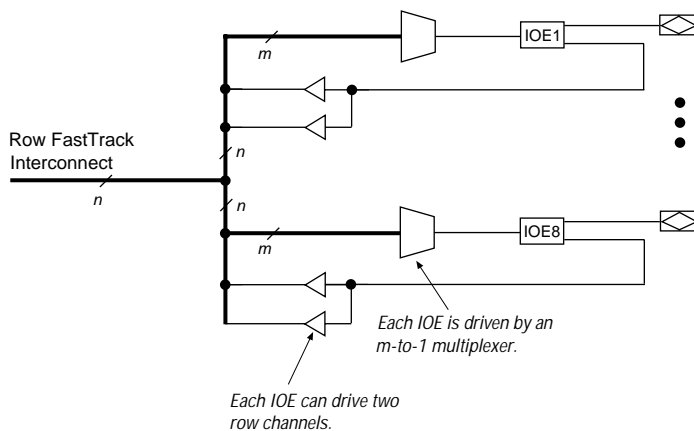


Table 10 lists the FLEX 10KE row-to-IOE interconnect resources.

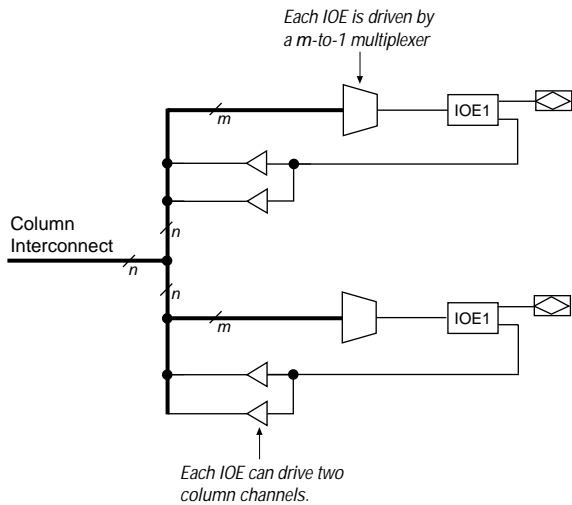
Table 10. FLEX 10KE Row-to-IOE Interconnect Resources		
Device	Channels per Row ( $n$ )	Row Channels per Pin ( $m$ )
EPF10K30E	216	27
EPF10K50E EPF10K50S	216	27
EPF10K100E	312	39
EPF10K130E	312	39
EPF10K200E EPF10K200S	312	39

Column-to-IOE Connections

When an IOE is used as an input, it can drive up to two separate column channels. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the column channels. Two IOEs connect to each side of the column channels. Each IOE can be driven by column channels via a multiplexer. The set of column channels is different for each IOE (see [Figure 17](#)).

Figure 17. FLEX 10KE Column-to-IOE Connections

The values for *m* and *n* are provided in [Table 11](#).



[Table 11](#) lists the FLEX 10KE column-to-IOE interconnect resources.

Table 11. FLEX 10KE Column-to-IOE Interconnect Resources		
Device	Channels per Column ( <i>n</i> )	Column Channels per Pin ( <i>m</i> )
EPF10K30E	24	16
EPF10K50E EPF10K50S	24	16
EPF10K100E	24	16
EPF10K130E	32	24
EPF10K200E EPF10K200S	48	40



*Table 17. 32-Bit IDCODE for FLEX 10KE Devices* *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) (2)
EPF10K30E	0001	0001 0000 0011 0000	00001101110	1
EPF10K50E EPF10K50S	0001	0001 0000 0101 0000	00001101110	1
EPF10K100E	0010	0000 0001 0000 0000	00001101110	1
EPF10K130E	0001	0000 0001 0011 0000	00001101110	1
EPF10K200E EPF10K200S	0001	0000 0010 0000 0000	00001101110	1

**Notes:**

- (1) The most significant bit (MSB) is on the left.  
 (2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

FLEX 10KE devices include weak pull-up resistors on the JTAG pins.



For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Jam Programming & Test Language Specification*

Figure 22 shows the required relationship between  $V_{CCIO}$  and  $V_{CCINT}$  for 3.3-V PCI compliance.

Figure 22. Relationship between  $V_{CCIO}$  &  $V_{CCINT}$  for 3.3-V PCI Compliance

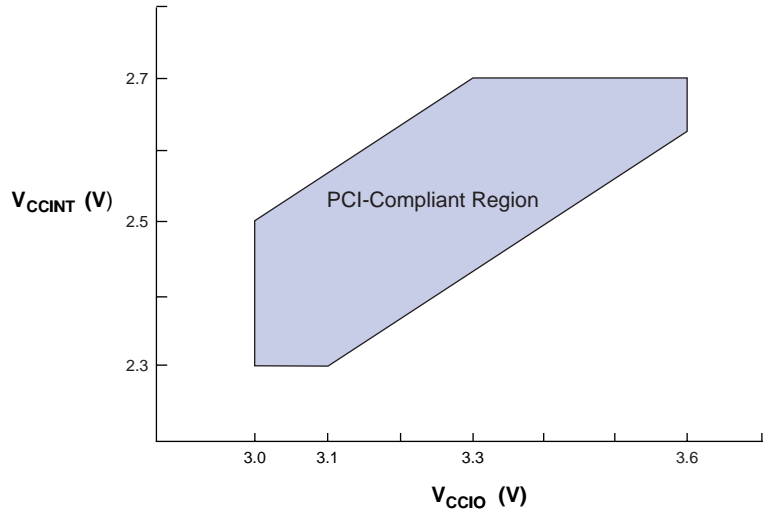


Figure 23 shows the typical output drive characteristics of FLEX 10KE devices with 3.3-V and 2.5-V  $V_{CCIO}$ . The output driver is compliant to the 3.3-V **PCI Local Bus Specification, Revision 2.2** (when  $V_{CCIO}$  pins are connected to 3.3 V). FLEX 10KE devices with a -1 speed grade also comply with the drive strength requirements of the **PCI Local Bus Specification, Revision 2.2** (when  $V_{CCINT}$  pins are powered with a minimum supply of 2.375 V, and  $V_{CCIO}$  pins are connected to 3.3 V). Therefore, these devices can be used in open 5.0-V PCI systems.

**Table 30. External Bidirectional Timing Parameters** *Note (9)*

Symbol	Parameter	Conditions
$t_{\text{INSUBIDIR}}$	Setup time for bi-directional pins with global clock at same-row or same-column LE register	
$t_{\text{INHBIDIR}}$	Hold time for bidirectional pins with global clock at same-row or same-column LE register	
$t_{\text{INH}}$	Hold time with global clock at IOE register	
$t_{\text{OUTCOBIDIR}}$	Clock-to-output delay for bidirectional pins with global clock at IOE register	C1 = 35 pF
$t_{\text{XZBIDIR}}$	Synchronous IOE output buffer disable delay	C1 = 35 pF
$t_{\text{ZXBIDIR}}$	Synchronous IOE output buffer enable delay, slow slew rate= off	C1 = 35 pF

**Notes to tables:**

- (1) Microparameters are timing delays contributed by individual architectural elements. These parameters cannot be measured explicitly.
- (2) Operating conditions:  $V_{\text{CCIO}} = 3.3 \text{ V} \pm 10\%$  for commercial or industrial use.
- (3) Operating conditions:  $V_{\text{CCIO}} = 2.5 \text{ V} \pm 5\%$  for commercial or industrial use in EPF10K30E, EPF10K50S, EPF10K100E, EPF10K130E, and EPF10K200S devices.
- (4) Operating conditions:  $V_{\text{CCIO}} = 3.3 \text{ V}$ .
- (5) Because the RAM in the EAB is self-timed, this parameter can be ignored when the  $\text{WE}$  signal is registered.
- (6) EAB macroparameters are internal parameters that can simplify predicting the behavior of an EAB at its boundary; these parameters are calculated by summing selected microparameters.
- (7) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.
- (8) Contact Altera Applications for test circuit specifications and test conditions.
- (9) This timing parameter is sample-tested only.
- (10) This parameter is measured with the measurement and test conditions, including load, specified in the PCI Local Bus Specification, revision 2.2.

Table 31. EPF10K30E Device LE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CGENR}$		0.1		0.1		0.2	ns
$t_{CASC}$		0.6		0.8		1.0	ns
$t_C$		0.0		0.0		0.0	ns
$t_{CO}$		0.3		0.4		0.5	ns
$t_{COMB}$		0.4		0.4		0.6	ns
$t_{SU}$	0.4		0.6		0.6		ns
$t_H$	0.7		1.0		1.3		ns
$t_{PRE}$		0.8		0.9		1.2	ns
$t_{CLR}$		0.8		0.9		1.2	ns
$t_{CH}$	2.0		2.5		2.5		ns
$t_{CL}$	2.0		2.5		2.5		ns

Table 32. EPF10K30E Device IOE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{IOD}$		2.4		2.8		3.8	ns
$t_{IOC}$		0.3		0.4		0.5	ns
$t_{IOCO}$		1.0		1.1		1.6	ns
$t_{IOCOMB}$		0.0		0.0		0.0	ns
$t_{IOSU}$	1.2		1.4		1.9		ns
$t_{IOH}$	0.3		0.4		0.5		ns
$t_{IOCLR}$		1.0		1.1		1.6	ns
$t_{OD1}$		1.9		2.3		3.0	ns
$t_{OD2}$		1.4		1.8		2.5	ns
$t_{OD3}$		4.4		5.2		7.0	ns
$t_{XZ}$		2.7		3.1		4.3	ns
$t_{ZX1}$		2.7		3.1		4.3	ns
$t_{ZX2}$		2.2		2.6		3.8	ns
$t_{ZX3}$		5.2		6.0		8.3	ns
$t_{INREG}$		3.4		4.1		5.5	ns
$t_{IOFD}$		0.8		1.3		2.4	ns
$t_{INCOMB}$		0.8		1.3		2.4	ns

Table 35. EPF10K30E Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		1.8		2.4		2.9	ns
$t_{DIN2LE}$		1.5		1.8		2.4	ns
$t_{DIN2DATA}$		1.5		1.8		2.2	ns
$t_{DCLK2IOE}$		2.2		2.6		3.0	ns
$t_{DCLK2LE}$		1.5		1.8		2.4	ns
$t_{SAMELAB}$		0.1		0.2		0.3	ns
$t_{SAMEROW}$		2.0		2.4		2.7	ns
$t_{SAMECOLUMN}$		0.7		1.0		0.8	ns
$t_{DIFFROW}$		2.7		3.4		3.5	ns
$t_{TWOROWS}$		4.7		5.8		6.2	ns
$t_{LEPERIPH}$		2.7		3.4		3.8	ns
$t_{LABCARRY}$		0.3		0.4		0.5	ns
$t_{LABCASC}$		0.8		0.8		1.1	ns

Table 36. EPF10K30E External Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DDR}$		8.0		9.5		12.5	ns
$t_{INSU}$ (3)	2.1		2.5		3.9		ns
$t_{INH}$ (3)	0.0		0.0		0.0		ns
$t_{OUTCO}$ (3)	2.0	4.9	2.0	5.9	2.0	7.6	ns
$t_{INSU}$ (4)	1.1		1.5		—		ns
$t_{INH}$ (4)	0.0		0.0		—		ns
$t_{OUTCO}$ (4)	0.5	3.9	0.5	4.9	—	—	ns
$t_{PCISU}$	3.0		4.2		—		ns
$t_{PCIH}$	0.0		0.0		—		ns
$t_{PCICO}$	2.0	6.0	2.0	7.5	—	—	ns

Table 45. EPF10K100E Device LE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CGENR}$		0.1		0.1		0.2	ns
$t_{CASC}$		0.6		0.9		1.2	ns
$t_C$		0.8		1.0		1.4	ns
$t_{CO}$		0.6		0.8		1.1	ns
$t_{COMB}$		0.4		0.5		0.7	ns
$t_{SU}$	0.4		0.6		0.7		ns
$t_H$	0.5		0.7		0.9		ns
$t_{PRE}$		0.8		1.0		1.4	ns
$t_{CLR}$		0.8		1.0		1.4	ns
$t_{CH}$	1.5		2.0		2.5		ns
$t_{CL}$	1.5		2.0		2.5		ns

Table 46. EPF10K100E Device IOE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{IOD}$		1.7		2.0		2.6	ns
$t_{IOC}$		0.0		0.0		0.0	ns
$t_{IOCO}$		1.4		1.6		2.1	ns
$t_{IOCOMB}$		0.5		0.7		0.9	ns
$t_{IOSU}$	0.8		1.0		1.3		ns
$t_{IOH}$	0.7		0.9		1.2		ns
$t_{IOCLR}$		0.5		0.7		0.9	ns
$t_{OD1}$		3.0		4.2		5.6	ns
$t_{OD2}$		3.0		4.2		5.6	ns
$t_{OD3}$		4.0		5.5		7.3	ns
$t_{XZ}$		3.5		4.6		6.1	ns
$t_{ZX1}$		3.5		4.6		6.1	ns
$t_{ZX2}$		3.5		4.6		6.1	ns
$t_{ZX3}$		4.5		5.9		7.8	ns
$t_{INREG}$		2.0		2.6		3.5	ns
$t_{IOFD}$		0.5		0.8		1.2	ns
$t_{INCOMB}$		0.5		0.8		1.2	ns

Table 53. EPF10K130E Device IOE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{OD3}$		4.0		5.6		7.5	ns
$t_{XZ}$		2.8		4.1		5.5	ns
$t_{ZX1}$		2.8		4.1		5.5	ns
$t_{ZX2}$		2.8		4.1		5.5	ns
$t_{ZX3}$		4.0		5.6		7.5	ns
$t_{INREG}$		2.5		3.0		4.1	ns
$t_{IOFD}$		0.4		0.5		0.6	ns
$t_{INCOMB}$		0.4		0.5		0.6	ns

Table 54. EPF10K130E Device EAB Internal Microparameters (Part 1 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.5		2.0		2.6	ns
$t_{EABDATA2}$		0.0		0.0		0.0	ns
$t_{EABWE1}$		1.5		2.0		2.6	ns
$t_{EABWE2}$		0.3		0.4		0.5	ns
$t_{EABRE1}$		0.3		0.4		0.5	ns
$t_{EABRE2}$		0.0		0.0		0.0	ns
$t_{EABCLK}$		0.0		0.0		0.0	ns
$t_{EABCO}$		0.3		0.4		0.5	ns
$t_{EABYPASS}$		0.1		0.1		0.2	ns
$t_{EABSU}$	0.8		1.0		1.4		ns
$t_{EABH}$	0.1		0.2		0.2		ns
$t_{EABCLR}$	0.3		0.4		0.5		ns
$t_{AA}$		4.0		5.0		6.6	ns
$t_{WP}$	2.7		3.5		4.7		ns
$t_{RP}$	1.0		1.3		1.7		ns
$t_{WDSU}$	1.0		1.3		1.7		ns
$t_{WDH}$	0.2		0.2		0.3		ns
$t_{WASU}$	1.6		2.1		2.8		ns
$t_{WAH}$	1.6		2.1		2.8		ns
$t_{RASU}$	3.0		3.9		5.2		ns
$t_{RAH}$	0.1		0.1		0.2		ns
$t_{WO}$		1.5		2.0		2.6	ns

Table 54. EPF10K130E Device EAB Internal Microparameters (Part 2 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DD}$		1.5		2.0		2.6	ns
$t_{EABOUT}$		0.2		0.3		0.3	ns
$t_{EABCH}$	1.5		2.0		2.5		ns
$t_{EABCL}$	2.7		3.5		4.7		ns

Table 55. EPF10K130E Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABAA}$		5.9		7.5		9.9	ns
$t_{EABRCOMB}$	5.9		7.5		9.9		ns
$t_{EABRCREG}$	5.1		6.4		8.5		ns
$t_{EABWP}$	2.7		3.5		4.7		ns
$t_{EABWCOMB}$	5.9		7.7		10.3		ns
$t_{EABWCREG}$	5.4		7.0		9.4		ns
$t_{EABDD}$		3.4		4.5		5.9	ns
$t_{EABDATA CO}$		0.5		0.7		0.8	ns
$t_{EABDATASU}$	0.8		1.0		1.4		ns
$t_{EABDATAH}$	0.1		0.1		0.2		ns
$t_{EABWESU}$	1.1		1.4		1.9		ns
$t_{EABWEH}$	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.0		1.3		1.7		ns
$t_{EABWDH}$	0.2		0.2		0.3		ns
$t_{EABWASU}$	4.1		5.1		6.8		ns
$t_{EABWAH}$	0.0		0.0		0.0		ns
$t_{EABWO}$		3.4		4.5		5.9	ns



Table 56. EPF10K130E Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		2.8		3.5		4.4	ns
$t_{DIN2LE}$		0.7		1.2		1.6	ns
$t_{DIN2DATA}$		1.6		1.9		2.2	ns
$t_{DCLK2IOE}$		1.6		2.1		2.7	ns
$t_{DCLK2LE}$		0.7		1.2		1.6	ns
$t_{SAMELAB}$		0.1		0.2		0.2	ns
$t_{SAMEROW}$		1.9		3.4		5.1	ns
$t_{SAMECOLUMN}$		0.9		2.6		4.4	ns
$t_{DIFFROW}$		2.8		6.0		9.5	ns
$t_{TWOROWS}$		4.7		9.4		14.6	ns
$t_{LEPERIPH}$		3.1		4.7		6.9	ns
$t_{LABCARRY}$		0.6		0.8		1.0	ns
$t_{LABCASC}$		0.9		1.2		1.6	ns

Table 57. EPF10K130E External Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DRR}$		9.0		12.0		16.0	ns
$t_{INSU}^{(3)}$	1.9		2.1		3.0		ns
$t_{INH}^{(3)}$	0.0		0.0		0.0		ns
$t_{OUTCO}^{(3)}$	2.0	5.0	2.0	7.0	2.0	9.2	ns
$t_{INSU}^{(4)}$	0.9		1.1		—		ns
$t_{INH}^{(4)}$	0.0		0.0		—		ns
$t_{OUTCO}^{(4)}$	0.5	4.0	0.5	6.0	—	—	ns
$t_{PCISU}$	3.0		6.2		—		ns
$t_{PCIH}$	0.0		0.0		—		ns
$t_{PCICO}$	2.0	6.0	2.0	6.9	—	—	ns

Table 64. EPF10K200E External Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{DRR}}$		10.0		12.0		16.0	ns
$t_{\text{INSU}}$	2.8		3.4		4.4		ns
$t_{\text{INH}}$	0.0		0.0		0.0		ns
$t_{\text{OUTCO}}$	2.0	4.5	2.0	5.3	2.0	7.8	ns
$t_{\text{PCISU}}$	3.0		6.2		-		ns
$t_{\text{PCIH}}$	0.0		0.0		-		ns
$t_{\text{PCICO}}$	2.0	6.0	2.0	8.9	-	-	ns

Table 65. EPF10K200E External Bidirectional Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{INSUBIDIR}}$	3.0		4.0		5.5		ns
$t_{\text{INHBIDIR}}$	0.0		0.0		0.0		ns
$t_{\text{OUTCOBIDIR}}$	2.0	4.5	2.0	5.3	2.0	7.8	ns
$t_{\text{XZBIDIR}}$		8.1		9.5		13.0	ns
$t_{\text{ZXBIDIR}}$		8.1		9.5		13.0	ns

**Notes to tables:**

- (1) All timing parameters are described in [Tables 24](#) through [30](#) in this data sheet.  
 (2) These parameters are specified by characterization.

[Tables 66](#) through [79](#) show EPF10K50S and EPF10K200S device external timing parameters.

Table 66. EPF10K50S Device LE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{\text{LUT}}$		0.6		0.8		1.1	ns
$t_{\text{CLUT}}$		0.5		0.6		0.8	ns
$t_{\text{RLUT}}$		0.6		0.7		0.9	ns
$t_{\text{PACKED}}$		0.2		0.3		0.4	ns
$t_{\text{EN}}$		0.6		0.7		0.9	ns
$t_{\text{CICO}}$		0.1		0.1		0.1	ns
$t_{\text{CGEN}}$		0.4		0.5		0.6	ns

Table 66. EPF10K50S Device LE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{CGENR}$		0.1		0.1		0.1	ns
$t_{CASC}$		0.5		0.8		1.0	ns
$t_C$		0.5		0.6		0.8	ns
$t_{CO}$		0.6		0.6		0.7	ns
$t_{COMB}$		0.3		0.4		0.5	ns
$t_{SU}$	0.5		0.6		0.7		ns
$t_H$	0.5		0.6		0.8		ns
$t_{PRE}$		0.4		0.5		0.7	ns
$t_{CLR}$		0.8		1.0		1.2	ns
$t_{CH}$	2.0		2.5		3.0		ns
$t_{CL}$	2.0		2.5		3.0		ns

Table 67. EPF10K50S Device IOE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{IOD}$		1.3		1.3		1.9	ns
$t_{IOC}$		0.3		0.4		0.4	ns
$t_{IOCO}$		1.7		2.1		2.6	ns
$t_{IOCOMB}$		0.5		0.6		0.8	ns
$t_{IOSU}$	0.8		1.0		1.3		ns
$t_{IOH}$	0.4		0.5		0.6		ns
$t_{IOCLR}$		0.2		0.2		0.4	ns
$t_{OD1}$		1.2		1.2		1.9	ns
$t_{OD2}$		0.7		0.8		1.7	ns
$t_{OD3}$		2.7		3.0		4.3	ns
$t_{XZ}$		4.7		5.7		7.5	ns
$t_{ZX1}$		4.7		5.7		7.5	ns
$t_{ZX2}$		4.2		5.3		7.3	ns
$t_{ZX3}$		6.2		7.5		9.9	ns
$t_{INREG}$		3.5		4.2		5.6	ns
$t_{IOFD}$		1.1		1.3		1.8	ns
$t_{INCOMB}$		1.1		1.3		1.8	ns

Table 69. EPF10K50S Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABAA}$		3.7		5.2		7.0	ns
$t_{EABRCCOMB}$	3.7		5.2		7.0		ns
$t_{EABRCREG}$	3.5		4.9		6.6		ns
$t_{EABWP}$	2.0		2.8		3.8		ns
$t_{EABWCCOMB}$	4.5		6.3		8.6		ns
$t_{EABWCREG}$	5.6		7.8		10.6		ns
$t_{EABDD}$		3.8		5.3		7.2	ns
$t_{EABDATACO}$		0.8		1.1		1.5	ns
$t_{EABDATASU}$	1.1		1.6		2.1		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	0.7		1.0		1.3		ns
$t_{EABWEH}$	0.4		0.6		0.8		ns
$t_{EABWDSU}$	1.2		1.7		2.2		ns
$t_{EABWDH}$	0.0		0.0		0.0		ns
$t_{EABWASU}$	1.6		2.3		3.0		ns
$t_{EABWAH}$	0.9		1.2		1.8		ns
$t_{EABWO}$		3.1		4.3		5.9	ns

Table 70. EPF10K50S Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		3.1		3.7		4.6	ns
$t_{DIN2LE}$		1.7		2.1		2.7	ns
$t_{DIN2DATA}$		2.7		3.1		5.1	ns
$t_{DCLK2IOE}$		1.6		1.9		2.6	ns
$t_{DCLK2LE}$		1.7		2.1		2.7	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		1.5		1.7		2.4	ns
$t_{SAMECOLUMN}$		1.0		1.3		2.1	ns
$t_{DIFFROW}$		2.5		3.0		4.5	ns
$t_{TWOROWS}$		4.0		4.7		6.9	ns
$t_{LEPERIPH}$		2.6		2.9		3.4	ns
$t_{LABCARRY}$		0.1		0.2		0.2	ns
$t_{LABCASC}$		0.8		1.0		1.3	ns

## Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the Altera Digital Library for pin-out information.

## Revision History

The information contained in the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.5 supersedes information published in previous versions.

### Version 2.5

The following changes were made to the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.5:

- *Note (1)* added to **Figure 23**.
- Text added to “**I/O Element**” section on **page 34**.
- Updated **Table 22**.

### Version 2.4

The following changes were made to the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.4: updated text on **page 34** and **page 63**.