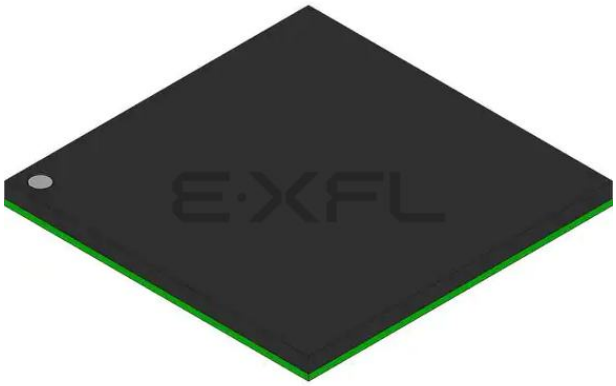
# Altera - EPF10K50SFC256-1X Datasheet



**Welcome to E-XFL.COM**

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 360 |
| Number of Logic Elements/Cells | 2880 |
| Total RAM Bits | 40960 |
| Number of I/O | 191 |
| Number of Gates | 199000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 256-BGA |
| Supplier Device Package | 256-FBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=epf10k50sfc256-1x |

*Table 4. FLEX 10KE Package Sizes*

| Device | 144-Pin TQFP | 208-Pin PQFP | 240-Pin PQFP RQFP | 256-Pin FineLine BGA | 356-Pin BGA | 484-Pin FineLine BGA | 599-Pin PGA | 600-Pin BGA | 672-Pin FineLine BGA |
|---|---|---|---|---|---|---|---|---|---|
| Pitch (mm) | 0.50 | 0.50 | 0.50 | 1.0 | 1.27 | 1.0 | – | 1.27 | 1.0 |
| Area ($mm^2$) | 484 | 936 | 1,197 | 289 | 1,225 | 529 | 3,904 | 2,025 | 729 |
| Length × width (mm × mm) | 22 × 22 | 30.6 × 30.6 | 34.6 × 34.6 | 17 × 17 | 35 × 35 | 23 × 23 | 62.5 × 62.5 | 45 × 45 | 27 × 27 |

## General Description

Altera FLEX 10KE devices are enhanced versions of FLEX 10K devices. Based on reconfigurable CMOS SRAM elements, the FLEX architecture incorporates all features necessary to implement common gate array megafunctions. With up to 200,000 typical gates, FLEX 10KE devices provide the density, speed, and features to integrate entire systems, including multiple 32-bit buses, into a single device.

The ability to reconfigure FLEX 10KE devices enables 100% testing prior to shipment and allows the designer to focus on simulation and design verification. FLEX 10KE reconfigurability eliminates inventory management for gate array designs and generation of test vectors for fault coverage.

Table 5 shows FLEX 10KE performance for some common designs. All performance values were obtained with Synopsys DesignWare or LPM functions. Special design techniques are not required to implement the applications; the designer simply infers or instantiates a function in a Verilog HDL, VHDL, Altera Hardware Description Language (AHDL), or schematic design file.

*Table 5. FLEX 10KE Performance*

| Application | Resources Used | | Performance | | | Units |
|---|---|---|---|---|---|---|
| | LEs | EABs | -1 Speed Grade | -2 Speed Grade | -3 Speed Grade | |
| 16-bit loadable counter | 16 | 0 | 285 | 250 | 200 | MHz |
| 16-bit accumulator | 16 | 0 | 285 | 250 | 200 | MHz |
| 16-to-1 multiplexer *(1)* | 10 | 0 | 3.5 | 4.9 | 7.0 | ns |
| 16-bit multiplier with 3-stage pipeline *(2)* | 592 | 0 | 156 | 131 | 93 | MHz |
| 256 × 16 RAM read cycle speed *(2)* | 0 | 1 | 196 | 154 | 118 | MHz |
| 256 × 16 RAM write cycle speed *(2)* | 0 | 1 | 185 | 143 | 106 | MHz |

***Notes:***
(1) This application uses combinatorial inputs and outputs.
(2) This application uses registered inputs and outputs.

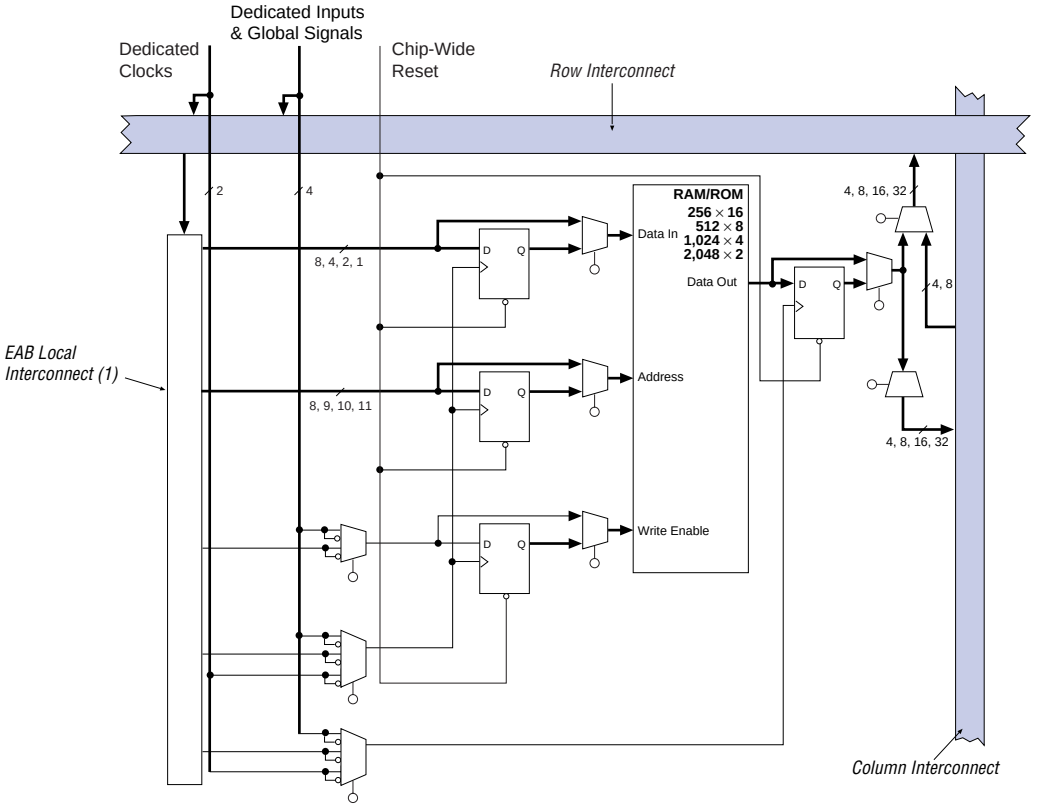
Table 6 shows FLEX 10KE performance for more complex designs. These designs are available as Altera MegaCore® functions.

*Table 6. FLEX 10KE Performance for Complex Designs*

| Application | LEs Used | Performance | | | Units |
|---|---|---|---|---|---|
| | | -1 Speed Grade | -2 Speed Grade | -3 Speed Grade | |
| 8-bit, 16-tap parallel finite impulse response (FIR) filter | 597 | 192 | 156 | 116 | MSPS |
| 8-bit, 512-point fast Fourier transform (FFT) function | 1,854 | 23.4 | 28.7 | 38.9 | µs *(1)* |
| | | 113 | 92 | 68 | MHz |
| a16450 universal asynchronous receiver/transmitter (UART) | 342 | 36 | 28 | 20.5 | MHz |

***Note:***
(1) These values are for calculation time. Calculation time = number of clocks required / $f_{max}$. Number of clocks required = ceiling [log 2 (points) / 2] × [points +14 + ceiling]

*Figure 4. FLEX 10KE Device in Single-Port RAM Mode*




***Note:***

(1) EPF10K30E, EPF10K50E, and EPF10K50S devices have 88 EAB local interconnect channels; EPF10K100E, EPF10K130E, EPF10K200E, and EPF10K200S devices have 104 EAB local interconnect channels.

EABs can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the write enable signal. In contrast, the EAB's synchronous RAM generates its own write enable signal and is self-timed with respect to the input or write clock. A circuit using the EAB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

### *LE Operating Modes*

The FLEX 10KE LE can operate in the following four modes:

- Normal mode
- Arithmetic mode
- Up / down counter mode
- Clearable counter mode

Each of these modes uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. Three inputs to the LE provide clock, clear, and preset control for the register. The Altera software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that use a specific LE operating mode for optimal performance.

The architecture provides a synchronous clock enable to the register in all four modes. The Altera software can set DATA1 to enable the register synchronously, providing easy implementation of fully synchronous designs.

### *Column-to-IOE Connections*

When an IOE is used as an input, it can drive up to two separate column channels. When an IOE is used as an output, the signal is driven by a multiplexer that selects a signal from the column channels. Two IOEs connect to each side of the column channels. Each IOE can be driven by column channels via a multiplexer. The set of column channels is different for each IOE (see Figure 17).

***Figure 17. FLEX 10KE Column-to-IOE Connections***

*The values for m and n are provided in Table 11.*

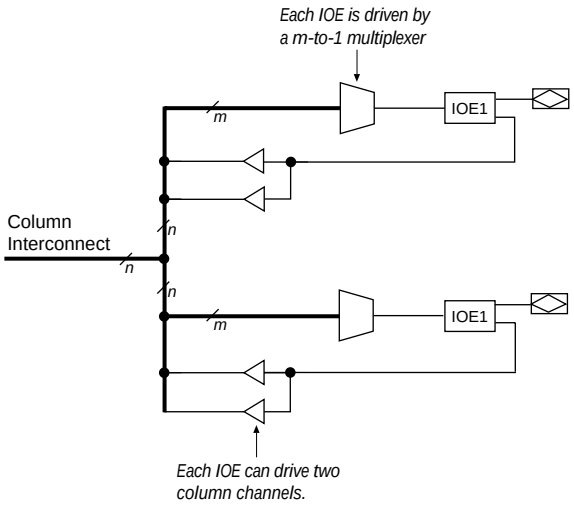



Table 11 lists the FLEX 10KE column-to-IOE interconnect resources.

***Table 11. FLEX 10KE Column-to-IOE Interconnect Resources***

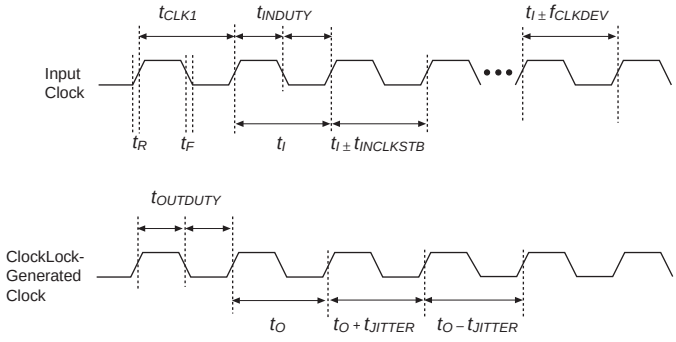
| Device | Channels per Column *(n)* | Column Channels per Pin *(m)* |
|---|---|---|
| EPF10K30E | 24 | 16 |
| EPF10K50E<br>EPF10K50S | 24 | 16 |
| EPF10K100E | 24 | 16 |
| EPF10K130E | 32 | 24 |
| EPF10K200E<br>EPF10K200S | 48 | 40 |

## ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. Figure 19 shows the incoming and generated clock specifications.

***Figure 19. Specifications for Incoming & Generated Clocks***

*The $t_I$ parameter refers to the nominal input clock period; the $t_O$ parameter refers to the nominal output clock period.*



## PCI Pull-Up Clamping Diode Option

FLEX 10KE devices have a pull-up clamping diode on every I/O, dedicated input, and dedicated clock pin. PCI clamping diodes clamp the signal to the $V_{CCIO}$ value and are required for 3.3-V PCI compliance. Clamping diodes can also be used to limit overshoot in other systems.

Clamping diodes are controlled on a pin-by-pin basis. When $V_{CCIO}$ is 3.3 V, a pin that has the clamping diode option turned on can be driven by a 2.5-V or 3.3-V signal, but not a 5.0-V signal. When $V_{CCIO}$ is 2.5 V, a pin that has the clamping diode option turned on can be driven by a 2.5-V signal, but not a 3.3-V or 5.0-V signal. Additionally, a clamping diode can be activated for a subset of pins, which would allow a device to bridge between a 3.3-V PCI bus and a 5.0-V device.

## Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces system noise and adds a maximum delay of 4.3 ns. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate pin-by-pin or assign a default slew rate to all pins on a device-wide basis. The slow slew rate setting affects the falling edge of the output.

## Open-Drain Output Option

FLEX 10KE devices provide an optional open-drain output (electrically equivalent to open-collector output) for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

## MultiVolt I/O Interface

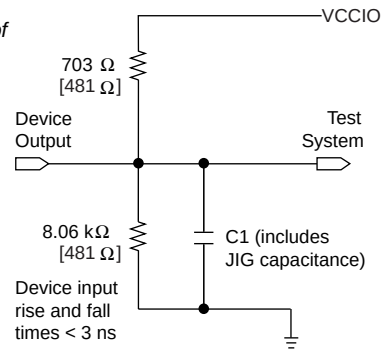
The FLEX 10KE device architecture supports the MultiVolt I/O interface feature, which allows FLEX 10KE devices in all packages to interface with systems of differing supply voltages. These devices have one set of $V_{CC}$ pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

## Generic Testing

Each FLEX 10KE device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for FLEX 10KE devices are made under conditions equivalent to those shown in Figure 21. Multiple test patterns can be used to configure devices during all stages of the production flow.

***Figure 21. FLEX 10KE AC Test Conditions***

*Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V devices or outputs. Numbers without brackets are for 3.3-V. devices or outputs.*



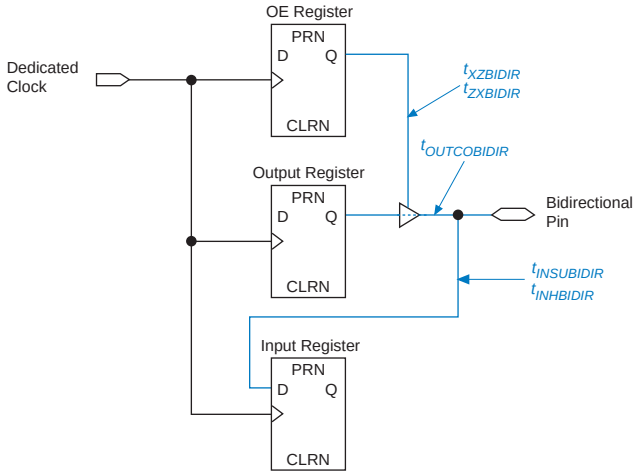

## Operating Conditions

Tables 19 through 23 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V FLEX 10KE devices.

***Table 19. FLEX 10KE 2.5-V Device Absolute Maximum Ratings*** *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage | With respect to ground *(2)* | –0.5 | 3.6 | V |
| $V_{CCIO}$ | | | –0.5 | 4.6 | V |
| $V_I$ | DC input voltage | | –2.0 | 5.75 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | PQFP, TQFP, BGA, and FineLine BGA packages, under bias | | 135 | ° C |
| | | Ceramic PGA packages, under bias | | 150 | ° C |

*Figure 28. Synchronous Bidirectional Pin External Timing Model*




Tables 24 through 28 describe the FLEX 10KE device internal timing parameters. Tables 29 through 30 describe the FLEX 10KE external timing parameters and their symbols.

*Table 24. LE Timing Microparameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | Condition |
|---|---|---|
| $t_{LUT}$ | LUT delay for data-in | |
| $t_{CLUT}$ | LUT delay for carry-in | |
| $t_{RLUT}$ | LUT delay for LE register feedback | |
| $t_{PACKED}$ | Data-in to packed register delay | |
| $t_{EN}$ | LE register enable delay | |
| $t_{CICO}$ | Carry-in to carry-out delay | |
| $t_{CGEN}$ | Data-in to carry-out delay | |
| $t_{CGENR}$ | LE register feedback to carry-out delay | |
| $t_{CASC}$ | Cascade-in to cascade-out delay | |
| $t_{C}$ | LE register control signal delay | |
| $t_{CO}$ | LE register clock-to-output delay | |
| $t_{COMB}$ | Combinatorial delay | |
| $t_{SU}$ | LE register setup time for data and enable signals before clock; LE register recovery time after asynchronous clear, preset, or load | |
| $t_{H}$ | LE register hold time for data and enable signals after clock | |
| $t_{PRE}$ | LE register preset delay | |

Figures 29 and 30 show the asynchronous and synchronous timing waveforms, respectively, or the EAB macroparameters in Tables 26 and 27.

*Figure 29. EAB Asynchronous Timing Waveforms*

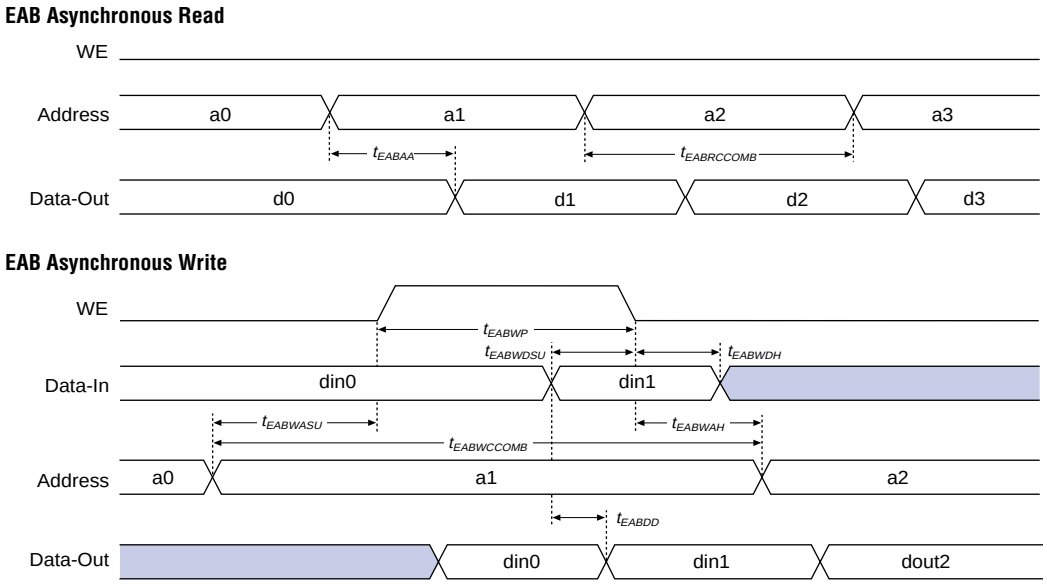


**Table 38. EPF10K50E Device LE Timing Microparameters (Part 2 of 2)** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{H}$ | 0.9 | | 1.0 | | 1.4 | | ns |
| $t_{PRE}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{CLR}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 3.0 | | ns |

**Table 39. EPF10K50E Device IOE Timing Microparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 2.2 | | 2.4 | | 3.3 | ns |
| $t_{IOC}$ | | 0.3 | | 0.3 | | 0.5 | ns |
| $t_{IOCO}$ | | 1.0 | | 1.0 | | 1.4 | ns |
| $t_{IOCOMB}$ | | 0.0 | | 0.0 | | 0.2 | ns |
| $t_{IOSU}$ | 1.0 | | 1.2 | | 1.7 | | ns |
| $t_{IOH}$ | 0.3 | | 0.3 | | 0.5 | | ns |
| $t_{IOCLR}$ | | 0.9 | | 1.0 | | 1.4 | ns |
| $t_{OD1}$ | | 0.8 | | 0.9 | | 1.2 | ns |
| $t_{OD2}$ | | 0.3 | | 0.4 | | 0.7 | ns |
| $t_{OD3}$ | | 3.0 | | 3.5 | | 3.5 | ns |
| $t_{XZ}$ | | 1.4 | | 1.7 | | 2.3 | ns |
| $t_{ZX1}$ | | 1.4 | | 1.7 | | 2.3 | ns |
| $t_{ZX2}$ | | 0.9 | | 1.2 | | 1.8 | ns |
| $t_{ZX3}$ | | 3.6 | | 4.3 | | 4.6 | ns |
| $t_{INREG}$ | | 4.9 | | 5.8 | | 7.8 | ns |
| $t_{IOFD}$ | | 2.8 | | 3.3 | | 4.5 | ns |
| $t_{INCOMB}$ | | 2.8 | | 3.3 | | 4.5 | ns |

*Table 40. EPF10K50E Device EAB Internal Microparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 1.7 | | 2.0 | | 2.7 | ns |
| $t_{EABDATA1}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{EABWE1}$ | | 1.1 | | 1.3 | | 1.8 | ns |
| $t_{EABWE2}$ | | 0.4 | | 0.4 | | 0.6 | ns |
| $t_{EABRE1}$ | | 0.8 | | 0.9 | | 1.2 | ns |
| $t_{EABRE2}$ | | 0.4 | | 0.4 | | 0.6 | ns |
| $t_{EABCLK}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCO}$ | | 0.3 | | 0.3 | | 0.5 | ns |
| $t_{EABBYPASS}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{EABSU}$ | 0.9 | | 1.0 | | 1.4 | | ns |
| $t_{EABH}$ | 0.4 | | 0.4 | | 0.6 | | ns |
| $t_{EABCLR}$ | 0.3 | | 0.3 | | 0.5 | | ns |
| $t_{AA}$ | | 3.2 | | 3.8 | | 5.1 | ns |
| $t_{WP}$ | 2.5 | | 2.9 | | 3.9 | | ns |
| $t_{RP}$ | 0.9 | | 1.1 | | 1.5 | | ns |
| $t_{WDSU}$ | 0.9 | | 1.0 | | 1.4 | | ns |
| $t_{WDH}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{WASU}$ | 1.7 | | 2.0 | | 2.7 | | ns |
| $t_{WAH}$ | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RASU}$ | 3.1 | | 3.7 | | 5.0 | | ns |
| $t_{RAH}$ | 0.2 | | 0.2 | | 0.3 | | ns |
| $t_{WO}$ | | 2.5 | | 2.9 | | 3.9 | ns |
| $t_{DD}$ | | 2.5 | | 2.9 | | 3.9 | ns |
| $t_{EABOUT}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{EABCH}$ | 1.5 | | 2.0 | | 2.5 | | ns |
| $t_{EABCL}$ | 2.5 | | 2.9 | | 3.9 | | ns |

**Table 41. EPF10K50E Device EAB Internal Timing Macroparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABAA}$ | | 6.4 | | 7.6 | | 10.2 | ns |
| $t_{EABRCOMB}$ | 6.4 | | 7.6 | | 10.2 | | ns |
| $t_{EABRCREG}$ | 4.4 | | 5.1 | | 7.0 | | ns |
| $t_{EABWP}$ | 2.5 | | 2.9 | | 3.9 | | ns |
| $t_{EABWCOMB}$ | 6.0 | | 7.0 | | 9.5 | | ns |
| $t_{EABWCREG}$ | 6.8 | | 7.8 | | 10.6 | | ns |
| $t_{EABDD}$ | | 5.7 | | 6.7 | | 9.0 | ns |
| $t_{EABDATACO}$ | | 0.8 | | 0.9 | | 1.3 | ns |
| $t_{EABDATASU}$ | 1.5 | | 1.7 | | 2.3 | | ns |
| $t_{EABDATAH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWESU}$ | 1.3 | | 1.4 | | 2.0 | | ns |
| $t_{EABWEH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWDSU}$ | 1.5 | | 1.7 | | 2.3 | | ns |
| $t_{EABWDH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWASU}$ | 3.0 | | 3.6 | | 4.8 | | ns |
| $t_{EABWAH}$ | 0.5 | | 0.5 | | 0.8 | | ns |
| $t_{EABWO}$ | | 5.1 | | 6.0 | | 8.1 | ns |

**Table 42. EPF10K50E Device Interconnect Timing Microparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DIN2IOE}$ | | 3.5 | | 4.3 | | 5.6 | ns |
| $t_{DIN2LE}$ | | 2.1 | | 2.5 | | 3.4 | ns |
| $t_{DIN2DATA}$ | | 2.2 | | 2.4 | | 3.1 | ns |
| $t_{DCLK2IOE}$ | | 2.9 | | 3.5 | | 4.7 | ns |
| $t_{DCLK2LE}$ | | 2.1 | | 2.5 | | 3.4 | ns |
| $t_{SAMELAB}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{SAMEROW}$ | | 1.1 | | 1.1 | | 1.5 | ns |
| $t_{SAMECOLUMN}$ | | 0.8 | | 1.0 | | 1.3 | ns |
| $t_{DIFFROW}$ | | 1.9 | | 2.1 | | 2.8 | ns |
| $t_{TWOROWS}$ | | 3.0 | | 3.2 | | 4.3 | ns |
| $t_{LEPERIPH}$ | | 3.1 | | 3.3 | | 3.7 | ns |
| $t_{LABCARRY}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{LABCASC}$ | | 0.3 | | 0.3 | | 0.5 | ns |

| Table 58. EPF10K130E External Bidirectional Timing Parameters Notes (1), (2) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ (3) | 2.2 | | 2.4 | | 3.2 | | ns |
| $t_{INHBIDIR}$ (3) | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSUBIDIR}$ (4) | 2.8 | | 3.0 | | – | | ns |
| $t_{INHBIDIR}$ (4) | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCOBIDIR}$ (3) | 2.0 | 5.0 | 2.0 | 7.0 | 2.0 | 9.2 | ns |
| $t_{XZBIDIR}$ (3) | | 5.6 | | 8.1 | | 10.8 | ns |
| $t_{ZXBIDIR}$ (3) | | 5.6 | | 8.1 | | 10.8 | ns |
| $t_{OUTCOBIDIR}$ (4) | 0.5 | 4.0 | 0.5 | 6.0 | – | – | ns |
| $t_{XZBIDIR}$ (4) | | 4.6 | | 7.1 | | – | ns |
| $t_{ZXBIDIR}$ (4) | | 4.6 | | 7.1 | | – | ns |

***Notes to tables:***

(1) All timing parameters are described in Tables 24 through 30 in this data sheet.
(2) These parameters are specified by characterization.
(3) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 59 through 65 show EPF10K200E device internal and external timing parameters.

| Table 59. EPF10K200E Device LE Timing Microparameters (Part 1 of 2) Note (1) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 0.7 | | 0.8 | | 1.2 | ns |
| $t_{CLUT}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{RLUT}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{PACKED}$ | | 0.3 | | 0.5 | | 0.7 | ns |
| $t_{EN}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{CICO}$ | | 0.2 | | 0.2 | | 0.3 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.4 | | 0.6 | ns |
| $t_{CGENR}$ | | 0.2 | | 0.2 | | 0.3 | ns |
| $t_{CASC}$ | | 0.7 | | 0.8 | | 1.2 | ns |
| $t_{C}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{CO}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{COMB}$ | | 0.4 | | 0.6 | | 0.8 | ns |
| $t_{SU}$ | 0.4 | | 0.6 | | 0.7 | | ns |

*Table 68. EPF10K50S Device EAB Internal Microparameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 1.7 | | 2.4 | | 3.2 | ns |
| $t_{EABDATA2}$ | | 0.4 | | 0.6 | | 0.8 | ns |
| $t_{EABWE1}$ | | 1.0 | | 1.4 | | 1.9 | ns |
| $t_{EABWE2}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABRE1}$ | | 0.0 | | 0.0 | | 0.0 | |
| $t_{EABRE2}$ | | 0.4 | | 0.6 | | 0.8 | |
| $t_{EABCLK}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCO}$ | | 0.8 | | 1.1 | | 1.5 | ns |
| $t_{EABBYPASS}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABSU}$ | 0.7 | | 1.0 | | 1.3 | | ns |
| $t_{EABH}$ | 0.4 | | 0.6 | | 0.8 | | ns |
| $t_{EABCLR}$ | 0.8 | | 1.1 | | 1.5 | | |
| $t_{AA}$ | | 2.0 | | 2.8 | | 3.8 | ns |
| $t_{WP}$ | 2.0 | | 2.8 | | 3.8 | | ns |
| $t_{RP}$ | 1.0 | | 1.4 | | 1.9 | | |
| $t_{WDSU}$ | 0.5 | | 0.7 | | 0.9 | | ns |
| $t_{WDH}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{WASU}$ | 1.0 | | 1.4 | | 1.9 | | ns |
| $t_{WAH}$ | 1.5 | | 2.1 | | 2.9 | | ns |
| $t_{RASU}$ | 1.5 | | 2.1 | | 2.8 | | |
| $t_{RAH}$ | 0.1 | | 0.1 | | 0.2 | | |
| $t_{WO}$ | | 2.1 | | 2.9 | | 4.0 | ns |
| $t_{DD}$ | | 2.1 | | 2.9 | | 4.0 | ns |
| $t_{EABOUT}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCH}$ | 1.5 | | 2.0 | | 2.5 | | ns |
| $t_{EABCL}$ | 1.5 | | 2.0 | | 2.5 | | ns |

*Table 71. EPF10K50S External Timing Parameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 8.0 | | 9.5 | | 12.5 | ns |
| $t_{INSU}$ *(2)* | 2.4 | | 2.9 | | 3.9 | | ns |
| $t_{INH}$ *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(2)* | 2.0 | 4.3 | 2.0 | 5.2 | 2.0 | 7.3 | ns |
| $t_{INSU}$ *(3)* | 2.4 | | 2.9 | | | | ns |
| $t_{INH}$ *(3)* | 0.0 | | 0.0 | | | | ns |
| $t_{OUTCO}$ *(3)* | 0.5 | 3.3 | 0.5 | 4.1 | | | ns |
| $t_{PCISU}$ | 2.4 | | 2.9 | | – | | ns |
| $t_{PCIH}$ | 0.0 | | 0.0 | | – | | ns |
| $t_{PCICO}$ | 2.0 | 6.0 | 2.0 | 7.7 | – | – | ns |

*Table 72. EPF10K50S External Bidirectional Timing Parameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ *(2)* | 2.7 | | 3.2 | | 4.3 | | ns |
| $t_{INHBIDIR}$ *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INHBIDIR}$ *(3)* | 0.0 | | 0.0 | | – | | ns |
| $t_{INSUBIDIR}$ *(3)* | 3.7 | | 4.2 | | – | | ns |
| $t_{OUTCOBIDIR}$ *(2)* | 2.0 | 4.5 | 2.0 | 5.2 | 2.0 | 7.3 | ns |
| $t_{XZBIDIR}$ *(2)* | | 6.8 | | 7.8 | | 10.1 | ns |
| $t_{ZXBIDIR}$ *(2)* | | 6.8 | | 7.8 | | 10.1 | ns |
| $t_{OUTCOBIDIR}$ *(3)* | 0.5 | 3.5 | 0.5 | 4.2 | – | – | |
| $t_{XZBIDIR}$ *(3)* | | 6.8 | | 8.4 | | – | ns |
| $t_{ZXBIDIR}$ *(3)* | | 6.8 | | 8.4 | | – | ns |

***Notes to tables:***

(1) All timing parameters are described in Tables 24 through 30.
(2) This parameter is measured without use of the ClockLock or ClockBoost circuits.
(3) This parameter is measured with use of the ClockLock or ClockBoost circuits

*Table 73. EPF10K200S Device Internal & External Timing Parameters* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 0.7 | | 0.8 | | 1.2 | ns |
| $t_{CLUT}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{RLUT}$ | | 0.5 | | 0.7 | | 0.9 | ns |
| $t_{PACKED}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{EN}$ | | 0.6 | | 0.5 | | 0.6 | ns |
| $t_{CICO}$ | | 0.1 | | 0.2 | | 0.3 | ns |
| $t_{CGEN}$ | | 0.3 | | 0.4 | | 0.6 | ns |
| $t_{CGENR}$ | | 0.1 | | 0.2 | | 0.3 | ns |
| $t_{CASC}$ | | 0.7 | | 0.8 | | 1.2 | ns |
| $t_{C}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{CO}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{COMB}$ | | 0.3 | | 0.6 | | 0.8 | ns |
| $t_{SU}$ | 0.4 | | 0.6 | | 0.7 | | ns |
| $t_{H}$ | 1.0 | | 1.1 | | 1.5 | | ns |
| $t_{PRE}$ | | 0.4 | | 0.6 | | 0.8 | ns |
| $t_{CLR}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 3.0 | | ns |

*Table 74. EPF10K200S Device IOE Timing Microparameters (Part 1 of 2)* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 1.8 | | 1.9 | | 2.6 | ns |
| $t_{IOC}$ | | 0.3 | | 0.3 | | 0.5 | ns |
| $t_{IOCO}$ | | 1.7 | | 1.9 | | 2.6 | ns |
| $t_{IOCOMB}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{IOSU}$ | 0.8 | | 0.9 | | 1.2 | | ns |
| $t_{IOH}$ | 0.4 | | 0.8 | | 1.1 | | ns |
| $t_{IOCLR}$ | | 0.2 | | 0.2 | | 0.3 | ns |
| $t_{OD1}$ | | 1.3 | | 0.7 | | 0.9 | ns |
| $t_{OD2}$ | | 0.8 | | 0.2 | | 0.4 | ns |
| $t_{OD3}$ | | 2.9 | | 3.0 | | 3.9 | ns |
| $t_{XZ}$ | | 5.0 | | 5.3 | | 7.1 | ns |
| $t_{ZX1}$ | | 5.0 | | 5.3 | | 7.1 | ns |

During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

SRAM configuration elements allow FLEX 10KE devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 85 ms and can be used to reconfigure an entire system dynamically. In-field upgrades can be performed by distributing new configuration files.

Before and during configuration, all I/O pins (except dedicated inputs, clock, or configuration pins) are pulled high by a weak pull-up resistor.

## Programming Files

Despite being function- and pin-compatible, FLEX 10KE devices are not programming- or configuration file-compatible with FLEX 10K or FLEX 10KA devices. A design therefore must be recompiled before it is transferred from a FLEX 10K or FLEX 10KA device to an equivalent FLEX 10KE device. This recompilation should be performed both to create a new programming or configuration file and to check design timing in FLEX 10KE devices, which has different timing characteristics than FLEX 10K or FLEX 10KA devices.

FLEX 10KE devices are generally pin-compatible with equivalent FLEX 10KA devices. In some cases, FLEX 10KE devices have fewer I/O pins than the equivalent FLEX 10KA devices. Table 81 shows which FLEX 10KE devices have fewer I/O pins than equivalent FLEX 10KA devices. However, power, ground, JTAG, and configuration pins are the same on FLEX 10KA and FLEX 10KE devices, enabling migration from a FLEX 10KA design to a FLEX 10KE design.

## Device Pin-Outs

See the Altera web site (**http://www.altera.com**) or the Altera Digital Library for pin-out information.

## Revision History

The information contained in the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.5 supersedes information published in previous versions.

### Version 2.5

The following changes were made to the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.5:

- *Note (1)* added to Figure 23.
- Text added to "I/O Element" section on page 34.
- Updated Table 22.

### Version 2.4

The following changes were made to the *FLEX 10KE Embedded Programmable Logic Data Sheet* version 2.4: updated text on page 34 and page 63.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com
Applications Hotline:
(800) 800-EPLD
Literature Services:
lit_req@altera.com