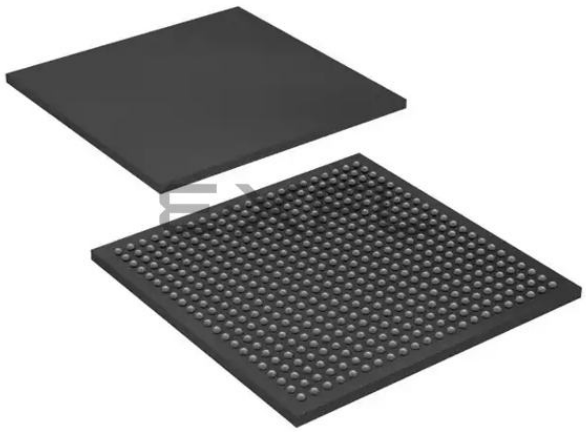


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	360
Number of Logic Elements/Cells	2880
Total RAM Bits	40960
Number of I/O	220
Number of Gates	199000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k50sfc484-1

For more information on FLEX device configuration, see the following documents:

- *Configuration Devices for APEX & FLEX Devices Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *MasterBlaster Download Cable Data Sheet*
- *Application Note 116 (Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices)*

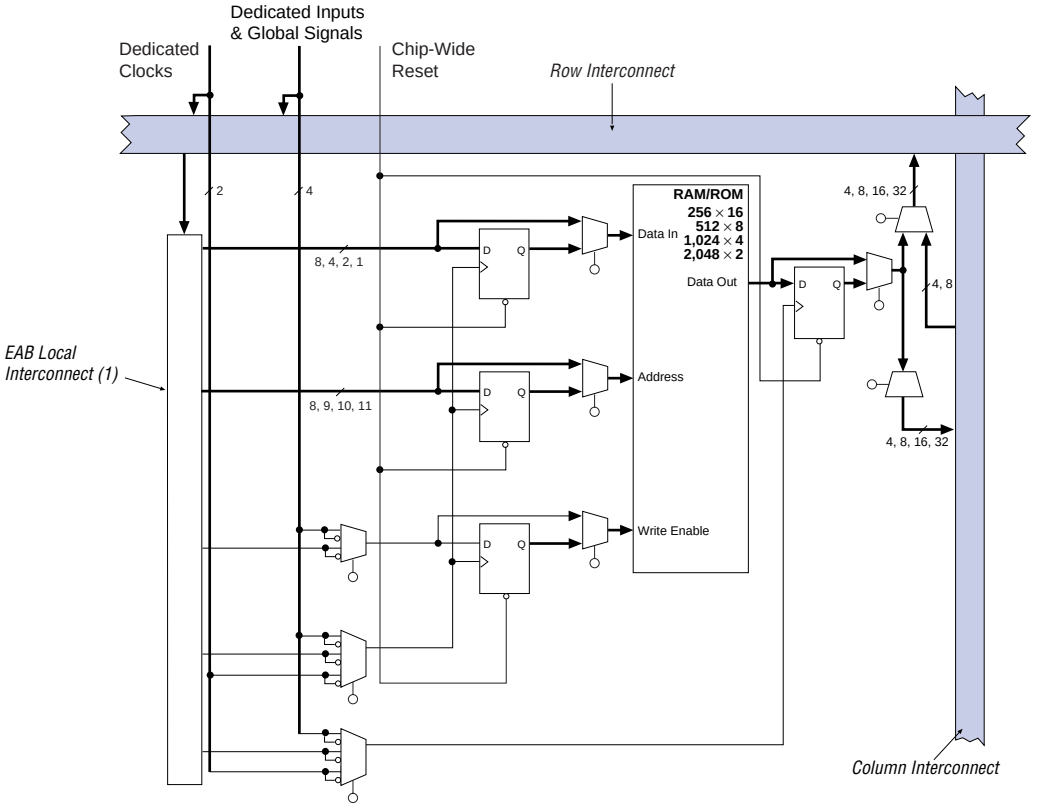
FLEX 10KE devices are supported by the Altera development systems, which are integrated packages that offer schematic, text (including AHDL), and waveform design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, and device configuration. The Altera software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools.

The Altera software works easily with common gate array EDA tools for synthesis and simulation. For example, the Altera software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the Altera software contains EDA libraries that use device-specific features such as carry chains, which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the Altera development system includes DesignWare functions that are optimized for the FLEX 10KE architecture.

The Altera development system runs on Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800.

See the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet* for more information.

Figure 4. FLEX 10KE Device in Single-Port RAM Mode



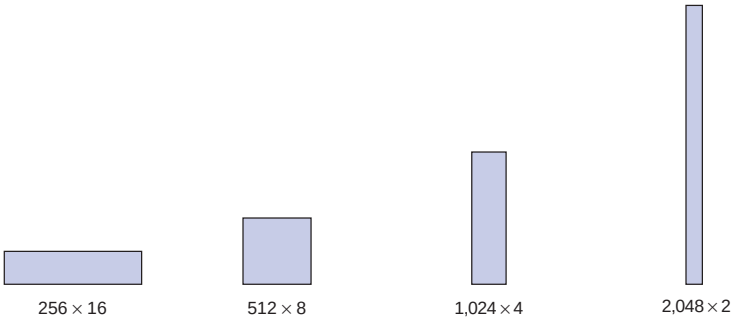
Note:

(1) EPF10K30E, EPF10K50E, and EPF10K50S devices have 88 EAB local interconnect channels; EPF10K100E, EPF10K130E, EPF10K200E, and EPF10K200S devices have 104 EAB local interconnect channels.

EABs can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the write enable signal. In contrast, the EAB's synchronous RAM generates its own write enable signal and is self-timed with respect to the input or write clock. A circuit using the EAB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

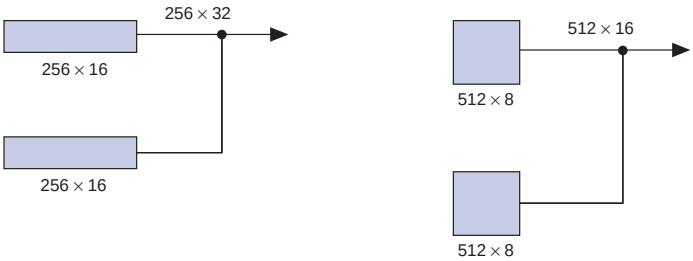
When used as RAM, each EAB can be configured in any of the following sizes: 256 × 16, 512 × 8, 1,024 × 4, or 2,048 × 2 (see Figure 5).

Figure 5. FLEX 10KE EAB Memory Configurations



Larger blocks of RAM are created by combining multiple EABs. For example, two 256 × 16 RAM blocks can be combined to form a 256 × 32 block; two 512 × 8 RAM blocks can be combined to form a 512 × 16 block (see Figure 6).

Figure 6. Examples of Combining FLEX 10KE EABs



If necessary, all EABs in a device can be cascaded to form a single RAM block. EABs can be cascaded to form RAM blocks of up to 2,048 words without impacting timing. The Altera software automatically combines EABs to meet a designer's RAM specifications.

EABs provide flexible options for driving and controlling clock signals. Different clocks and clock enables can be used for reading and writing to the EAB. Registers can be independently inserted on the data input, EAB output, write address, write enable signals, read address, and read enable signals. The global signals and the EAB local interconnect can drive write enable, read enable, and clock enable signals. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control write enable, read enable, clear, clock, and clock enable signals.

An EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs (see Figures 2 and 4). The column interconnect, which is adjacent to the EAB, has twice as many channels as other columns in the device.

Logic Array Block

An LAB consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure to the FLEX 10KE architecture, facilitating efficient routing with optimum device utilization and high performance (see Figure 7).

Each LAB provides four control signals with programmable inversion that can be used in all eight LEs. Two of these signals can be used as clocks, the other two can be used for clear / preset control. The LAB clocks can be driven by the dedicated clock input pins, global signals, I / O signals, or internal signals via the LAB local interconnect. The LAB preset and clear control signals can be driven by the global signals, I / O signals, or internal signals via the LAB local interconnect. The global control signals are typically used for global clock, clear, or preset signals because they provide asynchronous control with very low skew across the device. If logic is required on a control signal, it can be generated in one or more LE in any LAB and driven into the local interconnect of the target LAB. In addition, the global control signals can be generated from LE outputs.

Logic Element

The LE, the smallest unit of logic in the FLEX 10KE architecture, has a compact size that provides efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can quickly compute any function of four variables. In addition, each LE contains a programmable flipflop with a synchronous clock enable, a carry chain, and a cascade chain. Each LE drives both the local and the FastTrack Interconnect routing structure (see Figure 8).

Figure 8. FLEX 10KE Logic Element

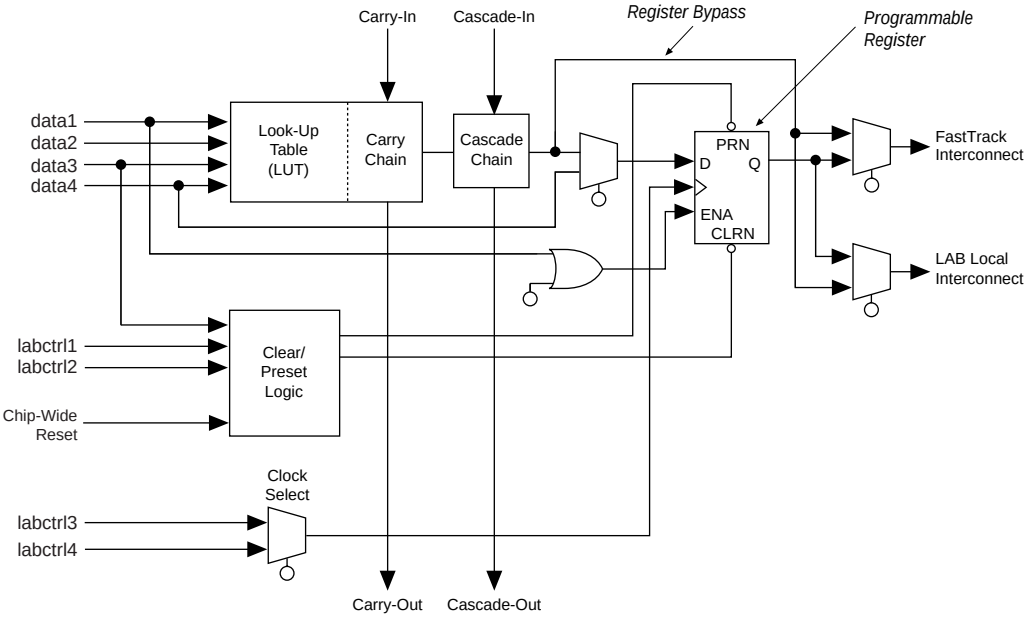
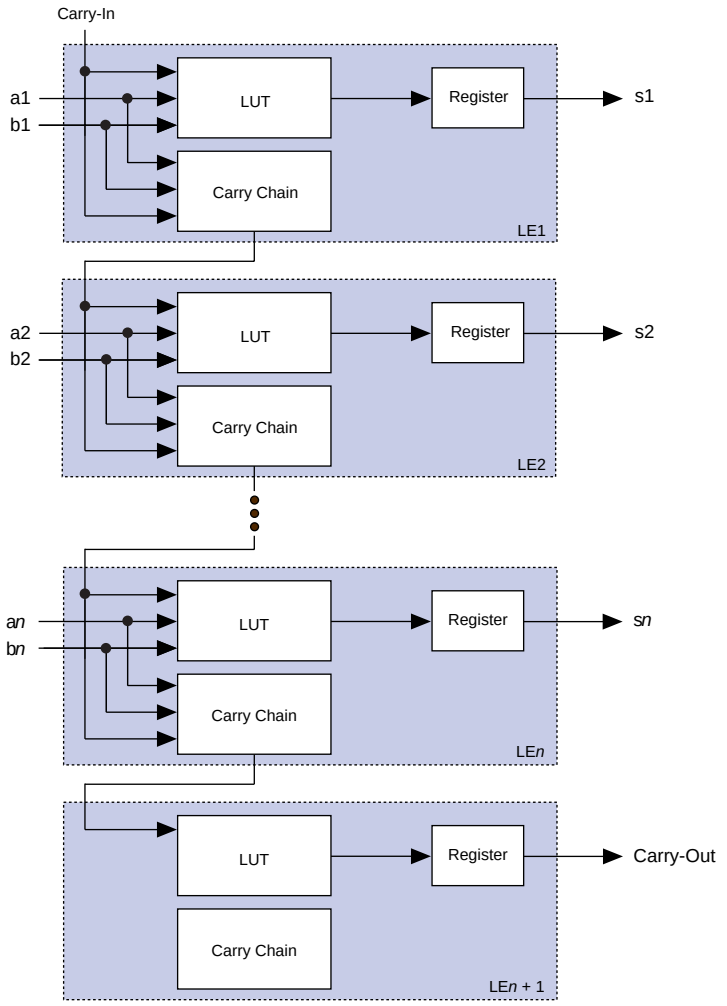


Figure 9 shows how an *n*-bit full adder can be implemented in *n* + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for an accumulator function. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal.

Figure 9. FLEX 10KE Carry Chain Operation (n-Bit Full Adder)



For improved routing, the row interconnect consists of a combination of full-length and half-length channels. The full-length channels connect to all LABs in a row; the half-length channels connect to the LABs in half of the row. The EAB can be driven by the half-length channels in the left half of the row and by the full-length channels. The EAB drives out to the full-length channels. In addition to providing a predictable, row-wide interconnect, this architecture provides increased routing resources. Two neighboring LABs can be connected using a half-row channel, thereby saving the other half of the channel for the other half of the row.

Table 7 summarizes the FastTrack Interconnect routing structure resources available in each FLEX 10KE device.

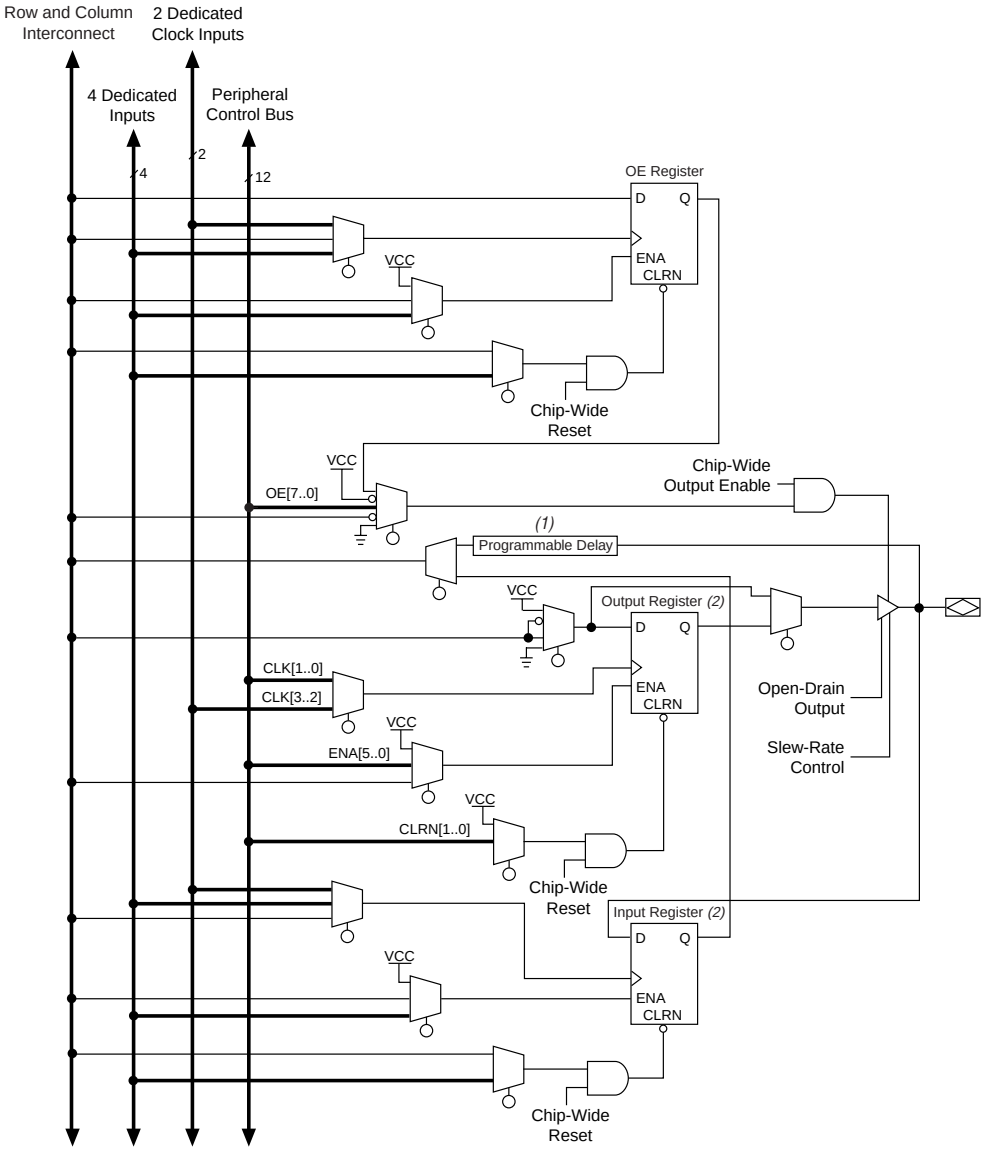
Table 7. FLEX 10KE FastTrack Interconnect Resources

Device	Rows	Channels per Row	Columns	Channels per Column
EPF10K30E	6	216	36	24
EPF10K50E EPF10K50S	10	216	36	24
EPF10K100E	12	312	52	24
EPF10K130E	16	312	52	32
EPF10K200E EPF10K200S	24	312	52	48

In addition to general-purpose I/O pins, FLEX 10KE devices have six dedicated input pins that provide low-skew signal distribution across the device. These six inputs can be used for global clock, clear, preset, and peripheral output enable and clock enable control signals. These signals are available as control signals for all LABs and IOEs in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device.

Figure 14 shows the interconnection of adjacent LABs and EABs, with row, column, and local interconnects, as well as the associated cascade and carry chains. Each LAB is labeled according to its location: a letter represents the row and a number represents the column. For example, LAB B3 is in row B, column 3.

Figure 15. FLEX 10KE Bidirectional I/O Registers



Note:

(1) All FLEX 10KE devices (except the EPF10K50E and EPF10K200E devices) have a programmable input delay buffer on the input path.

Tables 12 and 13 summarize the ClockLock and ClockBoost parameters for -1 and -2 speed-grade devices, respectively.

Table 12. ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_R	Input rise time				5	ns
t_F	Input fall time				5	ns
t_{INDUTY}	Input duty cycle		40		60	%
f_{CLK1}	Input clock frequency (ClockBoost clock multiplication factor equals 1)		25		180	MHz
f_{CLK2}	Input clock frequency (ClockBoost clock multiplication factor equals 2)		16		90	MHz
f_{CLKDEV}	Input deviation from user specification in the MAX+PLUS II software *(1)*				25,000 *(2)*	PPM
$t_{INCLKSTB}$	Input clock stability (measured between adjacent clocks)				100	ps
t_{LOCK}	Time required for ClockLock or ClockBoost to acquire lock *(3)*				10	µs
t_{JITTER}	Jitter on ClockLock or ClockBoost-generated clock *(4)*	$t_{INCLKSTB}$ < 100			250	ps
		$t_{INCLKSTB}$ < 50			200 *(4)*	ps
$t_{OUTDUTY}$	Duty cycle for ClockLock or ClockBoost-generated clock		40	50	60	%

Table 17. 32-Bit IDCODE for FLEX 10KE Devices *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) *(2)*
EPF10K30E	0001	0001 0000 0011 0000	00001101110	1
EPF10K50E EPF10K50S	0001	0001 0000 0101 0000	00001101110	1
EPF10K100E	0010	0000 0001 0000 0000	00001101110	1
EPF10K130E	0001	0000 0001 0011 0000	00001101110	1
EPF10K200E EPF10K200S	0001	0000 0010 0000 0000	00001101110	1

Notes:
(1) The most significant bit (MSB) is on the left.
(2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

FLEX 10KE devices include weak pull-up resistors on the JTAG pins.

For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Jam Programming & Test Language Specification*

Figure 20 shows the timing requirements for the JTAG signals.

Figure 20. FLEX 10KE JTAG Waveforms

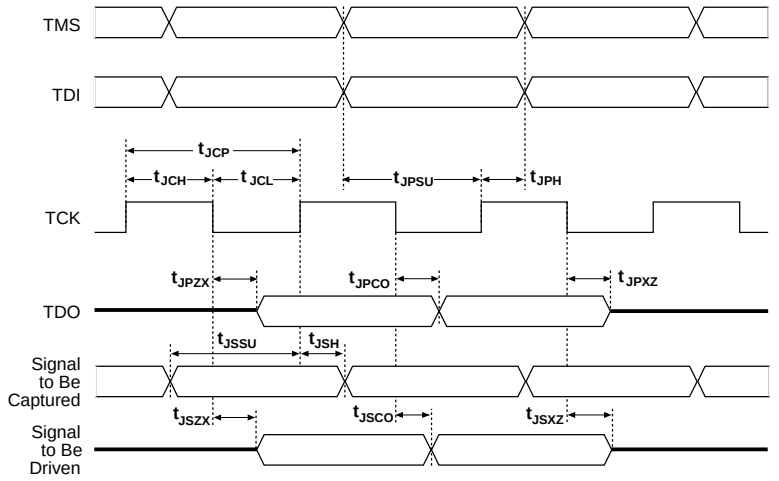


Table 18 shows the timing parameters and values for FLEX 10KE devices.

Table 18. FLEX 10KE JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

Figure 22 shows the required relationship between V_{CCIO} and V_{CCINT} for 3.3-V PCI compliance.

Figure 22. Relationship between V_{CCIO} & V_{CCINT} for 3.3-V PCI Compliance

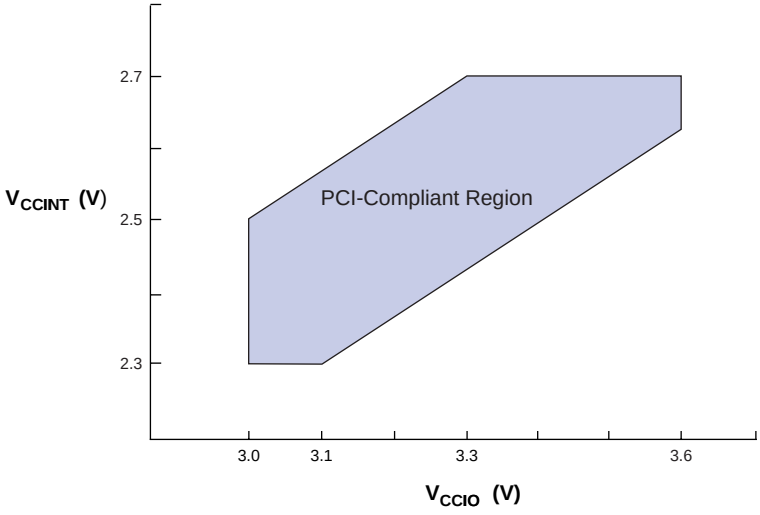


Figure 23 shows the typical output drive characteristics of FLEX 10KE devices with 3.3-V and 2.5-V V_{CCIO}. The output driver is compliant to the 3.3-V ***PCI Local Bus Specification, Revision 2.2*** (when VCCIO pins are connected to 3.3 V). FLEX 10KE devices with a -1 speed grade also comply with the drive strength requirements of the ***PCI Local Bus Specification, Revision 2.2*** (when VCCINT pins are powered with a minimum supply of 2.375 V, and VCCIO pins are connected to 3.3 V). Therefore, these devices can be used in open 5.0-V PCI systems.

Table 34. EPF10K30E Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		6.4		7.6		8.8	ns
$t_{EABRCOMB}$	6.4		7.6		8.8		ns
$t_{EABRCREG}$	4.4		5.1		6.0		ns
t_{EABWP}	2.5		2.9		3.3		ns
$t_{EABWCOMB}$	6.0		7.0		8.0		ns
$t_{EABWCREG}$	6.8		7.8		9.0		ns
t_{EABDD}		5.7		6.7		7.7	ns
$t_{EABDATACO}$		0.8		0.9		1.1	ns
$t_{EABDATASU}$	1.5		1.7		2.0		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	1.3		1.4		1.7		ns
t_{EABWEH}	0.0		0.0		0.0		ns
$t_{EABWDSU}$	1.5		1.7		2.0		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	3.0		3.6		4.3		ns
t_{EABWAH}	0.5		0.5		0.4		ns
t_{EABWO}		5.1		6.0		6.8	ns

Table 53. EPF10K130E Device IOE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{OD3}		4.0		5.6		7.5	ns
t_{XZ}		2.8		4.1		5.5	ns
t_{ZX1}		2.8		4.1		5.5	ns
t_{ZX2}		2.8		4.1		5.5	ns
t_{ZX3}		4.0		5.6		7.5	ns
t_{INREG}		2.5		3.0		4.1	ns
t_{IOFD}		0.4		0.5		0.6	ns
t_{INCOMB}		0.4		0.5		0.6	ns

Table 54. EPF10K130E Device EAB Internal Microparameters *(Part 1 of 2)* *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.5		2.0		2.6	ns
$t_{EABDATA2}$		0.0		0.0		0.0	ns
t_{EABWE1}		1.5		2.0		2.6	ns
t_{EABWE2}		0.3		0.4		0.5	ns
t_{EABRE1}		0.3		0.4		0.5	ns
t_{EABRE2}		0.0		0.0		0.0	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.3		0.4		0.5	ns
$t_{EABBYPASS}$		0.1		0.1		0.2	ns
t_{EABSU}	0.8		1.0		1.4		ns
t_{EABH}	0.1		0.2		0.2		ns
t_{EABCLR}	0.3		0.4		0.5		ns
t_{AA}		4.0		5.0		6.6	ns
t_{WP}	2.7		3.5		4.7		ns
t_{RP}	1.0		1.3		1.7		ns
t_{WDSU}	1.0		1.3		1.7		ns
t_{WDH}	0.2		0.2		0.3		ns
t_{WASU}	1.6		2.1		2.8		ns
t_{WAH}	1.6		2.1		2.8		ns
t_{RASU}	3.0		3.9		5.2		ns
t_{RAH}	0.1		0.1		0.2		ns
t_{WO}		1.5		2.0		2.6	ns

Table 56. EPF10K130E Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		2.8		3.5		4.4	ns
t_{DIN2LE}		0.7		1.2		1.6	ns
$t_{DIN2DATA}$		1.6		1.9		2.2	ns
$t_{DCLK2IOE}$		1.6		2.1		2.7	ns
$t_{DCLK2LE}$		0.7		1.2		1.6	ns
$t_{SAMELAB}$		0.1		0.2		0.2	ns
$t_{SAMEROW}$		1.9		3.4		5.1	ns
$t_{SAMECOLUMN}$		0.9		2.6		4.4	ns
$t_{DIFFROW}$		2.8		6.0		9.5	ns
$t_{TWOROWS}$		4.7		9.4		14.6	ns
$t_{LEPERIPH}$		3.1		4.7		6.9	ns
$t_{LABCARRY}$		0.6		0.8		1.0	ns
$t_{LABCASC}$		0.9		1.2		1.6	ns

Table 57. EPF10K130E External Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		9.0		12.0		16.0	ns
t_{INSU} *(3)*	1.9		2.1		3.0		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	5.0	2.0	7.0	2.0	9.2	ns
t_{INSU} *(4)*	0.9		1.1		–		ns
t_{INH} *(4)*	0.0		0.0		–		ns
t_{OUTCO} *(4)*	0.5	4.0	0.5	6.0	–	–	ns
t_{PCISU}	3.0		6.2		–		ns
t_{PCIH}	0.0		0.0		–		ns
t_{PCICO}	2.0	6.0	2.0	6.9	–	–	ns

Table 59. EPF10K200E Device LE Timing Microparameters *(Part 2 of 2)* *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_H	0.9		1.1		1.5		ns
t_{PRE}		0.5		0.6		0.8	ns
t_{CLR}		0.5		0.6		0.8	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns

Table 60. EPF10K200E Device IOE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{IOD}		1.6		1.9		2.6	ns
t_{IOC}		0.3		0.3		0.5	ns
t_{IOCO}		1.6		1.9		2.6	ns
t_{IOCOMB}		0.5		0.6		0.8	ns
t_{IOSU}	0.8		0.9		1.2		ns
t_{IOH}	0.7		0.8		1.1		ns
t_{IOCLR}		0.2		0.2		0.3	ns
t_{OD1}		0.6		0.7		0.9	ns
t_{OD2}		0.1		0.2		0.7	ns
t_{OD3}		2.5		3.0		3.9	ns
t_{XZ}		4.4		5.3		7.1	ns
t_{ZX1}		4.4		5.3		7.1	ns
t_{ZX2}		3.9		4.8		6.9	ns
t_{ZX3}		6.3		7.6		10.1	ns
t_{INREG}		4.8		5.7		7.7	ns
t_{IOFD}		1.5		1.8		2.4	ns
t_{INCOMB}		1.5		1.8		2.4	ns

Table 61. EPF10K200E Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		2.0		2.4		3.2	ns
$t_{EABDATA1}$		0.4		0.5		0.6	ns
t_{EABWE1}		1.4		1.7		2.3	ns
t_{EABWE2}		0.0		0.0		0.0	ns
t_{EABRE1}		0		0		0	ns
t_{EABRE2}		0.4		0.5		0.6	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.8		0.9		1.2	ns
$t_{EABBYPASS}$		0.0		0.1		0.1	ns
t_{EABSU}	0.9		1.1		1.5		ns
t_{EABH}	0.4		0.5		0.6		ns
t_{EABCLR}	0.8		0.9		1.2		ns
t_{AA}		3.1		3.7		4.9	ns
t_{WP}	3.3		4.0		5.3		ns
t_{RP}	0.9		1.1		1.5		ns
t_{WDSU}	0.9		1.1		1.5		ns
t_{WDH}	0.1		0.1		0.1		ns
t_{WASU}	1.3		1.6		2.1		ns
t_{WAH}	2.1		2.5		3.3		ns
t_{RASU}	2.2		2.6		3.5		ns
t_{RAH}	0.1		0.1		0.2		ns
t_{WO}		2.0		2.4		3.2	ns
t_{DD}		2.0		2.4		3.2	ns
t_{EABOUT}		0.0		0.1		0.1	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	3.3		4.0		5.3		ns

Table 62. EPF10K200E Device EAB Internal Timing Macroparameters (Part 1 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		5.1		6.4		8.4	ns
$t_{EABRCOMB}$	5.1		6.4		8.4		ns
$t_{EABRCREG}$	4.8		5.7		7.6		ns
t_{EABWP}	3.3		4.0		5.3		ns

Table 64. EPF10K200E External Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		10.0		12.0		16.0	ns
t_{INSU}	2.8		3.4		4.4		ns
t_{INH}	0.0		0.0		0.0		ns
t_{OUTCO}	2.0	4.5	2.0	5.3	2.0	7.8	ns
t_{PCISU}	3.0		6.2		-		ns
t_{PCIH}	0.0		0.0		-		ns
t_{PCICO}	2.0	6.0	2.0	8.9	-	-	ns

Table 65. EPF10K200E External Bidirectional Timing Parameters *Notes (1), (2)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$	3.0		4.0		5.5		ns
$t_{INHBIDIR}$	0.0		0.0		0.0		ns
$t_{OUTCOBIDIR}$	2.0	4.5	2.0	5.3	2.0	7.8	ns
$t_{XZBIDIR}$		8.1		9.5		13.0	ns
$t_{ZXBIDIR}$		8.1		9.5		13.0	ns

Notes to tables:

(1) All timing parameters are described in Tables 24 through 30 in this data sheet.
(2) These parameters are specified by characterization.

Tables 66 through 79 show EPF10K50S and EPF10K200S device external timing parameters.

Table 66. EPF10K50S Device LE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.6		0.8		1.1	ns
t_{CLUT}		0.5		0.6		0.8	ns
t_{RLUT}		0.6		0.7		0.9	ns
t_{PACKED}		0.2		0.3		0.4	ns
t_{EN}		0.6		0.7		0.9	ns
t_{CICO}		0.1		0.1		0.1	ns
t_{CGEN}		0.4		0.5		0.6	ns

Table 77. EPF10K200S Device Interconnect Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.5		1.0		1.4	ns

Table 78. EPF10K200S External Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{DRR}		9.0		12.0		16.0	ns
t_{INSU} *(2)*	3.1		3.7		4.7		ns
t_{INH} *(2)*	0.0		0.0		0.0		ns
t_{OUTCO} *(2)*	2.0	3.7	2.0	4.4	2.0	6.3	ns
t_{INSU}*(3)*	2.1		2.7		–		ns
t_{INH} *(3)*	0.0		0.0		–		ns
t_{OUTCO}*(3)*	0.5	2.7	0.5	3.4	–	–	ns
t_{PCISU}	3.0		4.2		–		ns
t_{PCIH}	0.0		0.0		–		ns
t_{PCICO}	2.0	6.0	2.0	8.9	–	–	ns

Table 79. EPF10K200S External Bidirectional Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{INSUBIDIR}$ *(2)*	2.3		3.4		4.4		ns
$t_{INHBIDIR}$ *(2)*	0.0		0.0		0.0		ns
$t_{INSUBIDIR}$ *(3)*	3.3		4.4		–		ns
$t_{INHBIDIR}$ *(3)*	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ *(2)*	2.0	3.7	2.0	4.4	2.0	6.3	ns
$t_{XZBIDIR}$ *(2)*		6.9		7.6		9.2	ns
$t_{ZXBIDIR}$ *(2)*		5.9		6.6		–	ns
$t_{OUTCOBIDIR}$ *(3)*	0.5	2.7	0.5	3.4	–	–	ns
$t_{XZBIDIR}$ *(3)*		6.9		7.6		9.2	ns
$t_{ZXBIDIR}$ *(3)*		5.9		6.6		–	ns

Notes to tables:

(1) All timing parameters are described in Tables 24 through 30 in this data sheet.
(2) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(3) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Additionally, the Altera software offers several features that help plan for future device migration by preventing the use of conflicting I/O pins.

Table 81. I/O Counts for FLEX 10KA & FLEX 10KE Devices

FLEX 10KA		FLEX 10KE	
Device	**I/O Count**	**Device**	**I/O Count**
EPF10K30AF256	191	EPF10K30EF256	176
EPF10K30AF484	246	EPF10K30EF484	220
EPF10K50VB356	274	EPF10K50SB356	220
EPF10K50VF484	291	EPF10K50EF484	254
EPF10K50VF484	291	EPF10K50SF484	254
EPF10K100AF484	369	EPF10K100EF484	338

Configuration Schemes

The configuration data for a FLEX 10KE device can be loaded with one of five configuration schemes (see Table 82), chosen on the basis of the target application. An EPC1, EPC2, or EPC16 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of a FLEX 10KE device, allowing automatic configuration on system power-up.

Multiple FLEX 10KE devices can be configured in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device. Additional FLEX 10K, FLEX 10KA, FLEX 10KE, and FLEX 6000 devices can be configured in the same serial chain.

Table 82. Data Sources for FLEX 10KE Configuration

Configuration Scheme	Data Source
Configuration device	EPC1, EPC2, or EPC16 configuration device
Passive serial (PS)	BitBlaster, ByteBlasterMV, or MasterBlaster download cables, or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	BitBlaster or ByteBlasterMV download cables, or microprocessor with a Jam STAPL file or JBC file