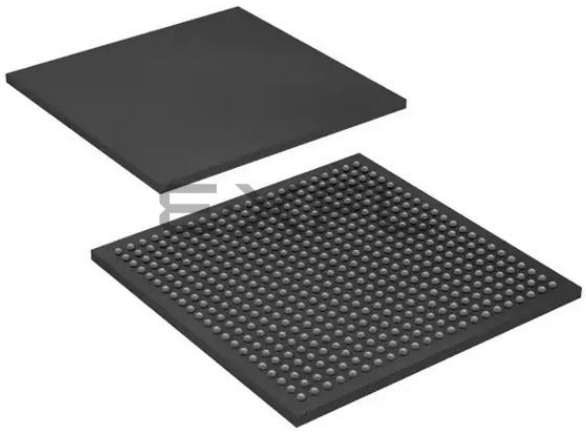

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	360
Number of Logic Elements/Cells	2880
Total RAM Bits	40960
Number of I/O	220
Number of Gates	199000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf10k50sfc484-2

- Software design support and automatic place-and-route provided by Altera's development systems for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800
- Flexible package options
  - Available in a variety of packages with 144 to 672 pins, including the innovative FineLine BGA™ packages (see Tables 3 and 4)
  - SameFrame™ pin-out compatibility between FLEX 10KA and FLEX 10KE devices across a range of device densities and pin counts
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), DesignWare components, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, VeriBest, and Viewlogic

Table 3. FLEX 10KE Package Options & I/O Pin Count *Notes (1), (2)*

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP RQFP	256-Pin FineLine BGA	356-Pin BGA	484-Pin FineLine BGA	599-Pin PGA	600-Pin BGA	672-Pin FineLine BGA
EPF10K30E	102	147		176		220			220 *(3)*
EPF10K50E	102	147	189	191		254			254 *(3)*
EPF10K50S	102	147	189	191	220	254			254 *(3)*
EPF10K100E		147	189	191	274	338			338 *(3)*
EPF10K130E			186		274	369		424	413
EPF10K200E							470	470	470
EPF10K200S			182		274	369	470	470	470

Notes:

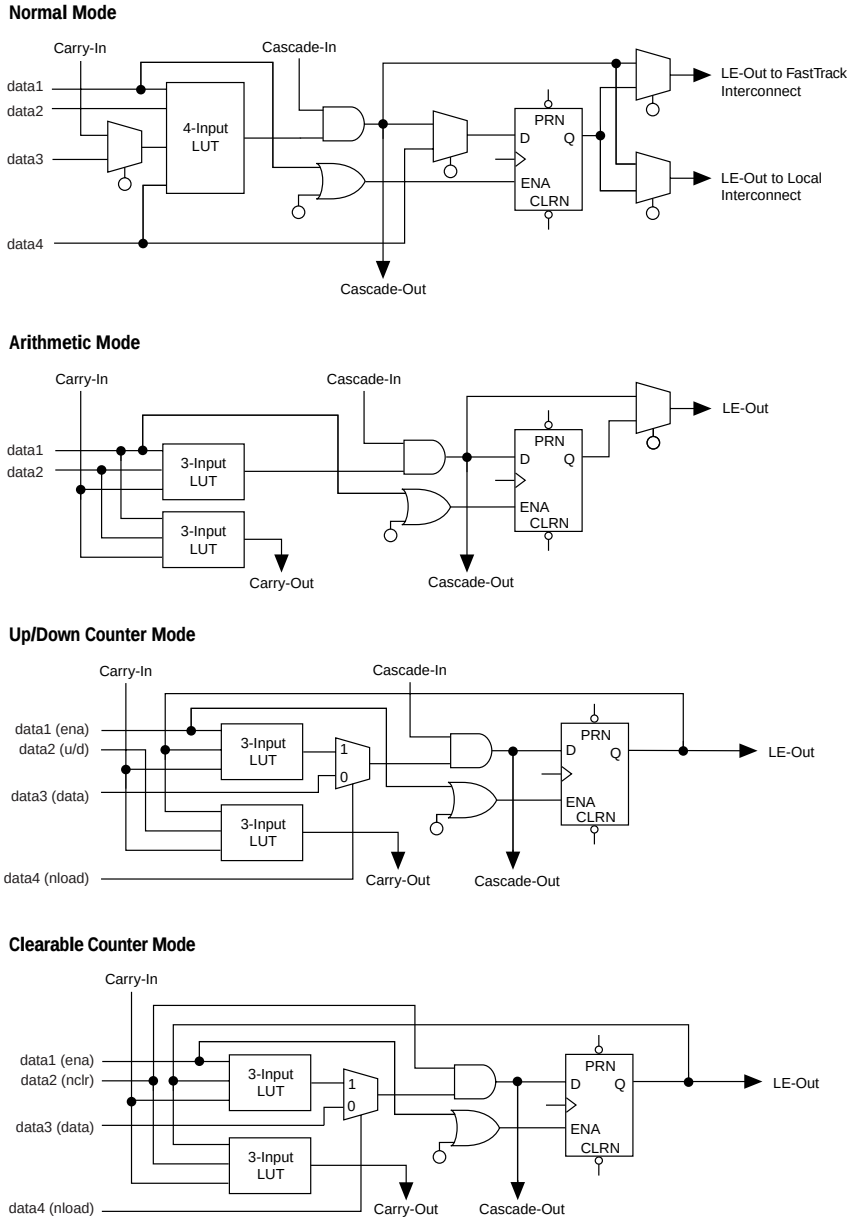
(1) FLEX 10KE device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), pin-grid array (PGA), and ball-grid array (BGA) packages.

(2) Devices in the same package are pin-compatible, although some devices have more I/O pins than others. When planning device migration, use the I/O pins that are common to all devices.

(3) This option is supported with a 484-pin FineLine BGA package. By using SameFrame pin migration, all FineLine BGA packages are pin-compatible. For example, a board can be designed to support 256-pin, 484-pin, and 672-pin FineLine BGA packages. The Altera software automatically avoids conflicting pins when future migration is set.

Figure 11 shows the LE operating modes.

Figure 11. FLEX 10KE LE Operating Modes



In addition to the six clear and preset modes, FLEX 10KE devices provide a chip-wide reset pin that can reset all registers in the device. Use of this feature is set during design entry. In any of the clear and preset modes, the chip-wide reset overrides all other signals. Registers with asynchronous presets may be preset when the chip-wide reset is asserted. Inversion can be used to implement the asynchronous preset. Figure 12 shows examples of how to setup the preset and clear inputs for the desired functionality.

Figure 12. FLEX 10KE LE Clear & Preset Modes

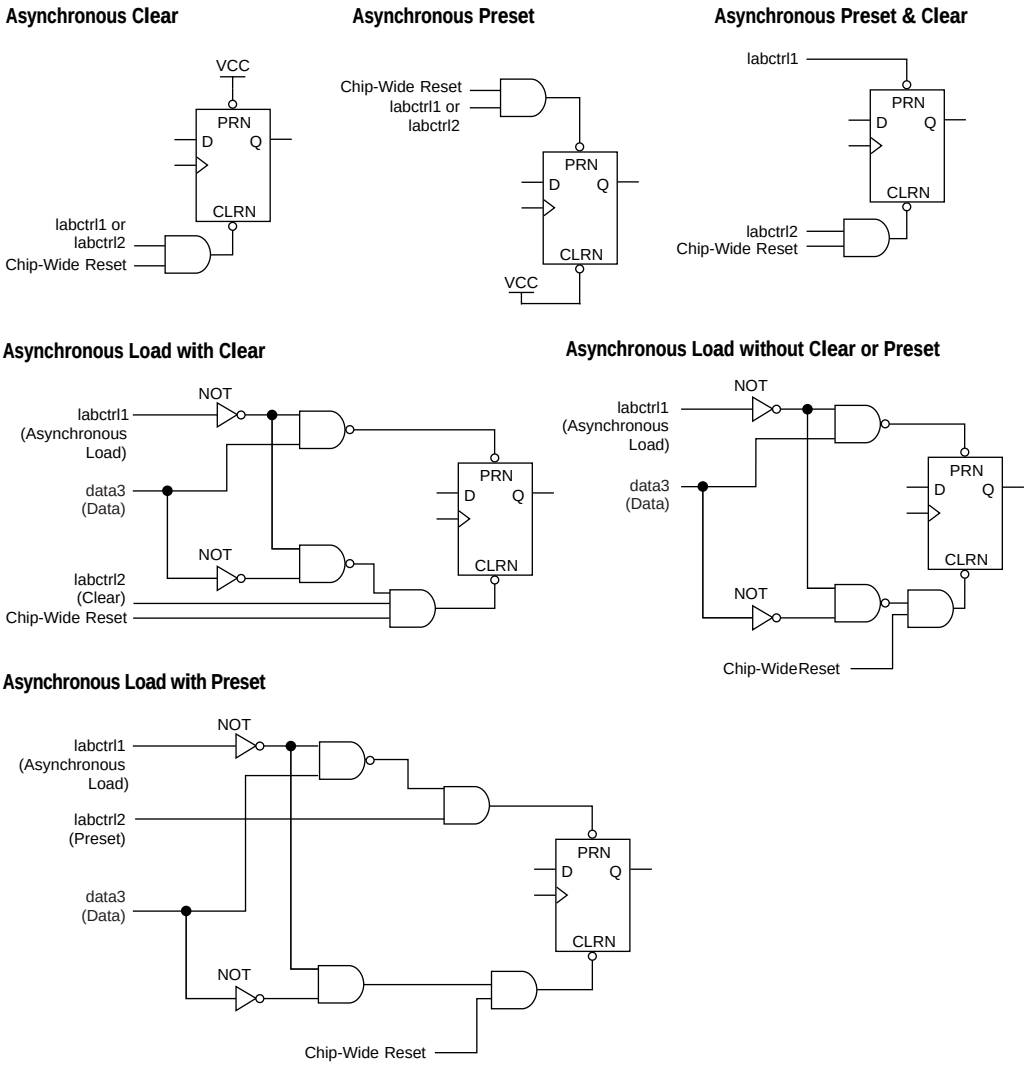
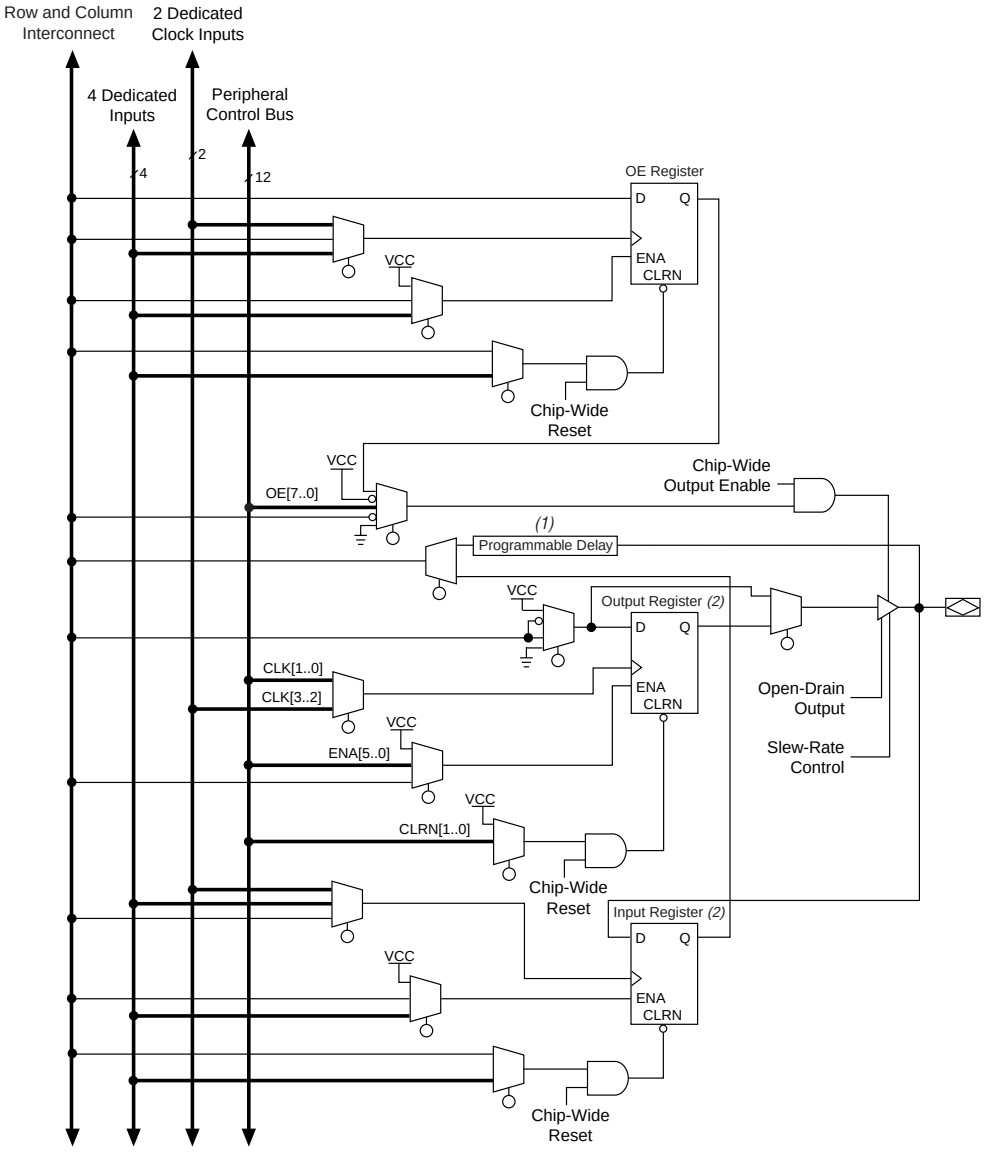


Figure 15. FLEX 10KE Bidirectional I/O Registers



Note:

(1) All FLEX 10KE devices (except the EPF10K50E and EPF10K200E devices) have a programmable input delay buffer on the input path.

On all FLEX 10KE devices (except EPF10K50E and EPF10K200E devices), the input path from the I/O pad to the FastTrack Interconnect has a programmable delay element that can be used to guarantee a zero hold time. EPF10K50S and EPF10K200S devices also support this feature. Depending on the placement of the IOE relative to what it is driving, the designer may choose to turn on the programmable delay to ensure a zero hold time or turn it off to minimize setup time. This feature is used to reduce setup time for complex pin-to-register paths (e.g., PCI designs).

Each IOE selects the clock, clear, clock enable, and output enable controls from a network of I/O control signals called the peripheral control bus. The peripheral control bus uses high-speed drivers to minimize signal skew across the device and provides up to 12 peripheral control signals that can be allocated as follows:

- Up to eight output enable signals
- Up to six clock enable signals
- Up to two clock signals
- Up to two clear signals

If more than six clock enable or eight output enable signals are required, each IOE on the device can be controlled by clock enable and output enable signals driven by specific LEs. In addition to the two clock signals available on the peripheral control bus, each IOE can use one of two dedicated clock pins. Each peripheral control signal can be driven by any of the dedicated input pins or the first LE of each LAB in a particular row. In addition, a LE in a different row can drive a column interconnect, which causes a row interconnect to drive the peripheral control signal. The chip-wide reset signal resets all IOE registers, overriding any other control signals.

When a dedicated clock pin drives IOE registers, it can be inverted for all IOEs in the device. All IOEs must use the same sense of the clock. For example, if any IOE uses the inverted clock, all IOEs must use the inverted clock and no IOE can use the non-inverted clock. However, LEs can still use the true or complement of the clock on a LAB-by-LAB basis.

The incoming signal may be inverted at the dedicated clock pin and will drive all IOEs. For the true and complement of a clock to be used to drive IOEs, drive it into both global clock pins. One global clock pin will supply the true, and the other will supply the complement.

When the true and complement of a dedicated input drives IOE clocks, two signals on the peripheral control bus are consumed, one for each sense of the clock.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All FLEX 10KE devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. FLEX 10KE devices can also be configured using the JTAG pins through the BitBlaster or ByteBlasterMV download cable, or via hardware that uses the Jam™ STAPL programming and test language. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. FLEX 10KE devices support the JTAG instructions shown in Table 15.

Table 15. FLEX 10KE JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation.
USERCODE	Selects the user electronic signature (USERCODE) register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ICR Instructions	These instructions are used when configuring a FLEX 10KE device via JTAG ports with a BitBlaster or ByteBlasterMV download cable, or using a Jam File (**.jam**) or Jam Byte-Code File (**.jbc**) via an embedded processor.

The instruction register length of FLEX 10KE devices is 10 bits. The USERCODE register length in FLEX 10KE devices is 32 bits; 7 bits are determined by the user, and 25 bits are pre-determined. Tables 16 and 17 show the boundary-scan register length and device IDCODE information for FLEX 10KE devices.

Table 16. FLEX 10KE Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPF10K30E	690
EPF10K50E EPF10K50S	798
EPF10K100E	1,050
EPF10K130E	1,308
EPF10K200E EPF10K200S	1,446

Table 17. 32-Bit IDCODE for FLEX 10KE Devices *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) *(2)*
EPF10K30E	0001	0001 0000 0011 0000	00001101110	1
EPF10K50E EPF10K50S	0001	0001 0000 0101 0000	00001101110	1
EPF10K100E	0010	0000 0001 0000 0000	00001101110	1
EPF10K130E	0001	0000 0001 0011 0000	00001101110	1
EPF10K200E EPF10K200S	0001	0000 0010 0000 0000	00001101110	1

Notes:
(1) The most significant bit (MSB) is on the left.
(2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

FLEX 10KE devices include weak pull-up resistors on the JTAG pins.

For more information, see the following documents:

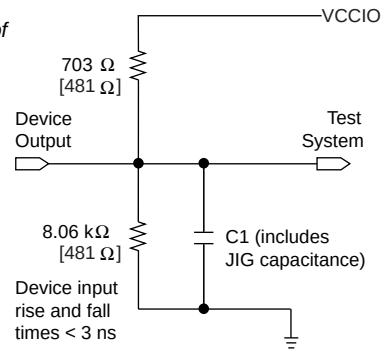
- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Jam Programming & Test Language Specification*

Generic Testing

Each FLEX 10KE device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for FLEX 10KE devices are made under conditions equivalent to those shown in Figure 21. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 21. FLEX 10KE AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V devices or outputs. Numbers without brackets are for 3.3-V. devices or outputs.



Operating Conditions

Tables 19 through 23 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V FLEX 10KE devices.

Table 19. FLEX 10KE 2.5-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground *(2)*	–0.5	3.6	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage		–2.0	5.75	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	PQFP, TQFP, BGA, and FineLine BGA packages, under bias		135	° C
		Ceramic PGA packages, under bias		150	° C

Table 20. 2.5-V EPF10K50E & EPF10K200E Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	2.30 (2.30)	2.70 (2.70)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(3)*, *(4)*	2.30 (2.30)	2.70 (2.70)	V
V_I	Input voltage	*(5)*	–0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

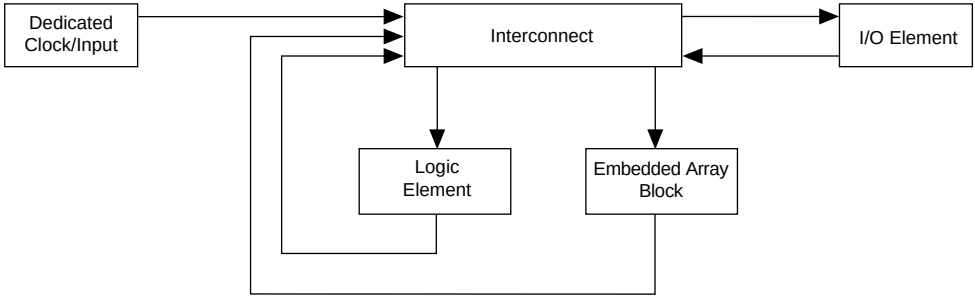
Table 21. 2.5-V EPF10K30E, EPF10K50S, EPF10K100E, EPF10K130E & EPF10K200S Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	2.375 (2.375)	2.625 (2.625)	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
	Supply voltage for output buffers, 2.5-V operation	*(3)*, *(4)*	2.375 (2.375)	2.625 (2.625)	V
V_I	Input voltage	*(5)*	–0.5	5.75	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
T_J	Operating temperature	For commercial use	0	85	° C
		For industrial use	–40	100	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Timing simulation and delay prediction are available with the Altera Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and device-wide performance analysis.

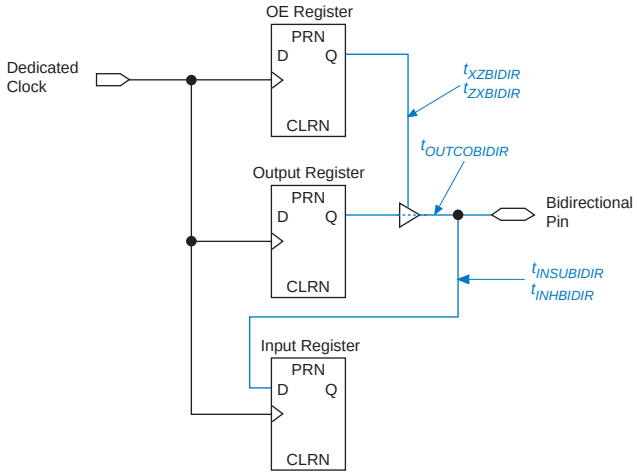
Figure 24 shows the overall timing model, which maps the possible paths to and from the various elements of the FLEX 10KE device.

Figure 24. FLEX 10KE Device Timing Model



Figures 25 through 28 show the delays that correspond to various paths and functions within the LE, IOE, EAB, and bidirectional timing models.

Figure 28. Synchronous Bidirectional Pin External Timing Model



Tables 24 through 28 describe the FLEX 10KE device internal timing parameters. Tables 29 through 30 describe the FLEX 10KE external timing parameters and their symbols.

Table 24. LE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Condition
t_{LUT}	LUT delay for data-in	
t_{CLUT}	LUT delay for carry-in	
t_{RLUT}	LUT delay for LE register feedback	
t_{PACKED}	Data-in to packed register delay	
t_{EN}	LE register enable delay	
t_{CICO}	Carry-in to carry-out delay	
t_{CGEN}	Data-in to carry-out delay	
t_{CGENR}	LE register feedback to carry-out delay	
t_{CASC}	Cascade-in to cascade-out delay	
t_{C}	LE register control signal delay	
t_{CO}	LE register clock-to-output delay	
t_{COMB}	Combinatorial delay	
t_{SU}	LE register setup time for data and enable signals before clock; LE register recovery time after asynchronous clear, preset, or load	
t_{H}	LE register hold time for data and enable signals after clock	
t_{PRE}	LE register preset delay	

Figures 29 and 30 show the asynchronous and synchronous timing waveforms, respectively, or the EAB macroparameters in Tables 26 and 27.

Figure 29. EAB Asynchronous Timing Waveforms

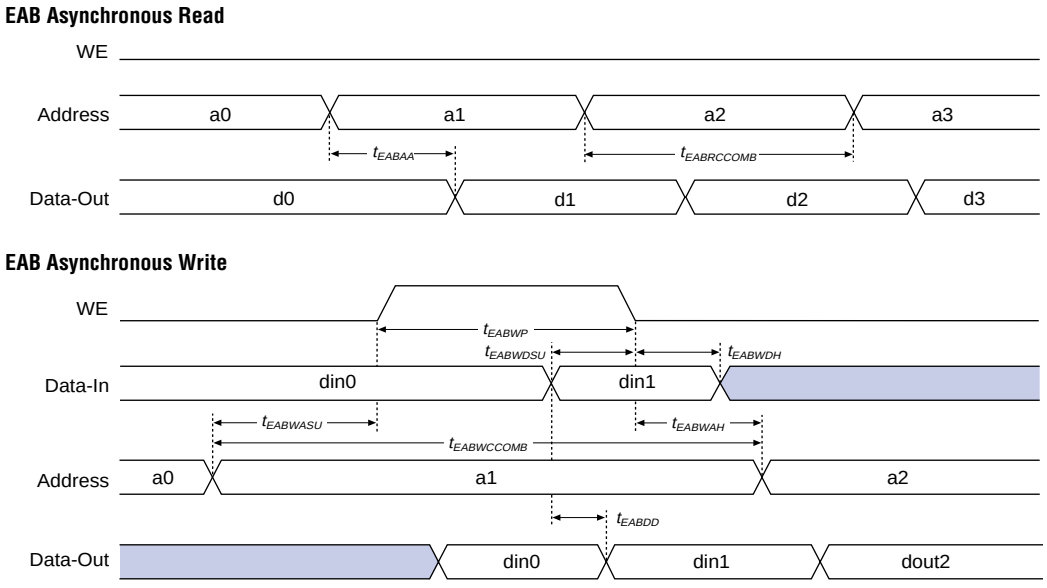


Table 38. EPF10K50E Device LE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{H}	0.9		1.0		1.4		ns
t_{PRE}		0.5		0.6		0.8	ns
t_{CLR}		0.5		0.6		0.8	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns

Table 39. EPF10K50E Device IOE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{IOD}		2.2		2.4		3.3	ns
t_{IOC}		0.3		0.3		0.5	ns
t_{IOCO}		1.0		1.0		1.4	ns
t_{IOCOMB}		0.0		0.0		0.2	ns
t_{IOSU}	1.0		1.2		1.7		ns
t_{IOH}	0.3		0.3		0.5		ns
t_{IOCLR}		0.9		1.0		1.4	ns
t_{OD1}		0.8		0.9		1.2	ns
t_{OD2}		0.3		0.4		0.7	ns
t_{OD3}		3.0		3.5		3.5	ns
t_{XZ}		1.4		1.7		2.3	ns
t_{ZX1}		1.4		1.7		2.3	ns
t_{ZX2}		0.9		1.2		1.8	ns
t_{ZX3}		3.6		4.3		4.6	ns
t_{INREG}		4.9		5.8		7.8	ns
t_{IOFD}		2.8		3.3		4.5	ns
t_{INCOMB}		2.8		3.3		4.5	ns

Table 40. EPF10K50E Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.7		2.0		2.7	ns
$t_{EABDATA1}$		0.6		0.7		0.9	ns
t_{EABWE1}		1.1		1.3		1.8	ns
t_{EABWE2}		0.4		0.4		0.6	ns
t_{EABRE1}		0.8		0.9		1.2	ns
t_{EABRE2}		0.4		0.4		0.6	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.3		0.3		0.5	ns
$t_{EABBYPASS}$		0.5		0.6		0.8	ns
t_{EABSU}	0.9		1.0		1.4		ns
t_{EABH}	0.4		0.4		0.6		ns
t_{EABCLR}	0.3		0.3		0.5		ns
t_{AA}		3.2		3.8		5.1	ns
t_{WP}	2.5		2.9		3.9		ns
t_{RP}	0.9		1.1		1.5		ns
t_{WDSU}	0.9		1.0		1.4		ns
t_{WDH}	0.1		0.1		0.2		ns
t_{WASU}	1.7		2.0		2.7		ns
t_{WAH}	1.8		2.1		2.9		ns
t_{RASU}	3.1		3.7		5.0		ns
t_{RAH}	0.2		0.2		0.3		ns
t_{WO}		2.5		2.9		3.9	ns
t_{DD}		2.5		2.9		3.9	ns
t_{EABOUT}		0.5		0.6		0.8	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	2.5		2.9		3.9		ns

Table 50. EPF10K100E External Timing Parameters *Notes (1), (2)*							
Symbol	**-1 Speed Grade**		**-2 Speed Grade**		**-3 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{DRR}		9.0		12.0		16.0	ns
t_{INSU} *(3)*	2.0		2.5		3.3		ns
t_{INH} *(3)*	0.0		0.0		0.0		ns
t_{OUTCO} *(3)*	2.0	5.2	2.0	6.9	2.0	9.1	ns
t_{INSU} *(4)*	2.0		2.2		–		ns
t_{INH} *(4)*	0.0		0.0		–		ns
t_{OUTCO} *(4)*	0.5	3.0	0.5	4.6	–	–	ns
t_{PCISU}	3.0		6.2		–		ns
t_{PCIH}	0.0		0.0		–		ns
t_{PCICO}	2.0	6.0	2.0	6.9	–	–	ns

Table 51. EPF10K100E External Bidirectional Timing Parameters *Notes (1), (2)*							
Symbol	**-1 Speed Grade**		**-2 Speed Grade**		**-3 Speed Grade**		**Unit**
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{INSUBIDIR}$ *(3)*	1.7		2.5		3.3		ns
$t_{INHBIDIR}$ *(3)*	0.0		0.0		0.0		ns
$t_{INSUBIDIR}$ *(4)*	2.0		2.8		–		ns
$t_{INHBIDIR}$ *(4)*	0.0		0.0		–		ns
$t_{OUTCOBIDIR}$ *(3)*	2.0	5.2	2.0	6.9	2.0	9.1	ns
$t_{XZBIDIR}$ *(3)*		5.6		7.5		10.1	ns
$t_{ZXBIDIR}$ *(3)*		5.6		7.5		10.1	ns
$t_{OUTCOBIDIR}$ *(4)*	0.5	3.0	0.5	4.6	–	–	ns
$t_{XZBIDIR}$ *(4)*		4.6		6.5		–	ns
$t_{ZXBIDIR}$ *(4)*		4.6		6.5		–	ns

Notes to tables:

(1) All timing parameters are described in Tables 24 through 30 in this data sheet.
(2) These parameters are specified by characterization.
(3) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Table 59. EPF10K200E Device LE Timing Microparameters *(Part 2 of 2)* *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_H	0.9		1.1		1.5		ns
t_{PRE}		0.5		0.6		0.8	ns
t_{CLR}		0.5		0.6		0.8	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns

Table 60. EPF10K200E Device IOE Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{IOD}		1.6		1.9		2.6	ns
t_{IOC}		0.3		0.3		0.5	ns
t_{IOCO}		1.6		1.9		2.6	ns
t_{IOCOMB}		0.5		0.6		0.8	ns
t_{IOSU}	0.8		0.9		1.2		ns
t_{IOH}	0.7		0.8		1.1		ns
t_{IOCLR}		0.2		0.2		0.3	ns
t_{OD1}		0.6		0.7		0.9	ns
t_{OD2}		0.1		0.2		0.7	ns
t_{OD3}		2.5		3.0		3.9	ns
t_{XZ}		4.4		5.3		7.1	ns
t_{ZX1}		4.4		5.3		7.1	ns
t_{ZX2}		3.9		4.8		6.9	ns
t_{ZX3}		6.3		7.6		10.1	ns
t_{INREG}		4.8		5.7		7.7	ns
t_{IOFD}		1.5		1.8		2.4	ns
t_{INCOMB}		1.5		1.8		2.4	ns

Table 69. EPF10K50S Device EAB Internal Timing Macroparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{EABAA}		3.7		5.2		7.0	ns
$t_{EABRCCOMB}$	3.7		5.2		7.0		ns
$t_{EABRCREG}$	3.5		4.9		6.6		ns
t_{EABWP}	2.0		2.8		3.8		ns
$t_{EABWCCOMB}$	4.5		6.3		8.6		ns
$t_{EABWCREG}$	5.6		7.8		10.6		ns
t_{EABDD}		3.8		5.3		7.2	ns
$t_{EABDATACO}$		0.8		1.1		1.5	ns
$t_{EABDATASU}$	1.1		1.6		2.1		ns
$t_{EABDATAH}$	0.0		0.0		0.0		ns
$t_{EABWESU}$	0.7		1.0		1.3		ns
t_{EABWEH}	0.4		0.6		0.8		ns
$t_{EABWDSU}$	1.2		1.7		2.2		ns
t_{EABWDH}	0.0		0.0		0.0		ns
$t_{EABWASU}$	1.6		2.3		3.0		ns
t_{EABWAH}	0.9		1.2		1.8		ns
t_{EABWO}		3.1		4.3		5.9	ns

Table 70. EPF10K50S Device Interconnect Timing Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{DIN2IOE}$		3.1		3.7		4.6	ns
t_{DIN2LE}		1.7		2.1		2.7	ns
$t_{DIN2DATA}$		2.7		3.1		5.1	ns
$t_{DCLK2IOE}$		1.6		1.9		2.6	ns
$t_{DCLK2LE}$		1.7		2.1		2.7	ns
$t_{SAMELAB}$		0.1		0.1		0.2	ns
$t_{SAMEROW}$		1.5		1.7		2.4	ns
$t_{SAMECOLUMN}$		1.0		1.3		2.1	ns
$t_{DIFFROW}$		2.5		3.0		4.5	ns
$t_{TWOROWS}$		4.0		4.7		6.9	ns
$t_{LEPERIPH}$		2.6		2.9		3.4	ns
$t_{LABCARRY}$		0.1		0.2		0.2	ns
$t_{LABCASC}$		0.8		1.0		1.3	ns

Table 73. EPF10K200S Device Internal & External Timing Parameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{LUT}		0.7		0.8		1.2	ns
t_{CLUT}		0.4		0.5		0.6	ns
t_{RLUT}		0.5		0.7		0.9	ns
t_{PACKED}		0.4		0.5		0.7	ns
t_{EN}		0.6		0.5		0.6	ns
t_{CICO}		0.1		0.2		0.3	ns
t_{CGEN}		0.3		0.4		0.6	ns
t_{CGENR}		0.1		0.2		0.3	ns
t_{CASC}		0.7		0.8		1.2	ns
t_{C}		0.5		0.6		0.8	ns
t_{CO}		0.5		0.6		0.8	ns
t_{COMB}		0.3		0.6		0.8	ns
t_{SU}	0.4		0.6		0.7		ns
t_{H}	1.0		1.1		1.5		ns
t_{PRE}		0.4		0.6		0.8	ns
t_{CLR}		0.5		0.6		0.8	ns
t_{CH}	2.0		2.5		3.0		ns
t_{CL}	2.0		2.5		3.0		ns

Table 74. EPF10K200S Device IOE Timing Microparameters (Part 1 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{IOD}		1.8		1.9		2.6	ns
t_{IOC}		0.3		0.3		0.5	ns
t_{IOCO}		1.7		1.9		2.6	ns
t_{IOCOMB}		0.5		0.6		0.8	ns
t_{IOSU}	0.8		0.9		1.2		ns
t_{IOH}	0.4		0.8		1.1		ns
t_{IOCLR}		0.2		0.2		0.3	ns
t_{OD1}		1.3		0.7		0.9	ns
t_{OD2}		0.8		0.2		0.4	ns
t_{OD3}		2.9		3.0		3.9	ns
t_{XZ}		5.0		5.3		7.1	ns
t_{ZX1}		5.0		5.3		7.1	ns

Table 74. EPF10K200S Device IOE Timing Microparameters (Part 2 of 2) *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
t_{ZX2}		4.5		4.8		6.6	ns
t_{ZX3}		6.6		7.6		10.1	ns
t_{INREG}		3.7		5.7		7.7	ns
t_{IOFD}		1.8		3.4		4.0	ns
t_{INCOMB}		1.8		3.4		4.0	ns

Table 75. EPF10K200S Device EAB Internal Microparameters *Note (1)*

Symbol	-1 Speed Grade		-2 Speed Grade		-3 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
$t_{EABDATA1}$		1.8		2.4		3.2	ns
$t_{EABDATA1}$		0.4		0.5		0.6	ns
t_{EABWE1}		1.1		1.7		2.3	ns
t_{EABWE2}		0.0		0.0		0.0	ns
t_{EABRE1}		0		0		0	ns
t_{EABRE2}		0.4		0.5		0.6	ns
t_{EABCLK}		0.0		0.0		0.0	ns
t_{EABCO}		0.8		0.9		1.2	ns
$t_{EABBYPASS}$		0.0		0.1		0.1	ns
t_{EABSU}	0.7		1.1		1.5		ns
t_{EABH}	0.4		0.5		0.6		ns
t_{EABCLR}	0.8		0.9		1.2		ns
t_{AA}		2.1		3.7		4.9	ns
t_{WP}	2.1		4.0		5.3		ns
t_{RP}	1.1		1.1		1.5		ns
t_{WDSU}	0.5		1.1		1.5		ns
t_{WDH}	0.1		0.1		0.1		ns
t_{WASU}	1.1		1.6		2.1		ns
t_{WAH}	1.6		2.5		3.3		ns
t_{RASU}	1.6		2.6		3.5		ns
t_{RAH}	0.1		0.1		0.2		ns
t_{WO}		2.0		2.4		3.2	ns
t_{DD}		2.0		2.4		3.2	ns
t_{EABOUT}		0.0		0.1		0.1	ns
t_{EABCH}	1.5		2.0		2.5		ns
t_{EABCL}	2.1		2.8		3.8		ns

Additionally, the Altera software offers several features that help plan for future device migration by preventing the use of conflicting I/O pins.

Table 81. I/O Counts for FLEX 10KA & FLEX 10KE Devices

FLEX 10KA		FLEX 10KE	
Device	**I/O Count**	**Device**	**I/O Count**
EPF10K30AF256	191	EPF10K30EF256	176
EPF10K30AF484	246	EPF10K30EF484	220
EPF10K50VB356	274	EPF10K50SB356	220
EPF10K50VF484	291	EPF10K50EF484	254
EPF10K50VF484	291	EPF10K50SF484	254
EPF10K100AF484	369	EPF10K100EF484	338

Configuration Schemes

The configuration data for a FLEX 10KE device can be loaded with one of five configuration schemes (see Table 82), chosen on the basis of the target application. An EPC1, EPC2, or EPC16 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of a FLEX 10KE device, allowing automatic configuration on system power-up.

Multiple FLEX 10KE devices can be configured in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device. Additional FLEX 10K, FLEX 10KA, FLEX 10KE, and FLEX 6000 devices can be configured in the same serial chain.

Table 82. Data Sources for FLEX 10KE Configuration

Configuration Scheme	Data Source
Configuration device	EPC1, EPC2, or EPC16 configuration device
Passive serial (PS)	BitBlaster, ByteBlasterMV, or MasterBlaster download cables, or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Passive parallel synchronous (PPS)	Parallel data source
JTAG	BitBlaster or ByteBlasterMV download cables, or microprocessor with a Jam STAPL file or JBC file