# Intel - EPF10K50SQC240-1N Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 360 |
| Number of Logic Elements/Cells | 2880 |
| Total RAM Bits | 40960 |
| Number of I/O | 189 |
| Number of Gates | 199000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 240-BFQFP |
| Supplier Device Package | 240-PQFP (32x32) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epf10k50sqc240-1n |

## Functional Description

Each FLEX 10KE device contains an enhanced embedded array to implement memory and specialized logic functions, and a logic array to implement general logic.

The embedded array consists of a series of EABs. When implementing memory functions, each EAB provides 4,096 bits, which can be used to create RAM, ROM, dual-port RAM, or first-in first-out (FIFO) functions. When implementing logic, each EAB can contribute 100 to 600 gates towards complex logic functions, such as multipliers, microcontrollers, state machines, and DSP functions. EABs can be used independently, or multiple EABs can be combined to implement larger functions.

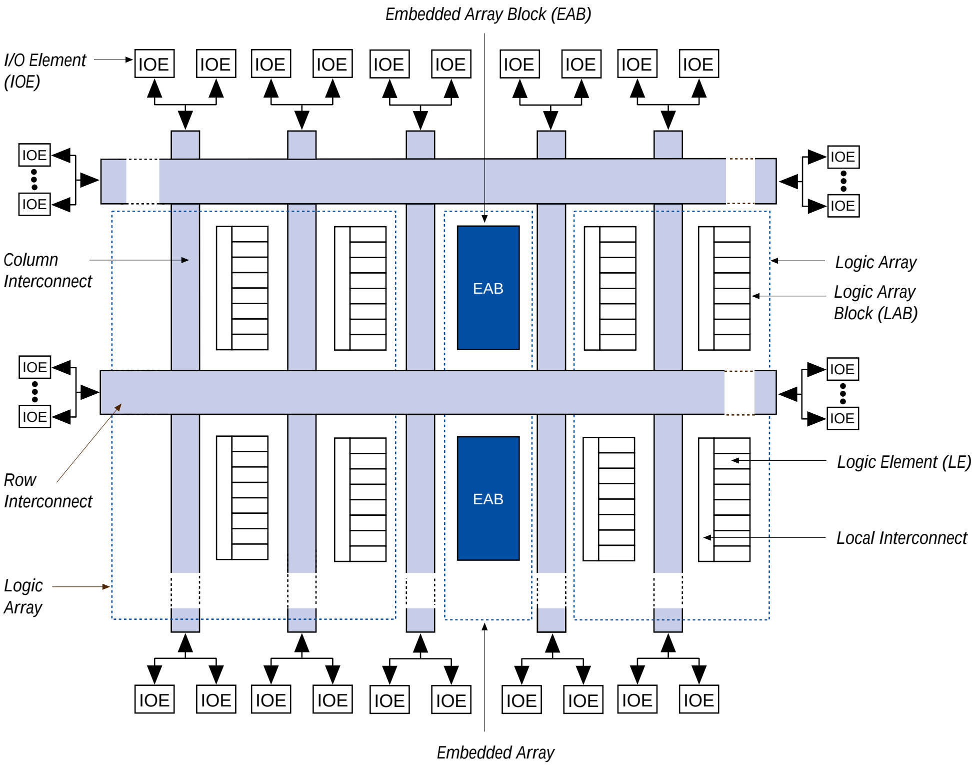
The logic array consists of logic array blocks (LABs). Each LAB contains eight LEs and a local interconnect. An LE consists of a four-input look-up table (LUT), a programmable flipflop, and dedicated signal paths for carry and cascade functions. The eight LEs can be used to create medium-sized blocks of logic—such as 8-bit counters, address decoders, or state machines—or combined across LABs to create larger logic blocks. Each LAB represents about 96 usable gates of logic.

Signal interconnections within FLEX 10KE devices (as well as to and from device pins) are provided by the FastTrack Interconnect routing structure, which is a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect routing structure. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an output or input register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. As inputs, they provide setup times as low as 0.9 ns and hold times of 0 ns. As outputs, these registers provide clock-to-output times as low as 3.0 ns. IOEs provide a variety of features, such as JTAG BST support, slew-rate control, tri-state buffers, and open-drain outputs.

Figure 1 shows a block diagram of the FLEX 10KE architecture. Each group of LEs is combined into an LAB; groups of LABs are arranged into rows and columns. Each row also contains a single EAB. The LABs and EABs are interconnected by the FastTrack Interconnect routing structure. IOEs are located at the end of each row and column of the FastTrack Interconnect routing structure.

***Figure 1. FLEX 10KE Device Block Diagram***

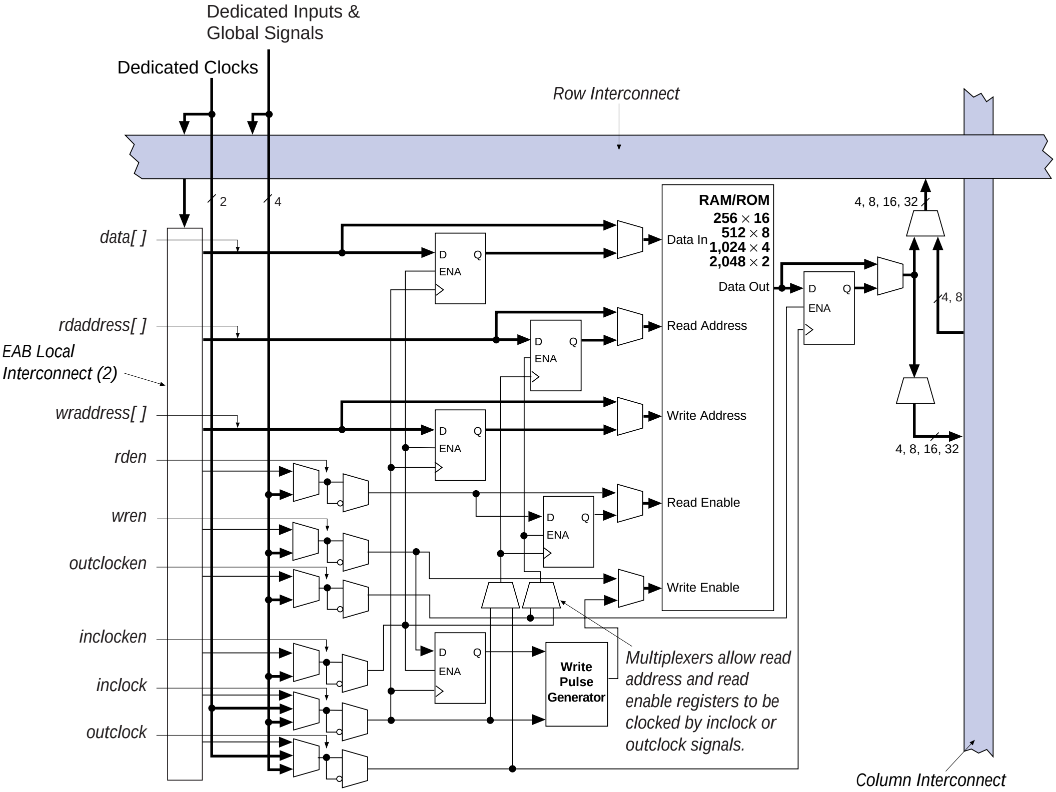


FLEX 10KE devices provide six dedicated inputs that drive the flipflops' control inputs and ensure the efficient distribution of high-speed, low-skew (less than 1.5 ns) control signals. These signals use dedicated routing channels that provide shorter delays and lower skews than the FastTrack Interconnect routing structure. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or an internally generated asynchronous clear signal that clears many registers in the device.

The EAB can also be used for bidirectional, dual-port memory applications where two ports read or write simultaneously. To implement this type of dual-port memory, two EABs are used to support two simultaneous read or writes.

Alternatively, one clock and clock enable can be used to control the input registers of the EAB, while a different clock and clock enable control the output registers (see Figure 2).

***Figure 2. FLEX 10KE Device in Dual-Port RAM Mode*** *Notes (1)*



***Notes:***

(1) All registers can be asynchronously cleared by EAB local interconnect signals, global signals, or the chip-wide reset.

(2) EPF10K30E and EPF10K50E devices have 88 EAB local interconnect channels; EPF10K100E, EPF10K130E, and EPF10K200E devices have 104 EAB local interconnect channels.

EABs provide flexible options for driving and controlling clock signals. Different clocks and clock enables can be used for reading and writing to the EAB. Registers can be independently inserted on the data input, EAB output, write address, write enable signals, read address, and read enable signals. The global signals and the EAB local interconnect can drive write enable, read enable, and clock enable signals. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control write enable, read enable, clear, clock, and clock enable signals.

An EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs (see Figures 2 and 4). The column interconnect, which is adjacent to the EAB, has twice as many channels as other columns in the device.

## Logic Array Block

An LAB consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure to the FLEX 10KE architecture, facilitating efficient routing with optimum device utilization and high performance (see Figure 7).

### *Cascade Chain*

With the cascade chain, the FLEX 10KE architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. An a delay as low as 0.6 ns per LE, each additional LE provides four more inputs to the effective width of a function. Cascade chain logic can be created automatically by the Altera Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than eight bits are implemented automatically by linking several LABs together. For easier routing, a long cascade chain skips every other LAB in a row. A cascade chain longer than one LAB skips either from even-numbered LAB to even-numbered LAB, or from odd-numbered LAB to odd-numbered LAB (e.g., the last LE of the first LAB in a row cascades to the first LE of the third LAB). The cascade chain does not cross the center of the row (e.g., in the EPF10K50E device, the cascade chain stops at the eighteenth LAB and a new one begins at the nineteenth LAB). This break is due to the EAB's placement in the middle of the row.

Figure 10 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of 4*n* variables implemented with *n* LEs. The LE delay is 0.9 ns; the cascade chain delay is 0.6 ns. With the cascade chain, 2.7 ns are needed to decode a 16-bit address.

***Figure 10. FLEX 10KE Cascade Chain Operation***

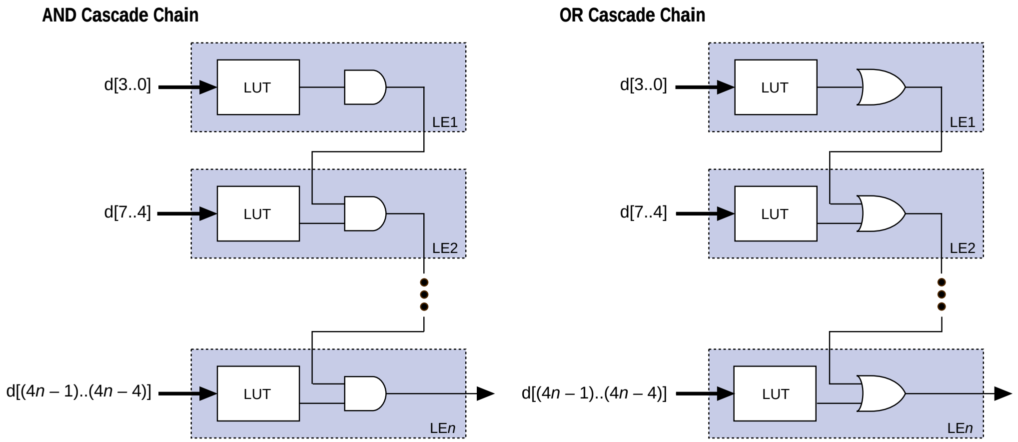
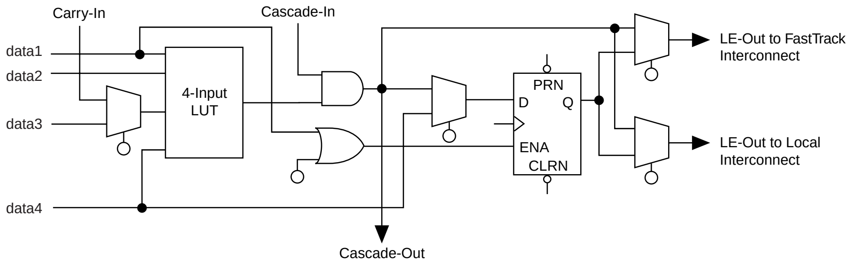


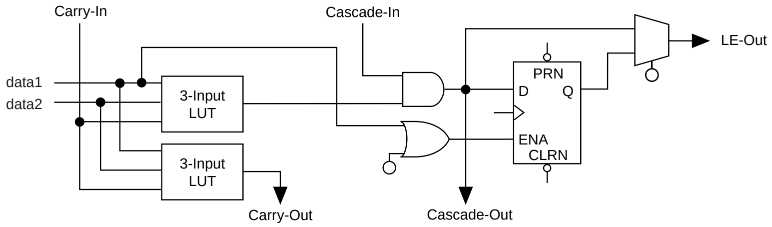
Figure 11 shows the LE operating modes.

*Figure 11. FLEX 10KE LE Operating Modes*

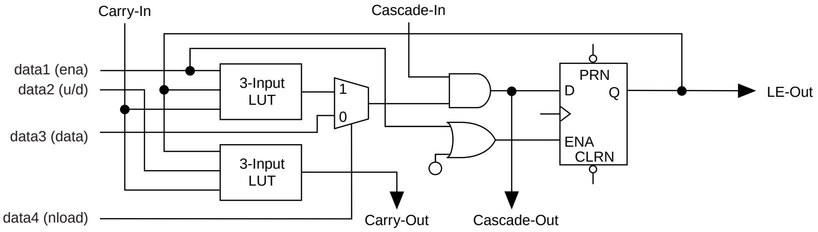
**Normal Mode**



**Arithmetic Mode**



**Up/Down Counter Mode**



**Clearable Counter Mode**

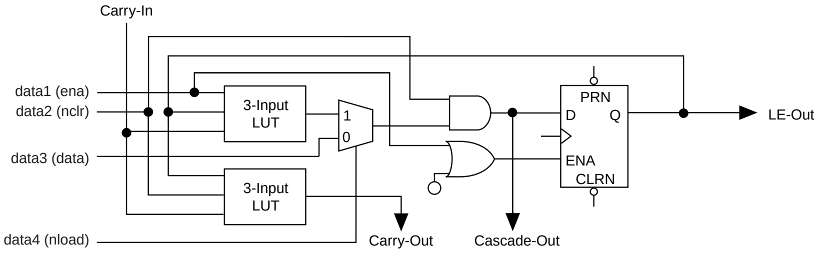


*Table 9. Peripheral Bus Sources for EPF10K100E, EPF10K130E, EPF10K200E & EPF10K200S Devices*

| Peripheral Control Signal | EPF10K100E | EPF10K130E | EPF10K200E<br>EPF10K200S |
|---|---|---|---|
| `OE0` | Row A | Row C | Row G |
| `OE1` | Row C | Row E | Row I |
| `OE2` | Row E | Row G | Row K |
| `OE3` | Row L | Row N | Row R |
| `OE4` | Row I | Row K | Row O |
| `OE5` | Row K | Row M | Row Q |
| `CLKENA0/CLK0/GLOBAL0` | Row F | Row H | Row L |
| `CLKENA1/OE6/GLOBAL1` | Row D | Row F | Row J |
| `CLKENA2/CLR0` | Row B | Row D | Row H |
| `CLKENA3/OE7/GLOBAL2` | Row H | Row J | Row N |
| `CLKENA4/CLR1` | Row J | Row L | Row P |
| `CLKENA5/CLK1/GLOBAL3` | Row G | Row I | Row M |

Signals on the peripheral control bus can also drive the four global signals, referred to as `GLOBAL0` through `GLOBAL3` in Tables 8 and 9. An internally generated signal can drive a global signal, providing the same low-skew, low-delay characteristics as a signal driven by an input pin. An LE drives the global signal by driving a row line that drives the peripheral bus, which then drives the global signal. This feature is ideal for internally generated clear or clock signals with high fan-out. However, internally driven global signals offer no advantage over the general-purpose interconnect for routing data signals. The dedicated input pin should be driven to a known logic state (such as ground) and not be allowed to float.

The chip-wide output enable pin is an active-high pin (`DEV_OE`) that can be used to tri-state all pins on the device. This option can be set in the Altera software. On EPF10K50E and EPF10K200E devices, the built-in I/O pin pull-up resistors (which are active during configuration) are active when the chip-wide output enable pin is asserted. The registers in the IOE can also be reset by the chip-wide reset pin.

## ClockLock & ClockBoost Features

To support high-speed designs, FLEX 10KE devices offer optional ClockLock and ClockBoost circuitry containing a phase-locked loop (PLL) used to increase design speed and reduce resource usage. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by resource sharing within the device. The ClockBoost feature allows the designer to distribute a low-speed clock and multiply that clock on-device. Combined, the ClockLock and ClockBoost features provide significant improvements in system performance and bandwidth.

All FLEX 10KE devices, except EPF10K50E and EPF10K200E devices, support ClockLock and ClockBoost circuitry. EPF10K50S and EPF10K200S devices support this circuitry. Devices that support ClockLock and ClockBoost circuitry are distinguished with an “X” suffix in the ordering code; for instance, the EPF10K200SFC672-1X device supports this circuit.

The ClockLock and ClockBoost features in FLEX 10KE devices are enabled through the Altera software. External devices are not required to use these features. The output of the ClockLock and ClockBoost circuits is not available at any of the device pins.

The ClockLock and ClockBoost circuitry locks onto the rising edge of the incoming clock. The circuit output can drive the clock inputs of registers only; the generated clock cannot be gated or inverted.

The dedicated clock pin (`GCLK1`) supplies the clock to the ClockLock and ClockBoost circuitry. When the dedicated clock pin is driving the ClockLock or ClockBoost circuitry, it cannot drive elsewhere in the device.

For designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to the `GCLK1` pin. In the Altera software, the `GCLK1` pin can feed both the ClockLock and ClockBoost circuitry in the FLEX 10KE device. However, when both circuits are used, the other clock pin cannot be used.

Tables 12 and 13 summarize the ClockLock and ClockBoost parameters for -1 and -2 speed-grade devices, respectively.

*Table 12. ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_R$ | Input rise time | | | | 5 | ns |
| $t_F$ | Input fall time | | | | 5 | ns |
| $t_{INDUTY}$ | Input duty cycle | | 40 | | 60 | % |
| $f_{CLK1}$ | Input clock frequency (ClockBoost clock multiplication factor equals 1) | | 25 | | 180 | MHz |
| $f_{CLK2}$ | Input clock frequency (ClockBoost clock multiplication factor equals 2) | | 16 | | 90 | MHz |
| $f_{CLKDEV}$ | Input deviation from user specification in the MAX+PLUS II software *(1)* | | | | 25,000 *(2)* | PPM |
| $t_{INCLKSTB}$ | Input clock stability (measured between adjacent clocks) | | | | 100 | ps |
| $t_{LOCK}$ | Time required for ClockLock or ClockBoost to acquire lock *(3)* | | | | 10 | µs |
| $t_{JITTER}$ | Jitter on ClockLock or ClockBoost-generated clock *(4)* | $t_{INCLKSTB} < 100$ | | | 250 | ps |
| | | $t_{INCLKSTB} < 50$ | | | 200 *(4)* | ps |
| $t_{OUTDUTY}$ | Duty cycle for ClockLock or ClockBoost-generated clock | | 40 | 50 | 60 | % |

**Table 23. FLEX 10KE Device Capacitance** *Note (14)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 10 | pF |
| $C_{INCLK}$ | Input capacitance on dedicated clock pin | $V_{IN}$ = 0 V, f = 1.0 MHz | | 12 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 10 | pF |

***Notes to tables:***

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum $V_{CC}$ rise time is 100 ms, and $V_{CC}$ must rise monotonically.
(5) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.
(6) Typical values are for $T_A$ = 25° C, $V_{CCINT}$ = 2.5 V, and $V_{CCIO}$ = 2.5 V or 3.3 V.
(7) These values are specified under the FLEX 10KE Recommended Operating Conditions shown in Tables 20 and 21.
(8) The FLEX 10KE input buffers are compatible with 2.5-V, 3.3-V (LVTTL and LVCMOS), and 5.0-V TTL and CMOS signals. Additionally, the input buffers are 3.3-V PCI compliant when $V_{CCIO}$ and $V_{CCINT}$ meet the relationship shown in Figure 22.
(9) The $I_{OH}$ parameter refers to high-level TTL, PCI, or CMOS output current.
(10) The $I_{OL}$ parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(11) This value is specified for normal device operation. The value may vary during power-up.
(12) This parameter applies to -1 speed-grade commercial-temperature devices and -2 speed-grade-industrial temperature devices.
(13) Pin pull-up resistance values will be lower if the pin is driven higher than $V_{CCIO}$ by an external source.
(14) Capacitance is sample-tested only.

***Table 27. EAB Timing Macroparameters*** *Note (1), (6)*

| Symbol | Parameter | Conditions |
|---|---|---|
| $t_{EABAA}$ | EAB address access delay | |
| $t_{EABRCCOMB}$ | EAB asynchronous read cycle time | |
| $t_{EABRCREG}$ | EAB synchronous read cycle time | |
| $t_{EABWP}$ | EAB write pulse width | |
| $t_{EABWCCOMB}$ | EAB asynchronous write cycle time | |
| $t_{EABWCREG}$ | EAB synchronous write cycle time | |
| $t_{EABDD}$ | EAB data-in to data-out valid delay | |
| $t_{EABDATACO}$ | EAB clock-to-output delay when using output registers | |
| $t_{EABDATASU}$ | EAB data/address setup time before clock when using input register | |
| $t_{EABDATAH}$ | EAB data/address hold time after clock when using input register | |
| $t_{EABWESU}$ | EAB `WE` setup time before clock when using input register | |
| $t_{EABWEH}$ | EAB `WE` hold time after clock when using input register | |
| $t_{EABWDSU}$ | EAB data setup time before falling edge of write pulse when not using input registers | |
| $t_{EABWDH}$ | EAB data hold time after falling edge of write pulse when not using input registers | |
| $t_{EABWASU}$ | EAB address setup time before rising edge of write pulse when not using input registers | |
| $t_{EABWAH}$ | EAB address hold time after falling edge of write pulse when not using input registers | |
| $t_{EABWO}$ | EAB write enable to data output valid delay | |

***Table 33. EPF10K30E Device EAB Internal Microparameters*** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 1.7 | | 2.0 | | 2.3 | ns |
| $t_{EABDATA1}$ | | 0.6 | | 0.7 | | 0.8 | ns |
| $t_{EABWE1}$ | | 1.1 | | 1.3 | | 1.4 | ns |
| $t_{EABWE2}$ | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{EABRE1}$ | | 0.8 | | 0.9 | | 1.0 | ns |
| $t_{EABRE2}$ | | 0.4 | | 0.4 | | 0.5 | ns |
| $t_{EABCLK}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCO}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{EABBYPASS}$ | | 0.5 | | 0.6 | | 0.7 | ns |
| $t_{EABSU}$ | 0.9 | | 1.0 | | 1.2 | | ns |
| $t_{EABH}$ | 0.4 | | 0.4 | | 0.5 | | ns |
| $t_{EABCLR}$ | 0.3 | | 0.3 | | 0.3 | | ns |
| $t_{AA}$ | | 3.2 | | 3.8 | | 4.4 | ns |
| $t_{WP}$ | 2.5 | | 2.9 | | 3.3 | | ns |
| $t_{RP}$ | 0.9 | | 1.1 | | 1.2 | | ns |
| $t_{WDSU}$ | 0.9 | | 1.0 | | 1.1 | | ns |
| $t_{WDH}$ | 0.1 | | 0.1 | | 0.1 | | ns |
| $t_{WASU}$ | 1.7 | | 2.0 | | 2.3 | | ns |
| $t_{WAH}$ | 1.8 | | 2.1 | | 2.4 | | ns |
| $t_{RASU}$ | 3.1 | | 3.7 | | 4.2 | | ns |
| $t_{RAH}$ | 0.2 | | 0.2 | | 0.2 | | ns |
| $t_{WO}$ | | 2.5 | | 2.9 | | 3.3 | ns |
| $t_{DD}$ | | 2.5 | | 2.9 | | 3.3 | ns |
| $t_{EABOUT}$ | | 0.5 | | 0.6 | | 0.7 | ns |
| $t_{EABCH}$ | 1.5 | | 2.0 | | 2.3 | | ns |
| $t_{EABCL}$ | 2.5 | | 2.9 | | 3.3 | | ns |

***Table 37. EPF10K30E External Bidirectional Timing Parameters*** *Notes (1), (2)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ *(3)* | 2.8 | | 3.9 | | 5.2 | | ns |
| $t_{INHBIDIR}$ *(3)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSUBIDIR}$ *(4)* | 3.8 | | 4.9 | | – | | ns |
| $t_{INHBIDIR}$ *(4)* | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCOBIDIR}$ *(3)* | 2.0 | 4.9 | 2.0 | 5.9 | 2.0 | 7.6 | ns |
| $t_{XZBIDIR}$ *(3)* | | 6.1 | | 7.5 | | 9.7 | ns |
| $t_{ZXBIDIR}$ *(3)* | | 6.1 | | 7.5 | | 9.7 | ns |
| $t_{OUTCOBIDIR}$ *(4)* | 0.5 | 3.9 | 0.5 | 4.9 | – | – | ns |
| $t_{XZBIDIR}$ *(4)* | | 5.1 | | 6.5 | | – | ns |
| $t_{ZXBIDIR}$ *(4)* | | 5.1 | | 6.5 | | – | ns |

***Notes to tables:***

(1) All timing parameters are described in Tables 24 through 30 in this data sheet.
(2) These parameters are specified by characterization.
(3) This parameter is measured without the use of the ClockLock or ClockBoost circuits.
(4) This parameter is measured with the use of the ClockLock or ClockBoost circuits.

Tables 38 through 44 show EPF10K50E device internal and external timing parameters.

***Table 38. EPF10K50E Device LE Timing Microparameters (Part 1 of 2)*** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 0.6 | | 0.9 | | 1.3 | ns |
| $t_{CLUT}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{RLUT}$ | | 0.7 | | 0.8 | | 1.1 | ns |
| $t_{PACKED}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{EN}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{CICO}$ | | 0.2 | | 0.2 | | 0.3 | ns |
| $t_{CGEN}$ | | 0.5 | | 0.5 | | 0.8 | ns |
| $t_{CGENR}$ | | 0.2 | | 0.2 | | 0.3 | ns |
| $t_{CASC}$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{C}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{CO}$ | | 0.7 | | 0.7 | | 0.9 | ns |
| $t_{COMB}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{SU}$ | 0.7 | | 0.7 | | 0.8 | | ns |

**Table 40. EPF10K50E Device EAB Internal Microparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 1.7 | | 2.0 | | 2.7 | ns |
| $t_{EABDATA1}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{EABWE1}$ | | 1.1 | | 1.3 | | 1.8 | ns |
| $t_{EABWE2}$ | | 0.4 | | 0.4 | | 0.6 | ns |
| $t_{EABRE1}$ | | 0.8 | | 0.9 | | 1.2 | ns |
| $t_{EABRE2}$ | | 0.4 | | 0.4 | | 0.6 | ns |
| $t_{EABCLK}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCO}$ | | 0.3 | | 0.3 | | 0.5 | ns |
| $t_{EABBYPASS}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{EABSU}$ | 0.9 | | 1.0 | | 1.4 | | ns |
| $t_{EABH}$ | 0.4 | | 0.4 | | 0.6 | | ns |
| $t_{EABCLR}$ | 0.3 | | 0.3 | | 0.5 | | ns |
| $t_{AA}$ | | 3.2 | | 3.8 | | 5.1 | ns |
| $t_{WP}$ | 2.5 | | 2.9 | | 3.9 | | ns |
| $t_{RP}$ | 0.9 | | 1.1 | | 1.5 | | ns |
| $t_{WDSU}$ | 0.9 | | 1.0 | | 1.4 | | ns |
| $t_{WDH}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{WASU}$ | 1.7 | | 2.0 | | 2.7 | | ns |
| $t_{WAH}$ | 1.8 | | 2.1 | | 2.9 | | ns |
| $t_{RASU}$ | 3.1 | | 3.7 | | 5.0 | | ns |
| $t_{RAH}$ | 0.2 | | 0.2 | | 0.3 | | ns |
| $t_{WO}$ | | 2.5 | | 2.9 | | 3.9 | ns |
| $t_{DD}$ | | 2.5 | | 2.9 | | 3.9 | ns |
| $t_{EABOUT}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{EABCH}$ | 1.5 | | 2.0 | | 2.5 | | ns |
| $t_{EABCL}$ | 2.5 | | 2.9 | | 3.9 | | ns |

**Table 45. EPF10K100E Device LE Timing Microparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CGENR}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CASC}$ | | 0.6 | | 0.9 | | 1.2 | ns |
| $t_C$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{CO}$ | | 0.6 | | 0.8 | | 1.1 | ns |
| $t_{COMB}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{SU}$ | 0.4 | | 0.6 | | 0.7 | | ns |
| $t_H$ | 0.5 | | 0.7 | | 0.9 | | ns |
| $t_{PRE}$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{CLR}$ | | 0.8 | | 1.0 | | 1.4 | ns |
| $t_{CH}$ | 1.5 | | 2.0 | | 2.5 | | ns |
| $t_{CL}$ | 1.5 | | 2.0 | | 2.5 | | ns |

**Table 46. EPF10K100E Device IOE Timing Microparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 1.7 | | 2.0 | | 2.6 | ns |
| $t_{IOC}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{IOCO}$ | | 1.4 | | 1.6 | | 2.1 | ns |
| $t_{IOCOMB}$ | | 0.5 | | 0.7 | | 0.9 | ns |
| $t_{IOSU}$ | 0.8 | | 1.0 | | 1.3 | | ns |
| $t_{IOH}$ | 0.7 | | 0.9 | | 1.2 | | ns |
| $t_{IOCLR}$ | | 0.5 | | 0.7 | | 0.9 | ns |
| $t_{OD1}$ | | 3.0 | | 4.2 | | 5.6 | ns |
| $t_{OD2}$ | | 3.0 | | 4.2 | | 5.6 | ns |
| $t_{OD3}$ | | 4.0 | | 5.5 | | 7.3 | ns |
| $t_{XZ}$ | | 3.5 | | 4.6 | | 6.1 | ns |
| $t_{ZX1}$ | | 3.5 | | 4.6 | | 6.1 | ns |
| $t_{ZX2}$ | | 3.5 | | 4.6 | | 6.1 | ns |
| $t_{ZX3}$ | | 4.5 | | 5.9 | | 7.8 | ns |
| $t_{INREG}$ | | 2.0 | | 2.6 | | 3.5 | ns |
| $t_{IOFD}$ | | 0.5 | | 0.8 | | 1.2 | ns |
| $t_{INCOMB}$ | | 0.5 | | 0.8 | | 1.2 | ns |

***Table 47. EPF10K100E Device EAB Internal Microparameters*** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 1.5 | | 2.0 | | 2.6 | ns |
| $t_{EABDATA1}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABWE1}$ | | 1.5 | | 2.0 | | 2.6 | ns |
| $t_{EABWE2}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{EABRE1}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{EABRE2}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCLK}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCO}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{EABBYPASS}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{EABSU}$ | 0.8 | | 1.0 | | 1.4 | | ns |
| $t_{EABH}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{EABCLR}$ | 0.3 | | 0.4 | | 0.5 | | ns |
| $t_{AA}$ | | 4.0 | | 5.1 | | 6.6 | ns |
| $t_{WP}$ | 2.7 | | 3.5 | | 4.7 | | ns |
| $t_{RP}$ | 1.0 | | 1.3 | | 1.7 | | ns |
| $t_{WDSU}$ | 1.0 | | 1.3 | | 1.7 | | ns |
| $t_{WDH}$ | 0.2 | | 0.2 | | 0.3 | | ns |
| $t_{WASU}$ | 1.6 | | 2.1 | | 2.8 | | ns |
| $t_{WAH}$ | 1.6 | | 2.1 | | 2.8 | | ns |
| $t_{RASU}$ | 3.0 | | 3.9 | | 5.2 | | ns |
| $t_{RAH}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{WO}$ | | 1.5 | | 2.0 | | 2.6 | ns |
| $t_{DD}$ | | 1.5 | | 2.0 | | 2.6 | ns |
| $t_{EABOUT}$ | | 0.2 | | 0.3 | | 0.3 | ns |
| $t_{EABCH}$ | 1.5 | | 2.0 | | 2.5 | | ns |
| $t_{EABCL}$ | 2.7 | | 3.5 | | 4.7 | | ns |

***Table 48. EPF10K100E Device EAB Internal Timing Macroparameters*** *(Part 1 of 2)* *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABAA}$ | | 5.9 | | 7.6 | | 9.9 | ns |
| $t_{EABRCOMB}$ | 5.9 | | 7.6 | | 9.9 | | ns |
| $t_{EABRCREG}$ | 5.1 | | 6.5 | | 8.5 | | ns |
| $t_{EABWP}$ | 2.7 | | 3.5 | | 4.7 | | ns |

Tables 52 through 58 show EPF10K130E device internal and external timing parameters.

**Table 52. EPF10K130E Device LE Timing Microparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 0.6 | | 0.9 | | 1.3 | ns |
| $t_{CLUT}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{RLUT}$ | | 0.7 | | 0.9 | | 0.2 | ns |
| $t_{PACKED}$ | | 0.3 | | 0.5 | | 0.6 | ns |
| $t_{EN}$ | | 0.2 | | 0.3 | | 0.4 | ns |
| $t_{CICO}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.6 | | 0.8 | ns |
| $t_{CGENR}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{CASC}$ | | 0.6 | | 0.9 | | 1.2 | ns |
| $t_C$ | | 0.3 | | 0.5 | | 0.6 | ns |
| $t_{CO}$ | | 0.5 | | 0.7 | | 0.8 | ns |
| $t_{COMB}$ | | 0.3 | | 0.5 | | 0.6 | ns |
| $t_{SU}$ | 0.5 | | 0.7 | | 0.8 | | ns |
| $t_H$ | 0.6 | | 0.7 | | 1.0 | | ns |
| $t_{PRE}$ | | 0.9 | | 1.2 | | 1.6 | ns |
| $t_{CLR}$ | | 0.9 | | 1.2 | | 1.6 | ns |
| $t_{CH}$ | 1.5 | | 1.5 | | 2.5 | | ns |
| $t_{CL}$ | 1.5 | | 1.5 | | 2.5 | | ns |

**Table 53. EPF10K130E Device IOE Timing Microparameters** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 1.3 | | 1.5 | | 2.0 | ns |
| $t_{IOC}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{IOCO}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{IOCOMB}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{IOSU}$ | 1.0 | | 1.2 | | 1.6 | | ns |
| $t_{IOH}$ | 0.9 | | 0.9 | | 1.4 | | ns |
| $t_{IOCLR}$ | | 0.6 | | 0.8 | | 1.0 | ns |
| $t_{OD1}$ | | 2.8 | | 4.1 | | 5.5 | ns |
| $t_{OD2}$ | | 2.8 | | 4.1 | | 5.5 | ns |

***Table 71. EPF10K50S External Timing Parameters*** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 8.0 | | 9.5 | | 12.5 | ns |
| $t_{INSU}$ *(2)* | 2.4 | | 2.9 | | 3.9 | | ns |
| $t_{INH}$ *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ *(2)* | 2.0 | 4.3 | 2.0 | 5.2 | 2.0 | 7.3 | ns |
| $t_{INSU}$ *(3)* | 2.4 | | 2.9 | | | | ns |
| $t_{INH}$ *(3)* | 0.0 | | 0.0 | | | | ns |
| $t_{OUTCO}$ *(3)* | 0.5 | 3.3 | 0.5 | 4.1 | | | ns |
| $t_{PCISU}$ | 2.4 | | 2.9 | | – | | ns |
| $t_{PCIH}$ | 0.0 | | 0.0 | | – | | ns |
| $t_{PCICO}$ | 2.0 | 6.0 | 2.0 | 7.7 | – | – | ns |

***Table 72. EPF10K50S External Bidirectional Timing Parameters*** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ *(2)* | 2.7 | | 3.2 | | 4.3 | | ns |
| $t_{INHBIDIR}$ *(2)* | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INHBIDIR}$ *(3)* | 0.0 | | 0.0 | | – | | ns |
| $t_{INSUBIDIR}$ *(3)* | 3.7 | | 4.2 | | – | | ns |
| $t_{OUTCOBIDIR}$ *(2)* | 2.0 | 4.5 | 2.0 | 5.2 | 2.0 | 7.3 | ns |
| $t_{XZBIDIR}$ *(2)* | | 6.8 | | 7.8 | | 10.1 | ns |
| $t_{ZXBIDIR}$ *(2)* | | 6.8 | | 7.8 | | 10.1 | ns |
| $t_{OUTCOBIDIR}$ *(3)* | 0.5 | 3.5 | 0.5 | 4.2 | – | – | |
| $t_{XZBIDIR}$ *(3)* | | 6.8 | | 8.4 | | – | ns |
| $t_{ZXBIDIR}$ *(3)* | | 6.8 | | 8.4 | | – | ns |

***Notes to tables:***

(1) All timing parameters are described in Tables 24 through 30.
(2) This parameter is measured without use of the ClockLock or ClockBoost circuits.
(3) This parameter is measured with use of the ClockLock or ClockBoost circuits

***Table 74. EPF10K200S Device IOE Timing Microparameters (Part 2 of 2)*** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ZX2}$ | | 4.5 | | 4.8 | | 6.6 | ns |
| $t_{ZX3}$ | | 6.6 | | 7.6 | | 10.1 | ns |
| $t_{INREG}$ | | 3.7 | | 5.7 | | 7.7 | ns |
| $t_{IOFD}$ | | 1.8 | | 3.4 | | 4.0 | ns |
| $t_{INCOMB}$ | | 1.8 | | 3.4 | | 4.0 | ns |

***Table 75. EPF10K200S Device EAB Internal Microparameters*** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABDATA1}$ | | 1.8 | | 2.4 | | 3.2 | ns |
| $t_{EABDATA1}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{EABWE1}$ | | 1.1 | | 1.7 | | 2.3 | ns |
| $t_{EABWE2}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABRE1}$ | | 0 | | 0 | | 0 | ns |
| $t_{EABRE2}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{EABCLK}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{EABCO}$ | | 0.8 | | 0.9 | | 1.2 | ns |
| $t_{EABBYPASS}$ | | 0.0 | | 0.1 | | 0.1 | ns |
| $t_{EABSU}$ | 0.7 | | 1.1 | | 1.5 | | ns |
| $t_{EABH}$ | 0.4 | | 0.5 | | 0.6 | | ns |
| $t_{EABCLR}$ | 0.8 | | 0.9 | | 1.2 | | ns |
| $t_{AA}$ | | 2.1 | | 3.7 | | 4.9 | ns |
| $t_{WP}$ | 2.1 | | 4.0 | | 5.3 | | ns |
| $t_{RP}$ | 1.1 | | 1.1 | | 1.5 | | ns |
| $t_{WDSU}$ | 0.5 | | 1.1 | | 1.5 | | ns |
| $t_{WDH}$ | 0.1 | | 0.1 | | 0.1 | | ns |
| $t_{WASU}$ | 1.1 | | 1.6 | | 2.1 | | ns |
| $t_{WAH}$ | 1.6 | | 2.5 | | 3.3 | | ns |
| $t_{RASU}$ | 1.6 | | 2.6 | | 3.5 | | ns |
| $t_{RAH}$ | 0.1 | | 0.1 | | 0.2 | | ns |
| $t_{WO}$ | | 2.0 | | 2.4 | | 3.2 | ns |
| $t_{DD}$ | | 2.0 | | 2.4 | | 3.2 | ns |
| $t_{EABOUT}$ | | 0.0 | | 0.1 | | 0.1 | ns |
| $t_{EABCH}$ | 1.5 | | 2.0 | | 2.5 | | ns |
| $t_{EABCL}$ | 2.1 | | 2.8 | | 3.8 | | ns |

***Table 76. EPF10K200S Device EAB Internal Timing Macroparameters*** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{EABAA}$ | | 3.9 | | 6.4 | | 8.4 | ns |
| $t_{EABRCOMB}$ | 3.9 | | 6.4 | | 8.4 | | ns |
| $t_{EABRCREG}$ | 3.6 | | 5.7 | | 7.6 | | ns |
| $t_{EABWP}$ | 2.1 | | 4.0 | | 5.3 | | ns |
| $t_{EABWCOMB}$ | 4.8 | | 8.1 | | 10.7 | | ns |
| $t_{EABWCREG}$ | 5.4 | | 8.0 | | 10.6 | | ns |
| $t_{EABDD}$ | | 3.8 | | 5.1 | | 6.7 | ns |
| $t_{EABDATACO}$ | | 0.8 | | 1.0 | | 1.3 | ns |
| $t_{EABDATASU}$ | 1.1 | | 1.6 | | 2.1 | | ns |
| $t_{EABDATAH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWESU}$ | 0.7 | | 1.1 | | 1.5 | | ns |
| $t_{EABWEH}$ | 0.4 | | 0.5 | | 0.6 | | ns |
| $t_{EABWDSU}$ | 1.2 | | 1.8 | | 2.4 | | ns |
| $t_{EABWDH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{EABWASU}$ | 1.9 | | 3.6 | | 4.7 | | ns |
| $t_{EABWAH}$ | 0.8 | | 0.5 | | 0.7 | | ns |
| $t_{EABWO}$ | | 3.1 | | 4.4 | | 5.8 | ns |

***Table 77. EPF10K200S Device Interconnect Timing Microparameters (Part 1 of 2)*** *Note (1)*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{DIN2IOE}$ | | 4.4 | | 4.8 | | 5.5 | ns |
| $t_{DIN2LE}$ | | 0.6 | | 0.6 | | 0.9 | ns |
| $t_{DIN2DATA}$ | | 1.8 | | 2.1 | | 2.8 | ns |
| $t_{DCLK2IOE}$ | | 1.7 | | 2.0 | | 2.8 | ns |
| $t_{DCLK2LE}$ | | 0.6 | | 0.6 | | 0.9 | ns |
| $t_{SAMELAB}$ | | 0.1 | | 0.1 | | 0.2 | ns |
| $t_{SAMEROW}$ | | 3.0 | | 4.6 | | 5.7 | ns |
| $t_{SAMECOLUMN}$ | | 3.5 | | 4.9 | | 6.4 | ns |
| $t_{DIFFROW}$ | | 6.5 | | 9.5 | | 12.1 | ns |
| $t_{TWOROWS}$ | | 9.5 | | 14.1 | | 17.8 | ns |
| $t_{LEPERIPH}$ | | 5.5 | | 6.2 | | 7.2 | ns |
| $t_{LABCARRY}$ | | 0.3 | | 0.1 | | 0.2 | ns |