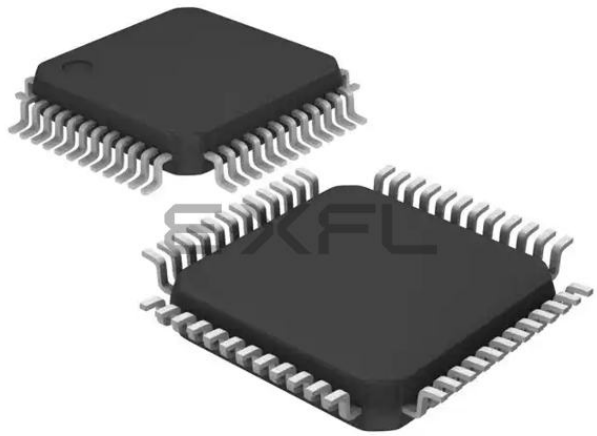

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800EX
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f84441vlf

- Operating characteristics
  - Single supply: 3.0 V to 3.6 V
  - 5 V–tolerant I/O

- LQFP packages:
  - 48-pin
  - 64-pin

Table 1. 56F844x/5x/7x Family (continued)

Part Number	MC56F84																	
	789	786	769	766	763	553	550	543	540	587	585	567	565	462	452	451	442	441
Standard channels	4	1	4	1	1	1	0	1	0	2x 12	1x 12, 1x9	2x 12	1x 12, 1x9	1x9	1x9	1x6	1x9	1x6
PWMB with input capture: Standard channels	1x 12	1x7	1x 12	1x7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DAC	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0
Quad Decoder	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1
DMA	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
CMP	4	4	4	4	4	4	3	4	3	4	4	4	4	4	4	3	4	3
QSCI	3	3	3	3	2	2	2	2	2	3	3	3	3	2	2	2	2	2
QSPI	3	2	3	2	2	2	2	2	2	3	2	3	2	2	2	2	2	2
I2C/SMBus	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
FlexCAN	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
LQFP package pin count	100	80	100	80	64	64	48	64	48	100	80	100	80	64	64	48	64	48

1. This total assumes no FlexNVM is used with FlexRAM for EEPROM.

1.2 56800EX 32-bit Digital Signal Controller Core

- Efficient 32-bit 56800EX Digital Signal Processor (DSP) engine with modified dual Harvard architecture
  - Three internal address buses
  - Four internal data buses: two 32-bit primary buses, one 16-bit secondary data bus, and one 16-bit instruction bus
  - 32-bit data accesses
  - Support for concurrent instruction fetches in the same cycle and dual data accesses in the same cycle
  - 20 addressing modes
- As many as 60 million instructions per second (MIPS) at 60 MHz core frequency
- 162 basic instructions
- Instruction set supports both fractional arithmetic and integer arithmetic
- 32-bit internal primary data buses supporting 8-bit, 16-bit, and 32-bit data movement, addition, subtraction, and logical operation
- Single-cycle 16 × 16-bit -> 32-bit and 32 x 32-bit -> 64-bit multiplier-accumulator (MAC) with dual parallel moves

1.6.3 Inter-Module Crossbar and AND-OR-INVERT logic

- Provides generalized connections between and among on-chip peripherals: ADCs, 12-bit DAC, Comparators, Quad Timers, eFlexPWMs, PDBs, EWM, Quadrature Decoder, and select I/O pins
- User-defined input/output pins for all modules connected to crossbar
- DMA request and interrupt generation from crossbar
- Write-once protection for all registers
- AND-OR-INVERT function that provides a universal Boolean function generator using a four-term sum-of-products expression, with each product term containing true or complement values of the four selected inputs (A, B, C, D).

1.6.4 Comparator

- Full rail-to-rail comparison range
- Support for high speed mode and low speed mode
- Selectable input source includes external pins and internal DACs
- Programmable output polarity
- 6-bit programmable DAC as voltage reference per comparator
- Three programmable hysteresis levels
- Selectable interrupt on rising edge, falling edge, or toggle of comparator output

1.6.5 12-bit Digital-to-Analog Converter

- 12-bit resolution
- Powerdown mode
- Automatic mode allows the DAC to automatically generate pre-programmed output waveforms including square, triangle, and sawtooth waveforms for applications such as slope compensation
- Programmable period, update rate, and range
- Output can be routed to an internal comparator, ADC, or optionally off chip

1.6.6 Quad Timer

- Four 16-bit up/down counters with programmable prescaler for each counter
- Operation modes: edge count, gated count, signed count, capture, compare, PWM, signal shot, single pulse, pulse string, cascaded, quadrature decode
- Programmable input filter
- Counting start can be synchronized across counters

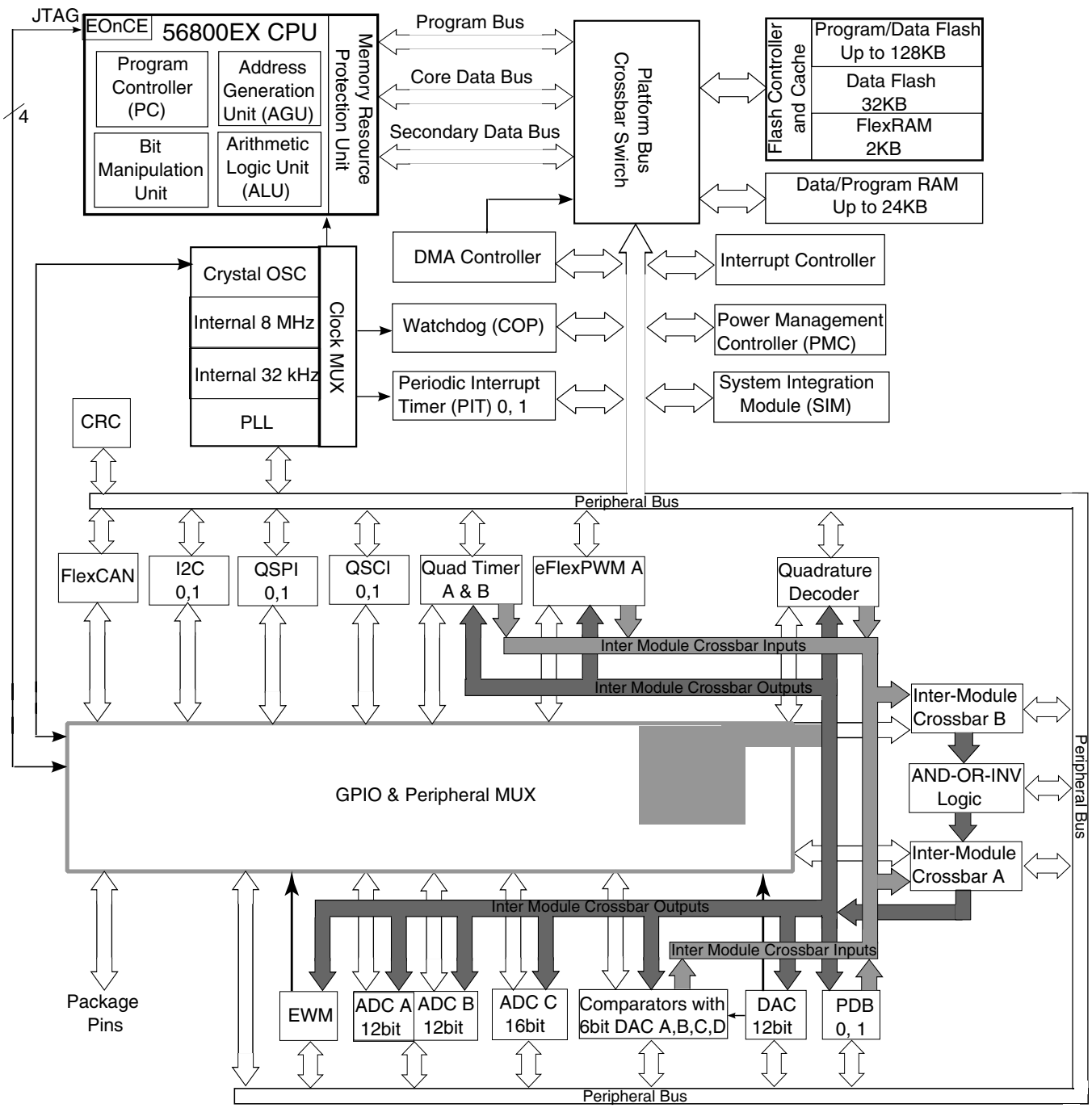

Figure 2. System Diagram

6.3 ESD handling ratings

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, use normal handling precautions to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM), and the charge device model (CDM).

All latch-up testing is in conformity with AEC-Q100 Stress Test Qualification.

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 3. ESD/Latch-up Protection

Characteristic[1]	Min	Max	Unit
ESD for Human Body Model (HBM)	–2000	+2000	V
ESD for Machine Model (MM)	–200	+200	V
ESD for Charge Device Model (CDM)	–500	+500	V
Latch-up current at TA= 85°C (I_{LAT})	–100	+100	mA

1. Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

6.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 4 may affect device reliability or cause permanent damage to the device.

Table 4. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic	Symbol	Notes[1]	Min	Max	Unit
Supply Voltage Range	V_{DD}		-0.3	4.0	V
Analog Supply Voltage Range	V_{DDA}		-0.3	4.0	V
ADC High Voltage Reference	V_{REFHx}		-0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		-0.3	0.3	V

Table continues on the next page...

Table 4. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V) (continued)

Characteristic	Symbol	Notes[1]	Min	Max	Unit
Digital Input Voltage Range	V_{IN}	Pin Groups 1, 2	-0.3	5.5	V
Oscillator Input Voltage Range	V_{OSC}	Pin Group 4	-0.4	4.0	V
Analog Input Voltage Range	V_{INA}	Pin Group 3	-0.3	4.0	V
Input clamp current, per pin (V_{IN} < V_{SS} - 0.3 V)[2, 3]	V_{IC}		—	-5.0	mA
Output clamp current, per pin[4]	V_{OC}		—	±20.0	mA
Contiguous pin DC injection current—regional limit sum of 16 contiguous pins	I_{ICont}		-25	25	mA
Output Voltage Range (normal push-pull mode)	V_{OUT}	Pin Group 1	-0.3	4.0	V
Output Voltage Range (open drain mode)	V_{OUTOD}	Pin Group 2	-0.3	5.5	V
DAC Output Voltage Range	V_{OUT_DAC}	Pin Group 5	-0.3	4.0	V
Ambient Temperature Industrial	T_A		-40	105	°C
Storage Temperature Range (Extended Industrial)	T_{STG}		-55	150	°C

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$, GPIOA7
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC analog output
2. Continuous clamp current
3. All 5 volt tolerant digital I/O pins are internally clamped to VSS through a ESD protection diode. There is no diode connection to VDD. If VIN greater than VDIO_MIN (=VSS-0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required.
4. I/O is configured as push-pull mode.

7 General

7.1 General Characteristics

The device is fabricated in high-density, low-power CMOS with 5 V–tolerant TTL-compatible digital inputs. The term “5 V–tolerant” refers to the capability of an I/O pin, built on a 3.3 V–compatible process technology, to withstand a voltage up to 5.5 V without damaging the device.

5 V–tolerant I/O is desirable because many systems have a mixture of devices designed for 3.3 V and 5 V power supplies. In such systems, a bus may carry both 3.3 V– and 5 V–compatible I/O voltage levels (a standard 3.3 V I/O is designed to receive a maximum voltage of 3.3 V ± 10% during normal operation without causing damage). This 5 V–tolerant capability therefore offers the power savings of 3.3 V I/O levels combined with the ability to receive 5 V levels without damage.

Absolute maximum ratings in Table 4 are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this chapter apply over the temperature range of -40°C to 105°C ambient temperature over the following supply ranges: VSS = VSSA = 0 V, VDD = VDDA = 3.0 V to 3.6 V, CL ≤ 50 pF, f_{OP} = 60 MHz.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

7.2 AC Electrical Characteristics

Tests are conducted using the input levels specified in Table 7. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in Figure 3.

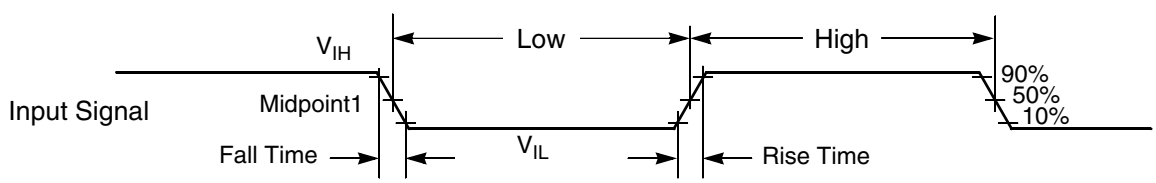

Figure 3. Input Signal Measurement References

Figure 4 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

7.4.1 Device clock specifications

Table 12. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYSCLK}	Device (system and core) clock frequency • using relaxation oscillator • using external clock source	 0.001 0	 60 60	MHz	
f_{IPBUS}	IP bus clock	—	60	MHz	

7.4.2 General Switching Timing

Table 13. Switching Timing

Symbol	Description	Min	Max	Unit	Notes
	GPIO pin interrupt pulse width[1] Synchronous path	1.5		IP Bus Clock Cycles	2
	Port rise and fall time (high drive strength), Slew disabled 2.7 ≤ V_{DD} ≤ 3.6V.	5.5	15.1	ns	3
	Port rise and fall time (high drive strength), Slew enabled 2.7 ≤ V_{DD} ≤ 3.6V.	1.5	6.8	ns	3
	Port rise and fall time (low drive strength). Slew disabled . 2.7 ≤ V_{DD} ≤ 3.6V	8.2	17.8	ns	4
	Port rise and fall time (low drive strength). Slew enabled . 2.7 ≤ V_{DD} ≤ 3.6V	3.2	9.2	ns	4

1. Applies to a pin only when it is configured as GPIO and configured to cause an interrupt by appropriately programming GPIOn_IPOLR and GPIOn_IENR.
2. The greater synchronous and asynchronous timing must be met.
3. 75 pF load
4. 15 pF load

7.5 Thermal specifications

7.5.1 Thermal operating requirements

Table 14. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature (extended industrial)	–40	105	°C

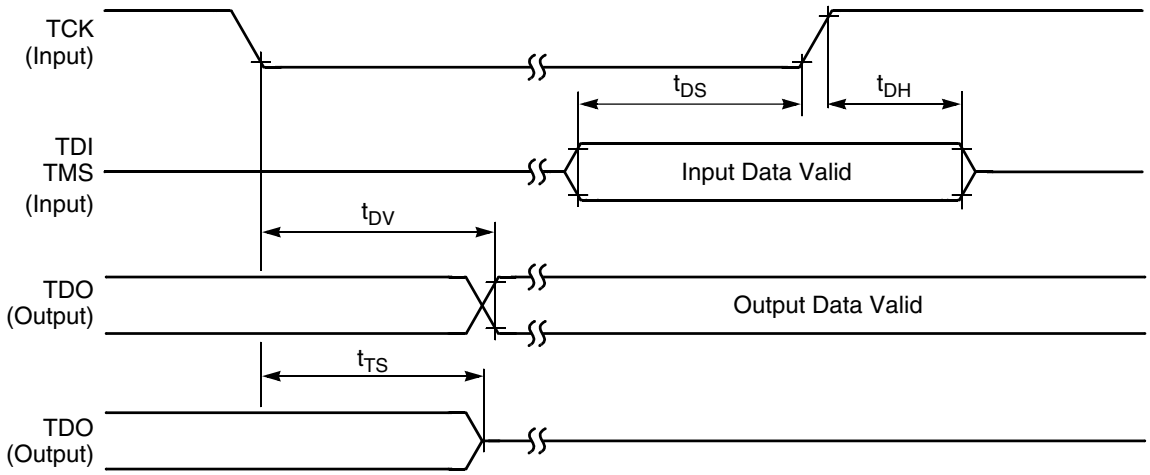

Figure 6. Test Access Port Timing Diagram

8.2 System modules

8.2.1 Voltage Regulator Specifications

The regulator supplies approximately 1.2 V to the MC56F84xxx's core logic. This regulator requires an external 2.2 µF capacitor on each V_{CAP} pin for proper operation. Ceramic and tantalum capacitors tend to provide better performance tolerances. The output voltage can be measured directly on the V_{CAP} pin. The specifications for this regulator are shown in Table 16.

Table 16. Regulator 1.2 V Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage[1]	V_{CAP}	—	1.22	—	V
Short Circuit Current[2]	I_{SS}	—	600	TBD	mA
Short Circuit Tolerance (V_{CAP} shorted to ground)	T_{RSC}	—	—	30	Minutes

1. Value is after trim
2. Guaranteed by design

Table 17. Bandgap Electrical Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Reference Voltage (after trim)	V_{REF}	—	1.21	—	V

8.3 Clock modules

8.3.3 External Crystal or Resonator Requirement

Table 20. Crystal or Resonator Requirement

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation	f_{XOSC}	4	8	16	MHz

8.3.4 Relaxation Oscillator Timing

Table 21. Relaxation Oscillator Electrical Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
8 MHz Output Frequency[1] RUN Mode • 0°C to 105°C • -40°C to 105°C Standby Mode (IRC trimmed @ 8 MHz) • -40°C to 105°C		 7.84 7.76 TBD	 8 8 TBD	 8.16 8.24 TBD	 MHz kHz
8 MHz Frequency Variation RUN Mode Due to temperature • 0°C to 105°C • -40°C to 105°C Standby Mode			 +/-1.5 +/- 1.5 Unspecified	 +/-2 +/-3	 %
32 kHz Output Frequency[2] RUN Mode • -40°C to 105°C		 TBD	 32	 TBD	 kHz
32 kHz Output Frequency Variation RUN Mode Due to temperature • -40°C to 105°C			 +/-2.5	 +/-4	 %
Stabilization Time • 8 MHz output[3] • 32 kHz output[4]	tstab		 0.12 14.4	 0.4 16.2	 µs
Output Duty Cycle		48	50	52	%

1. Frequency after application of 8 MHz trim
2. Frequency after application of 32 kHz trim
3. Standby to run mode transition
4. Power down to run mode transition

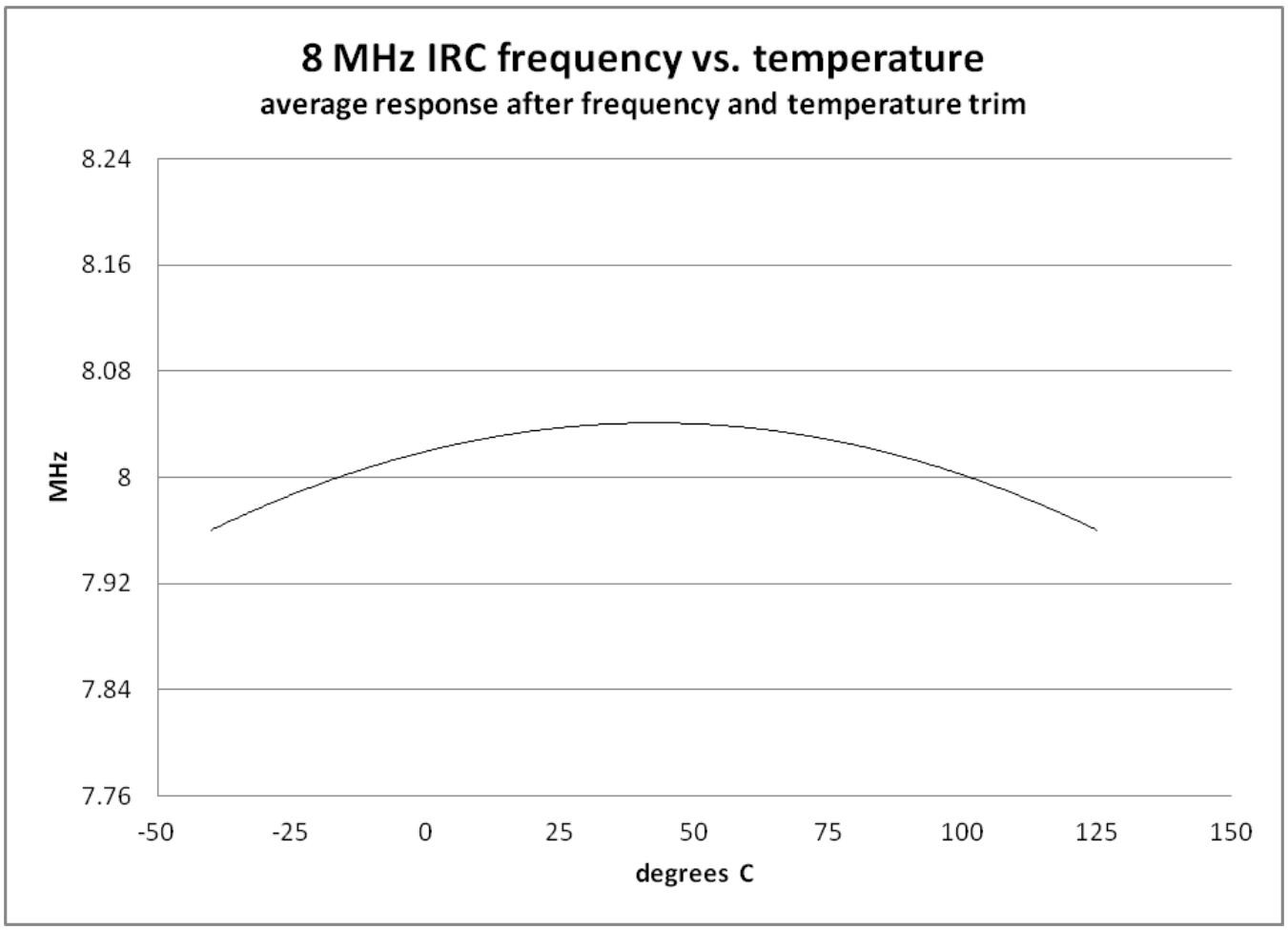

Figure 8. Relaxation Oscillator Temperature Variation (Typical) After Trim (Preliminary)

8.4 Memories and memory interfaces

8.4.1 Flash Memory Characteristics

Table 22. Flash Timing Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Longword Program high-voltage time[1]	thvpgm4	—	63	143	µs
Sector Erase high-voltage time [2]	thversscr	—	13	113	ms
Erase Block high-voltage time for 256 KB	thversblk256k	—	52	452	ms

1. There is additional overhead that is part of the programming sequence. See the device Reference Manual for detail.
2. Specifies page erase time.

7. For guidelines and examples of conversion rate calculation, download the ADC calculator tool: http://cache.freescale.com/files/soft_dev_tools/software/app_software/converters/ADC_CALCULATOR_CNV.zip?fpsp=1

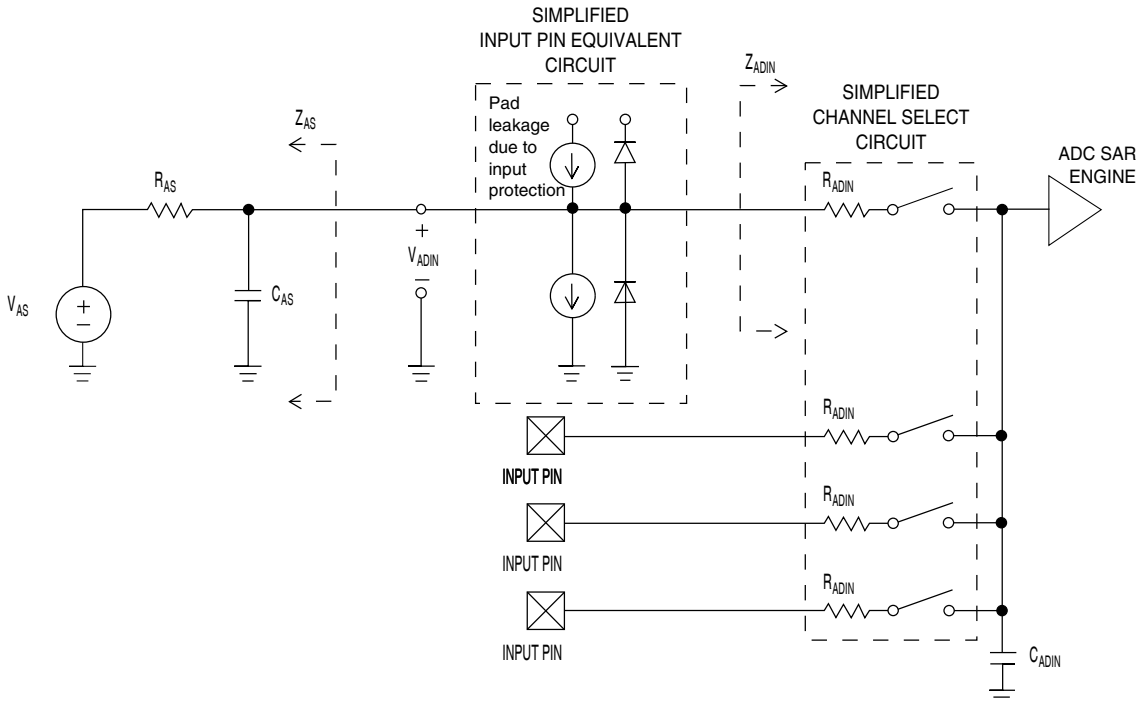

Figure 10. ADC input impedance equivalency diagram

8.5.2.2 16-bit ADC electrical characteristics

Table 27. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current			—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC=1, ADHSC=0	1.2	2.4	3.9	MHz	$t_{ADACK} = 1/f_{ADACK}$
		• ADLPC=1, ADHSC=1	3.0	4.0	7.3	MHz	
		• ADLPC=0, ADHSC=0	2.4	5.2	6.1	MHz	
		• ADLPC=0, ADHSC=1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12 bit modes	—	±4	±6.8	LSB[4]	5
		• <12 bit modes	—	±1.4	±2.1		
DNL	Differential non-linearity	• 16 bit modes	—	-1 to +4		LSB[4]	5
		• 12 bit modes	—	±0.7	TBD		
		• <12 bit modes	—	±0.2	-0.3 to 0.5		
INL	Integral non-linearity	• 16 bit modes	—	±7.0		LSB[4]	5
		• 12 bit modes	—	±1.0	-2.7 to +1.9		
		• <12 bit modes	—	±0.5	-0.7 to +0.5		

Table continues on the next page...

Table 27. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
E_{FS}	Full-scale error	• 12 bit modes • <12 bit modes	— —	-4 -1.4	-5.4 -1.8	LSB[4]	$V_{ADIN} = V_{DDA}$ 5
E_Q	Quantization error	• 16 bit modes • 12 bit modes	— —	-1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16 bit single-ended mode • Avg=32 • Avg=4 12 bit single-ended mode • Avg=32 • Avg=1	 12.2 11.4 	 13.9 13.1 10.8 10.2	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16 bit single-ended mode • Avg=32 12 bit single-ended mode • Avg=32	 — —	 -85 -74	 — —	 dB dB	7
SFDR	Spurious free dynamic range	16 bit single-ended mode • Avg=32 12 bit single-ended mode • Avg=32	 78 	 90 78	 — —	 dB dB	7
E_{IL}	Input leakage error		$I_{In} \times R_{AS}$			mV	I_{In} = leakage current (refer to the device's voltage and current operating ratings)
	Temp sensor slope	–40°C to 105°C	—	1.715	—	mV/°C	
V_{TEMP25}	Temp sensor voltage	25°C	—	722	—	mV	8

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit should be set, the HSC bit should be clear with 1MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock <16MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock <12MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock <12MHz.
8. System Clock = 4 MHz, ADC Clock = 2 MHz, AVG = Max, Long Sampling = Max

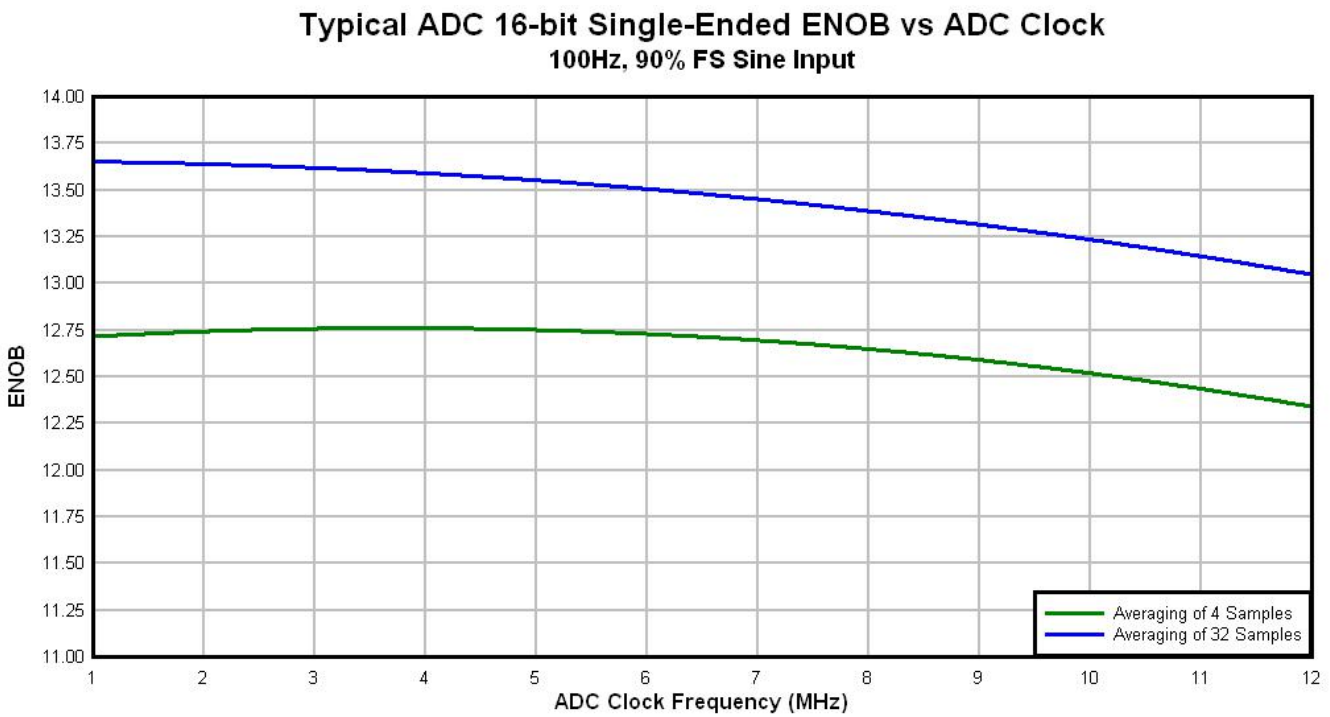

Figure 11. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

8.5.3 12-bit Digital-to-Analog Converter (DAC) Parameters

Table 28. DAC Parameters

Parameter	Conditions/Comments	Symbol	Min	Typ	Max	Unit
DC Specifications						
Resolution			12	12	12	bits
Settling time[1]	At output load RLD = 3 kΩ CLD = 400 pf		—	1		µs
Power-up time	Time from release of PWRDWN signal until DACOUT signal is valid	t_{DAPU}	—	—	11	µs
Accuracy						

Table continues on the next page...

8.7.2 Queued Serial Communication Interface (SCI) Timing

Parameters listed are guaranteed by design.

Table 33. SCI Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
Baud rate[1]	BR	—	(f_{MAX}/16)	Mbps	—
RXD pulse width	RXD_{PW}	0.965/BR	1.04/BR	ns	Figure 19
TXD pulse width	TXD_{PW}	0.965/BR	1.04/BR	ns	Figure 20
LIN Slave Mode					
Deviation of slave node clock from nominal clock rate before synchronization	$F_{TOL\_UNSYNCH}$	-14	14	%	—
Deviation of slave node clock relative to the master node clock after synchronization	F_{TOL_SYNCH}	-2	2	%	—
Minimum break character length	T_{BREAK}	13	—	Master node bit periods	—
		11	—	Slave node bit periods	—

1. f_{MAX} is the frequency of operation of the SCI clock in MHz, which can be selected system clock (max. 120 MHz depending on part number) or 2x system clock (max. 200 MHz) for the devices.

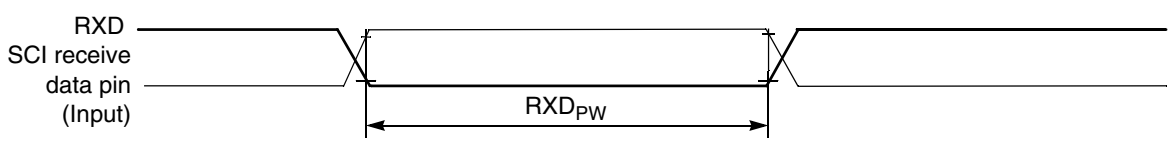

Figure 19. RXD Pulse Width

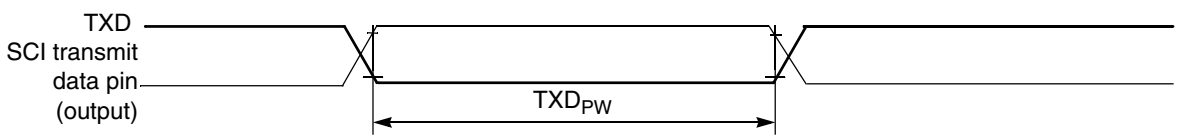

Figure 20. TXD Pulse Width

8.7.3 Freescale's Scalable Controller Area Network (FlexCAN)

Table 34. FlexCAN Timing Parameters

Characteristic	Symbol	Min	Max	Unit
Baud Rate	BR_{CAN}	—	1	Mbps
CAN Wakeup dominant pulse filtered	T_{WAKEUP}	—	2	µs
CAN Wakeup dominant pulse pass	T_{WAKEUP}	5	—	µs

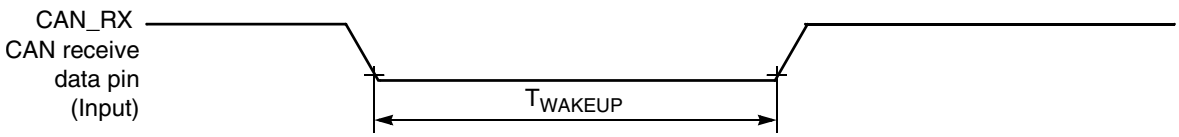

Figure 21. Bus Wake-up Detection

8.7.4 Inter-Integrated Circuit Interface (I^2C) Timing

Table 35. I^2C Timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I_2C bus devices	t_{HD}; DAT	0[1]	3.45[2]	0[3]	0.9[1]	µs
Data set-up time	t_{SU}; DAT	250[4]	—	100[2, 5]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[6]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[5]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
3. Input signal Slew = 10ns and Output Load = 50pf
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode I^2C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I^2C bus specification) before the SCL line is released.
6. C_b = total capacitance of the one bus line in pF.

64 LQFP	48 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
11	—	GPIOA5	GPIOA5	ANA5&ANC9			
12	8	GPIOA4	GPIOA4	ANA4&ANC8&CMPD_IN0			
13	9	GPIOA0	GPIOA0	ANA0&CMPA_IN3	CMPC_O		
14	10	GPIOA1	GPIOA1	ANA1&CMPA_IN0			
15	11	GPIOA2	GPIOA2	ANA2&VREFHA&CMPA_IN1			
16	12	GPIOA3	GPIOA3	ANA3&VREFLA&CMPA_IN2			
17	—	GPIOB7	GPIOB7	ANB7&ANC15&CMPB_IN2			
18	13	GPIOC5	GPIOC5	DACO	XB_IN7		
19	—	GPIOB6	GPIOB6	ANB6&ANC14&CMPB_IN1			
20	—	GPIOB5	GPIOB5	ANB5&ANC13&CMPC_IN2			
21	14	GPIOB4	GPIOB4	ANB4&ANC12&CMPC_IN1			
22	15	VDDA	VDDA				
23	16	VSSA	VSSA				
24	17	GPIOB0	GPIOB0	ANB0&CMPB_IN3			
25	18	GPIOB1	GPIOB1	ANB1&CMPB_IN0			
26	19	VCAP	VCAP				
27	20	GPIOB2	GPIOB2	ANB2&VREFHB&CMPC_IN3			
28	21	GPIOB3	GPIOB3	ANB3&VREFLB&CMPC_IN0			
29	—	VDD	VDD				
30	22	VSS	VSS				
31	23	GPIOC6	GPIOC6	TA2	XB_IN3	CMP_REF	
32	24	GPIOC7	GPIOC7	SS0_B	TXD0		
33	25	GPIOC8	GPIOC8	MISO0	RXD0	XB_IN9	
34	26	GPIOC9	GPIOC9	SCK0	XB_IN4		
35	27	GPIOC10	GPIOC10	MOSI0	XB_IN5	MISO0	
36	28	GPIOF0	GPIOF0	XB_IN6	TB2	SCK1	
37	29	GPIOC11	GPIOC11	CANTX	SCL1	TXD1	
38	30	GPIOC12	GPIOC12	CANRX	SDA1	RXD1	
39	—	GPIOF2	GPIOF2	SCL1	XB_OUT6		
40	—	GPIOF3	GPIOF3	SDA1	XB_OUT7		
41	—	GPIOF4	GPIOF4	TXD1	XB_OUT8		
42	—	GPIOF5	GPIOF5	RXD1	XB_OUT9		
43	31	VSS	VSS				
44	32	VDD	VDD				
45	33	GPIOE0	GPIOE0	PWMA_0B			
46	34	GPIOE1	GPIOE1	PWMA_0A			
47	35	GPIOE2	GPIOE2	PWMA_1B			
48	36	GPIOE3	GPIOE3	PWMA_1A			
49	37	GPIOC13	GPIOC13	TA3	XB_IN6	EWM_OUT_B	
50	38	GPIOF1	GPIOF1	CLKO1	XB_IN7	CMPD_O	
51	39	GPIOE4	GPIOE4	PWMA_2B	XB_IN2		

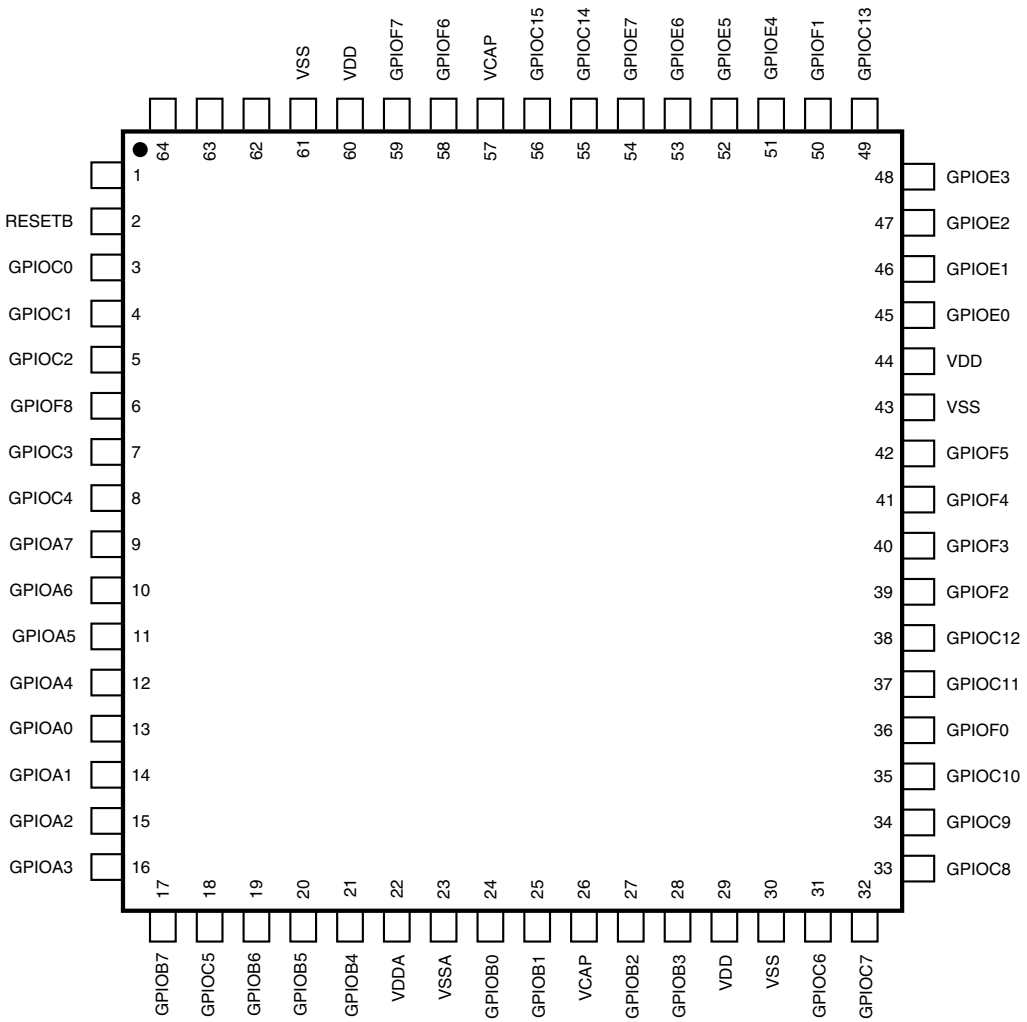

Figure 23. 64-pin LQFP

Table 36. Device Documentation

Topic	Description	Document Number
DSP56800E/DSP56800EX Reference Manual	Detailed description of the 56800EX family architecture, 32-bit digital signal controller core processor, and the instruction set	DSP56800ERM
MC56F844xx Reference Manual	Detailed functional description and programming model	MC56F844XXRM
Serial Bootloader User Guide	Detailed description of the Serial Bootloader in the DSC family of devices	TBD
MC56F844xx Data Sheet	Electrical and timing specifications, pin descriptions, and package information (this document)	MC56F844XX
MC56F84xxx Errata	Details any chip issues that might be present	MC56F84XXX_0N27E

13 Revision History

The following table summarizes changes to this document since the release of the previous version.

Table 37. Revision History

Rev.	Date	Substantial Changes
2	06/2012	This is the first publicly released version of this document.

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