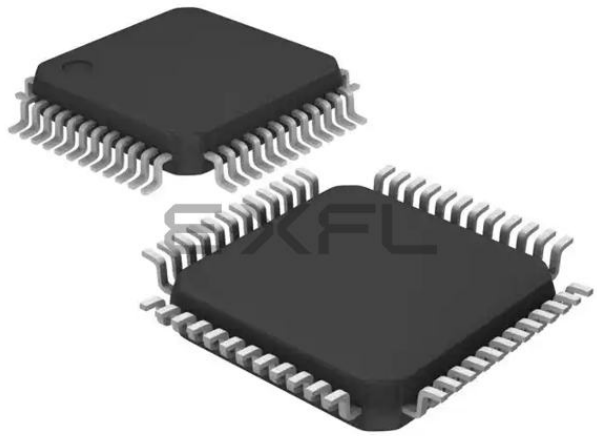


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 56800EX |
| Core Size | 32-Bit Single-Core |
| Speed | 60MHz |
| Connectivity | CANbus, I²C, LINbus, SCI, SPI |
| Peripherals | Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT |
| Number of I/O | 39 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 10x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f84441vlfr |

- Operating characteristics
  - Single supply: 3.0 V to 3.6 V
  - 5 V–tolerant I/O

- LQFP packages:
  - 48-pin
  - 64-pin

**Table 1. 56F844x/5x/7x Family (continued)**

| Part Number | MC56F84 | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 789 | 786 | 769 | 766 | 763 | 553 | 550 | 543 | 540 | 587 | 585 | 567 | 565 | 462 | 452 | 451 | 442 | 441 |
| Standard channels | 4 | 1 | 4 | 1 | 1 | 1 | 0 | 1 | 0 | 2x 12 | 1x 12, 1x9 | 2x 12 | 1x 12, 1x9 | 1x9 | 1x9 | 1x6 | 1x9 | 1x6 |
| PWMB with input capture: Standard channels | 1x 12 | 1x7 | 1x 12 | 1x7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| DAC | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Quad Decoder | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| DMA | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| CMP | 4 | 4 | 4 | 4 | 4 | 4 | 3 | 4 | 3 | 4 | 4 | 4 | 4 | 4 | 4 | 3 | 4 | 3 |
| QSCI | 3 | 3 | 3 | 3 | 2 | 2 | 2 | 2 | 2 | 3 | 3 | 3 | 3 | 2 | 2 | 2 | 2 | 2 |
| QSPI | 3 | 2 | 3 | 2 | 2 | 2 | 2 | 2 | 2 | 3 | 2 | 3 | 2 | 2 | 2 | 2 | 2 | 2 |
| I2C/SMBus | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| FlexCAN | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| LQFP package pin count | 100 | 80 | 100 | 80 | 64 | 64 | 48 | 64 | 48 | 100 | 80 | 100 | 80 | 64 | 64 | 48 | 64 | 48 |

1. This total assumes no FlexNVM is used with FlexRAM for EEPROM.

## 1.2 56800EX 32-bit Digital Signal Controller Core

- Efficient 32-bit 56800EX Digital Signal Processor (DSP) engine with modified dual Harvard architecture
  - Three internal address buses
  - Four internal data buses: two 32-bit primary buses, one 16-bit secondary data bus, and one 16-bit instruction bus
  - 32-bit data accesses
  - Support for concurrent instruction fetches in the same cycle and dual data accesses in the same cycle
  - 20 addressing modes
- As many as 60 million instructions per second (MIPS) at 60 MHz core frequency
- 162 basic instructions
- Instruction set supports both fractional arithmetic and integer arithmetic
- 32-bit internal primary data buses supporting 8-bit, 16-bit, and 32-bit data movement, addition, subtraction, and logical operation
- Single-cycle 16 × 16-bit -> 32-bit and 32 x 32-bit -> 64-bit multiplier-accumulator (MAC) with dual parallel moves

- Up to 16 KW FlexNVM, which can be used as additional program or data flash memory
- Up to 1 KW FlexRAM, which can be configured as enhanced EEPROM (used in conjunction with FlexNVM) or used as additional RAM

## 1.5 Interrupt Controller

- Five interrupt priority levels
  - Three user programmable priority levels for each interrupt source: level 0, 1, 2
  - Unmaskable level 3 interrupts include: illegal instruction, hardware stack overflow, misaligned data access, SWI3 instruction
  - Maskable level 3 interrupts include: EOnCE step counter, EOnCE breakpoint unit, EOnCE trace buffer
  - Lowest-priority software interrupt: level LP
- Support for nested interrupt: higher priority level interrupt request can interrupt lower priority interrupt subroutine
- Masking of interrupt priority level managed by the 56800EX core
- Two programmable fast interrupts that can be assigned to any interrupt source
- Notification to System Integration Module (SIM) to restart clock when in wait and stop states
- Ability to relocate interrupt vector table

## 1.6 Peripheral highlights

### 1.6.1 Enhanced Flex Pulse Width Modulator (eFlexPWM)

- Up to 12 output channels in each module
- 16 bits of resolution for center, edge aligned, and asymmetrical PWMs
- PWMA with accumulative fractional clock calculation
  - Accumulative fractional clock calculation improves the resolution of the PWM period and edge placement
  - Arbitrary PWM edge placement
  - Equivalent to 312 ps PWM frequency and duty-cycle resolution on average
- Each complementary pair can operate with its own PWM frequency base and deadtime values
  - 4 time base in each PWM module
  - Independent top and bottom deadtime insertion for each complementary pair
- PWM outputs can operate as complementary pairs or independent channels
- Independent control of both edges of each PWM output

### 1.6.13 Phase Locked Loop

- Wide programmable output frequency: 240 MHz to 400 MHz
- Input reference clock frequency: 8 MHz to 16 MHz
- Detection of loss of lock and loss of reference clock
- Ability to power down

### 1.6.14 Clock sources

#### 1.6.14.1 On-Chip Oscillators

- Tunable 8 MHz relaxation oscillator with 400 kHz at standby mode (divide-by-two output)
- 32 kHz low frequency clock as secondary clock source for COP, EWM, PIT

#### 1.6.14.2 Crystal Oscillator

- Support for both high ESR crystal oscillator (greater than 100-ohm ESR) and ceramic resonator
- 4 MHz to 16 MHz operating frequency

### 1.6.15 Cyclic Redundancy Check (CRC) Generator

- Hardware 16/32-bit CRC generator
- High-speed hardware CRC calculation
- Programmable initial seed value
- Programmable 16/32-bit polynomial
- Error detection for all single, double, odd, and most multi-bit errors
- Option to transpose input data or output data (CRC result) bitwise or bytewise,[1] which is required for certain CRC standards
- Option for inversion of final CRC result

### 1.6.16 General Purpose I/O (GPIO)

- 5 V tolerance
- Individual control of peripheral mode or GPIO mode for each pin
- Programmable push-pull or open drain output
- Configurable pullup or pulldown on all input pins

1. A bytewise transposition is not possible when accessing the CRC data register via 8-bit accesses. In this case, user software must perform the bytewise transposition.

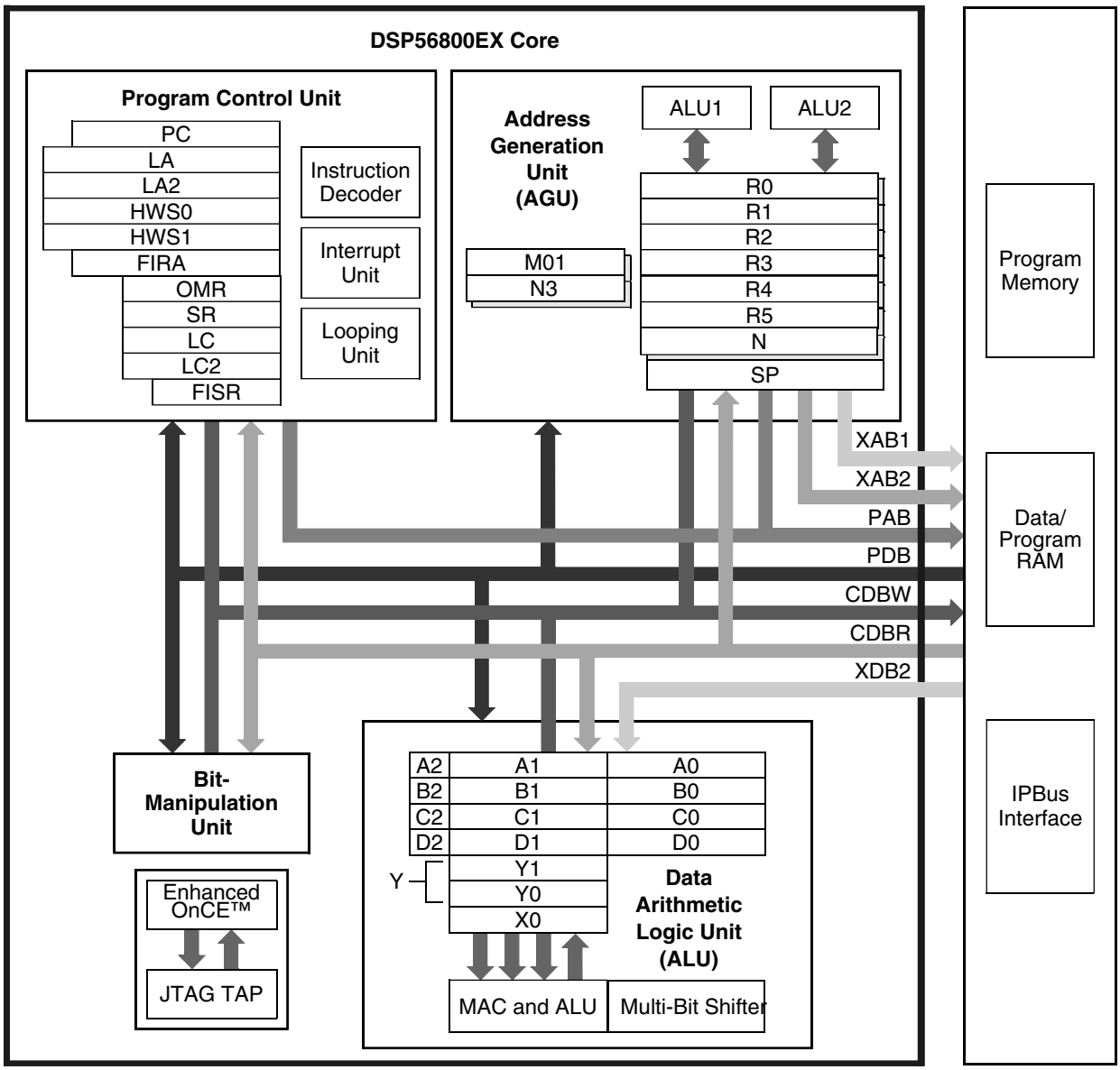



**Figure 1. 56800EX Basic Block Diagram**

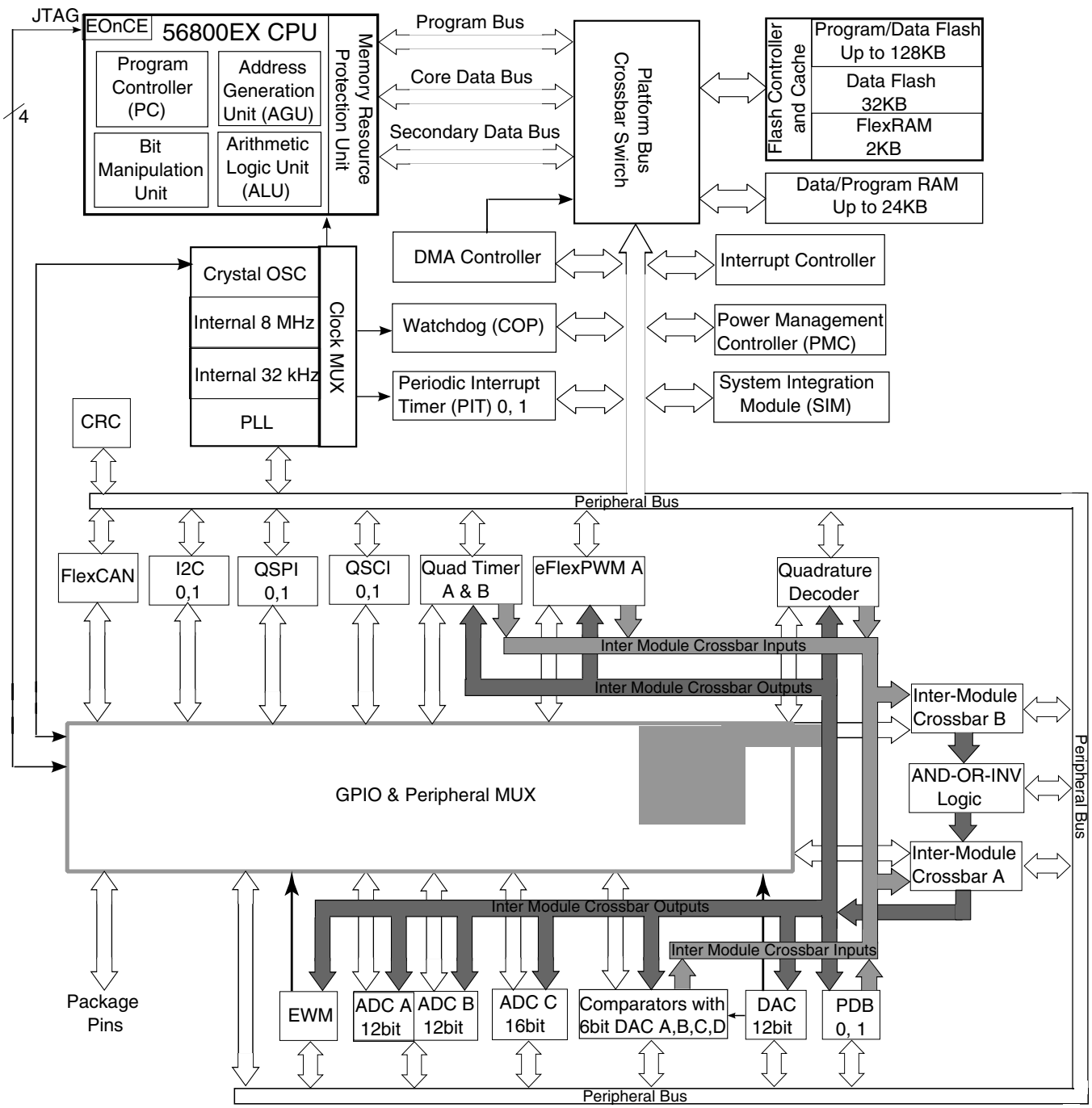



**Figure 2. System Diagram**

# 2 Signal groups

The input and output signals of the MC56F84xxx are organized into functional groups, as detailed in Table 2.

**Table 2. Functional Group Pin Allocations**

| Functional Group | Number of Pins in 48LQFP | Number of Pins in 64LQFP | Number of Pins in 80LQFP | Number of Pins in 100LQFP |
|---|---|---|---|---|
| Power Inputs ($V_{DD}$, $V_{DDA}$, $V_{CAP}$) | 5 | 6 | 6 | 6 |
| Ground ($V_{SS}$, $V_{SSA}$) | 4 | 4 | 4 | 4 |
| Reset | 1 | 1 | 1 | 1 |
| eFlexPWM ports, not including fault pins | 6 | 9 | N/A | N/A |
| Queued Serial Peripheral Interface (QSPI) ports | 5 | 6 | 8 | 15 |
| Queued Serial Communications Interface (QSCI) ports | 6 | 9 | 13 | 15 |
| Inter-Integrated Circuit ($I^2C$) interface ports | 4 | 6 | 6 | 6 |
| 12-bit Analog-to-Digital Converter (Cyclic ADC) inputs | 10 | 16 | 16 | 16 |
| 16-bit Analog-to-Digital Converter (SAR ADC) inputs | 2 | 8 | 10 | 16 |
| Analog Comparator inputs/outputs | 10/4 | 13/6 | 13/6 | 16/6 |
| 12-bit Digital-to-Analog output | 1 | 1 | 1 | 1 |
| Quad Timer Module (TMR) ports | 6 | 9 | 11 | 13 |
| Controller Area Network (FlexCAN) | 2 | 2 | 2 | 2 |
| Inter-Module Crossbar inputs/outputs | 12/2 | 16/6 | 19/17 | 25/19 |
| Clock inputs/outputs | 2/2 | 2/2 | 2/3 | 2/3 |
| JTAG / Enhanced On-Chip Emulation (EOnCE) | 4 | 4 | 4 | 4 |

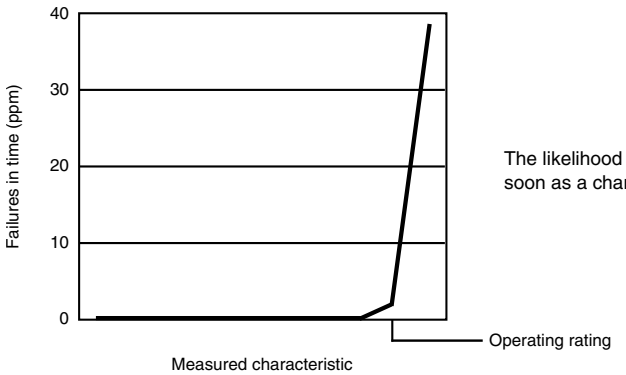
# 3 Ordering parts

## 3.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the following device numbers: MC56F84

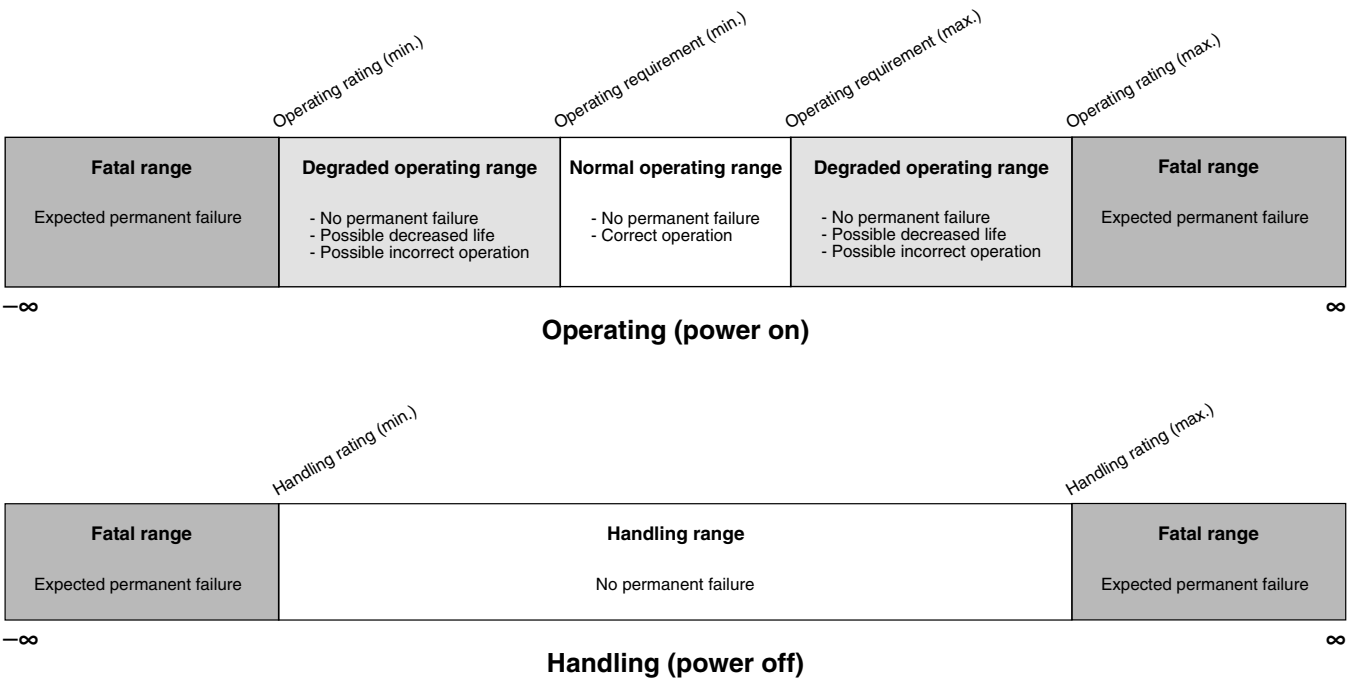
# 4 Part identification

## 5.5 Result of exceeding a rating




The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

## 5.6 Relationship between ratings and operating requirements




## 5.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

## 5.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient temperature | 25 | °C |
| $V_{DD}$ | 3.3 V supply voltage | 3.3 | V |

# 6 Ratings

## 6.1 Thermal handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature | –55 | 150 | °C | 1 |
| $T_{SDR}$ | Solder temperature, lead-free | — | 260 | °C | 2 |

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 6.2 Moisture handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| MSL | Moisture sensitivity level | — | 3 | — | 1 |

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 6.3 ESD handling ratings

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, use normal handling precautions to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM), and the charge device model (CDM).

All latch-up testing is in conformity with AEC-Q100 Stress Test Qualification.

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

**Table 3. ESD/Latch-up Protection**

| Characteristic[1] | Min | Max | Unit |
|---|---|---|---|
| ESD for Human Body Model (HBM) | –2000 | +2000 | V |
| ESD for Machine Model (MM) | –200 | +200 | V |
| ESD for Charge Device Model (CDM) | –500 | +500 | V |
| Latch-up current at TA= 85°C ($I_{LAT}$) | –100 | +100 | mA |

1. Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

## 6.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 4 may affect device reliability or cause permanent damage to the device.

**Table 4. Absolute Maximum Ratings ($V_{SS}$ = 0 V, $V_{SSA}$ = 0 V)**

| Characteristic | Symbol | Notes[1] | Min | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage Range | $V_{DD}$ | | -0.3 | 4.0 | V |
| Analog Supply Voltage Range | $V_{DDA}$ | | -0.3 | 4.0 | V |
| ADC High Voltage Reference | $V_{REFHx}$ | | -0.3 | 4.0 | V |
| Voltage difference $V_{DD}$ to $V_{DDA}$ | $\Delta V_{DD}$ | | -0.3 | 0.3 | V |
| Voltage difference $V_{SS}$ to $V_{SSA}$ | $\Delta V_{SS}$ | | -0.3 | 0.3 | V |

*Table continues on the next page...*

**Table 4. Absolute Maximum Ratings ($V_{SS}$ = 0 V, $V_{SSA}$ = 0 V) (continued)**

| Characteristic | Symbol | Notes[1] | Min | Max | Unit |
|---|---|---|---|---|---|
| Digital Input Voltage Range | $V_{IN}$ | Pin Groups 1, 2 | -0.3 | 5.5 | V |
| Oscillator Input Voltage Range | $V_{OSC}$ | Pin Group 4 | -0.4 | 4.0 | V |
| Analog Input Voltage Range | $V_{INA}$ | Pin Group 3 | -0.3 | 4.0 | V |
| Input clamp current, per pin ($V_{IN}$ < $V_{SS}$ - 0.3 V)[2, 3] | $V_{IC}$ | | — | -5.0 | mA |
| Output clamp current, per pin[4] | $V_{OC}$ | | — | ±20.0 | mA |
| Contiguous pin DC injection current—regional limit sum of 16 contiguous pins | $I_{ICont}$ | | -25 | 25 | mA |
| Output Voltage Range (normal push-pull mode) | $V_{OUT}$ | Pin Group 1 | -0.3 | 4.0 | V |
| Output Voltage Range (open drain mode) | $V_{OUTOD}$ | Pin Group 2 | -0.3 | 5.5 | V |
| DAC Output Voltage Range | $V_{OUT\_DAC}$ | Pin Group 5 | -0.3 | 4.0 | V |
| Ambient Temperature Industrial | $T_A$ | | -40 | 105 | °C |
| Storage Temperature Range (Extended Industrial) | $T_{STG}$ | | -55 | 150 | °C |

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$, GPIOA7
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC analog output
2. Continuous clamp current
3. All 5 volt tolerant digital I/O pins are internally clamped to VSS through a ESD protection diode. There is no diode connection to VDD. If VIN greater than VDIO_MIN (=VSS-0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required.
4. I/O is configured as push-pull mode.

# 7 General

## 7.1 General Characteristics

The device is fabricated in high-density, low-power CMOS with 5 V–tolerant TTL-compatible digital inputs. The term “5 V–tolerant” refers to the capability of an I/O pin, built on a 3.3 V–compatible process technology, to withstand a voltage up to 5.5 V without damaging the device.

5 V–tolerant I/O is desirable because many systems have a mixture of devices designed for 3.3 V and 5 V power supplies. In such systems, a bus may carry both 3.3 V– and 5 V–compatible I/O voltage levels (a standard 3.3 V I/O is designed to receive a maximum voltage of 3.3 V ± 10% during normal operation without causing damage). This 5 V–tolerant capability therefore offers the power savings of 3.3 V I/O levels combined with the ability to receive 5 V levels without damage.

### 7.5.2 Thermal attributes

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To account for $P_{I/O}$ in power calculations, determine the difference between actual pin voltage and $V_{SS}$ or $V_{DD}$ and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and $V_{SS}$ or $V_{DD}$ is very small.

See Thermal Design Considerations for more detail on thermal design considerations.

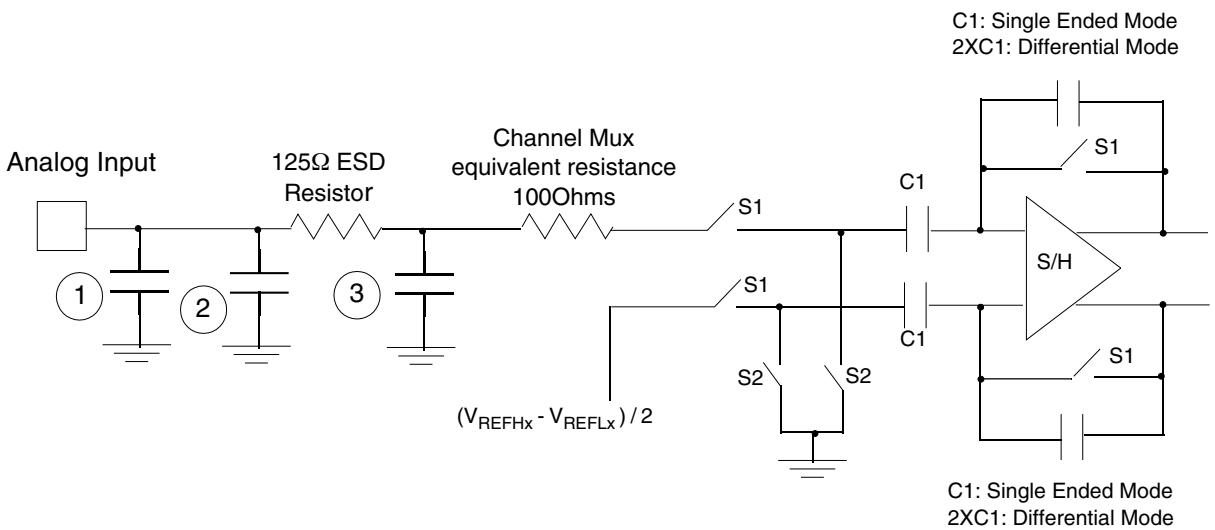
| Board type | Symbol | Description | 48 LQFP | 64 LQFP | Unit | Notes |
|---|---|---|---|---|---|---|
| Single-layer (1s) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 70 | 64 | °C/W | 1, 2 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 46 | 46 | °C/W | 1, 3 |
| Single-layer (1s) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./ min. air speed) | 57 | 52 | °C/W | 1,3 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./ min. air speed) | 39 | 39 | °C/W | 1,3 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 23 | 28 | °C/W | 4 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 17 | 15 | °C/W | 5 |
| — | $\Psi_{JT}$ | Thermal characterization parameter, junction to package top outside center (natural convection) | 3 | 3 | °C/W | 6 |

7. Offset over the conversion range of 0025 to 4080
8. Measured converting a 1 kHz input Full Scale sine wave
9. The current that can be injected into or sourced from an unselected ADC input without affecting the performance of the ADC

### 8.5.1.1 Equivalent Circuit for ADC Inputs

The following figure illustrates the ADC input circuit during sample and hold. S1 and S2 are always opened/closed at non-overlapping phases and operate at the ADC clock frequency. The following equation gives equivalent input impedance when the input is selected.

$$\frac{1}{(\text{ADC ClockRate}) \times 1.4 \times 10^{-12}} + 100ohm + 125ohm$$




1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pF
3. 8 pF noise damping capacitor
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1.4pF for x1 gain; 2.8pf for x2 gain, and 5.6pf for x4 gain
5. S1 and S2 switch phases are non-overlapping and operate at the ADC clock frequency

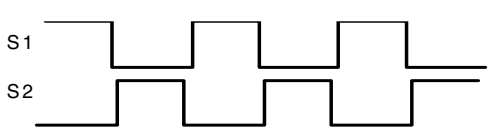



**Figure 9. Equivalent Circuit for A/D Loading**

**Table 28. DAC Parameters (continued)**

| Parameter | Conditions/Comments | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Integral non-linearity[2] | Range of input digital words:<br>410 to 3891 ($19A - $F33)<br>5% to 95% of full range | INL | — | +/- 3 | +/- 4 | LSB[3] |
| Differential non-linearity[2] | Range of input digital words:<br>410 to 3891 ($19A - $F33)<br>5% to 95% of full range | DNL | — | +/- 0.8 | +/- 0.9 | LSB[3] |
| Monotonicity | > 6 sigma monotonicity,<br>< 3.4 ppm non-monotonicity | | guaranteed | | | — |
| Offset error[2] | Range of input digital words:<br>410 to 3891 ($19A - $F33)<br>5% to 95% of full range | $V_{OFFSET}$ | — | + 25 | + 35 | mV |
| Gain error[2] | Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range | $E_{GAIN}$ | — | +/- 0.5 | +/- 1.5 | % |
| **DAC Output** | | | | | | |
| Output voltage range | Within 40 mV of either $V_{SSA}$ or $V_{DDA}$ | $V_{OUT}$ | $V_{SSA}$ + 0.04 V | — | $V_{DDA}$ - 0.04 V | V |
| **AC Specifications** | | | | | | |
| Signal-to-noise ratio | | SNR | — | 85 | — | dB |
| Spurious free dynamic range | | SFDR | — | -72 | — | dB |
| Effective number of bits | | ENOB | — | 11 | — | bits |

1. Settling time is swing range from $V_{SSA}$ to $V_{DDA}$
2. No guaranteed specification within 5% of $V_{DDA}$ or $V_{SSA}$
3. LSB = 0.806mV

## 8.5.4 CMP and 6-bit DAC electrical specifications

**Table 29. Comparator and 6-bit DAC electrical specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 2.7 | — | 3.6 | V |
| $I_{DDHS}$ | Supply current, High-speed mode (EN=1, PMODE=1) | — | — | 200 | µA |
| $I_{DDLS}$ | Supply current, low-speed mode (EN=1, PMODE=0) | — | — | 20 | µA |
| $V_{AIN}$ | Analog input voltage | $V_{SS}$ – 0.3 | — | $V_{DD}$ | V |
| $V_{AIO}$ | Analog input offset voltage | — | — | 20 | mV |

*Table continues on the next page...*

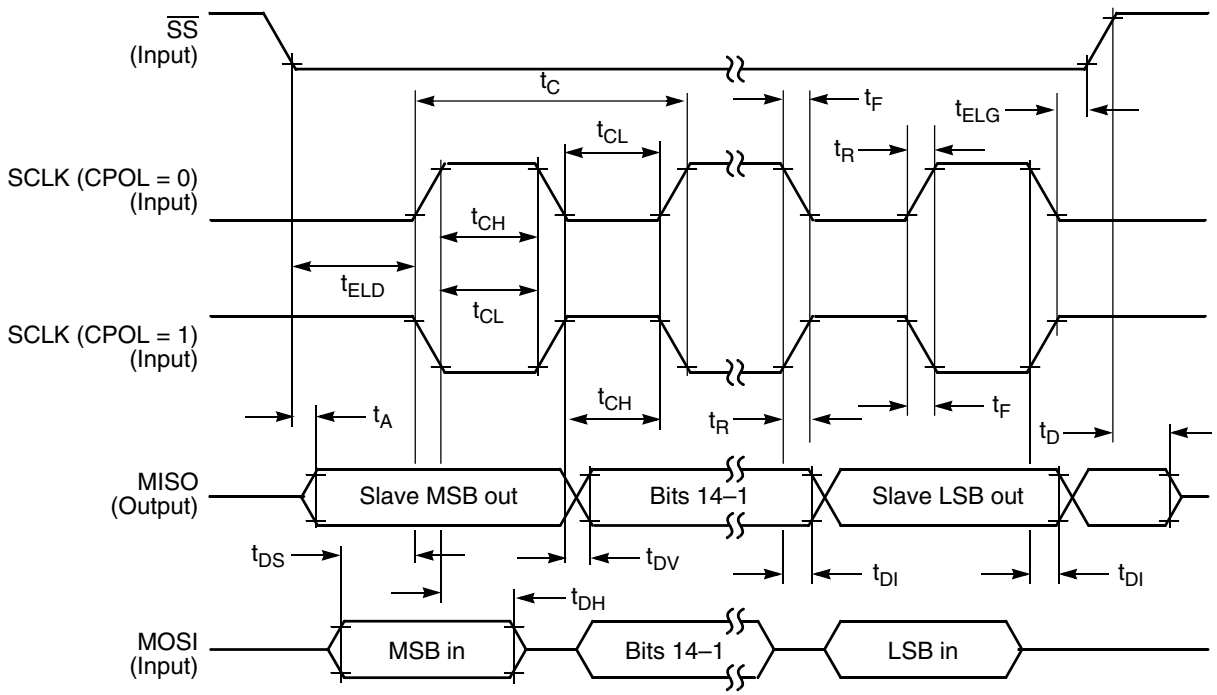



**Figure 17. SPI Slave Timing (CPHA = 0)**

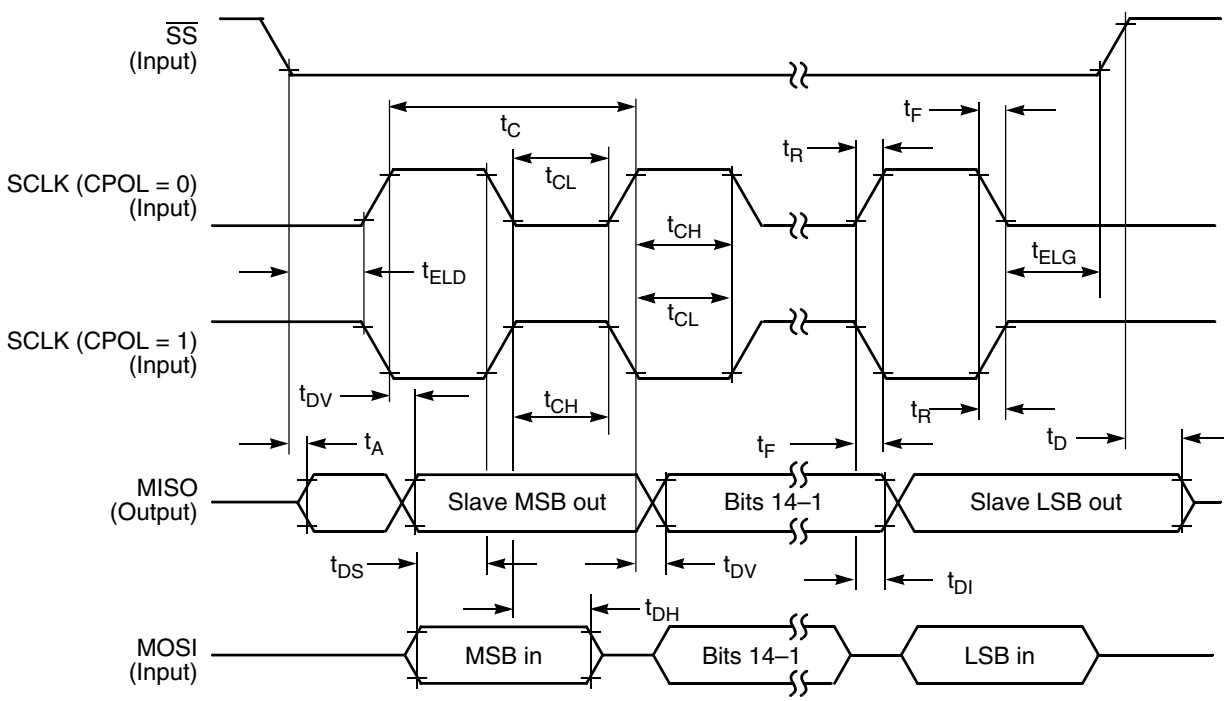



**Figure 18. SPI Slave Timing (CPHA = 1)**

## 8.7.2 Queued Serial Communication Interface (SCI) Timing

Parameters listed are guaranteed by design.

**Table 33. SCI Timing**

| Characteristic | Symbol | Min | Max | Unit | See Figure |
|---|---|---|---|---|---|
| Baud rate[1] | BR | — | ($f_{MAX}$/16) | Mbps | — |
| RXD pulse width | $RXD_{PW}$ | 0.965/BR | 1.04/BR | ns | Figure 19 |
| TXD pulse width | $TXD_{PW}$ | 0.965/BR | 1.04/BR | ns | Figure 20 |
| LIN Slave Mode | | | | | |
| Deviation of slave node clock from nominal clock rate before synchronization | $F_{TOL\_UNSYNCH}$ | -14 | 14 | % | — |
| Deviation of slave node clock relative to the master node clock after synchronization | $F_{TOL\_SYNCH}$ | -2 | 2 | % | — |
| Minimum break character length | $T_{BREAK}$ | 13 | — | Master node bit periods | — |
| | | 11 | — | Slave node bit periods | — |

1. $f_{MAX}$ is the frequency of operation of the SCI clock in MHz, which can be selected system clock (max. 120 MHz depending on part number) or 2x system clock (max. 200 MHz) for the devices.

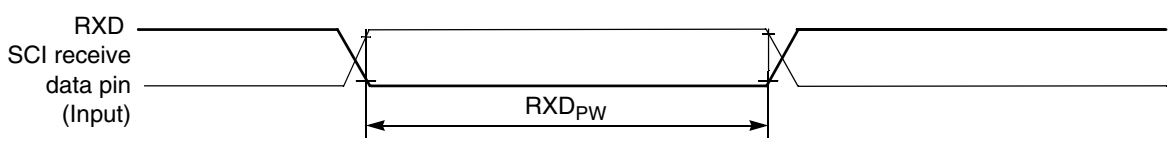



**Figure 19. RXD Pulse Width**

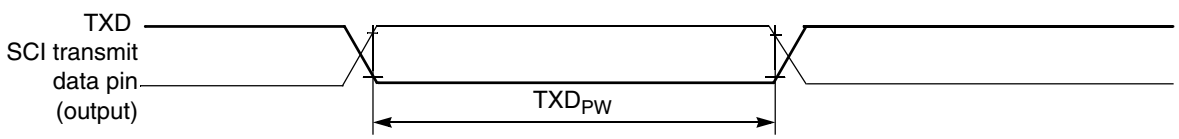



**Figure 20. TXD Pulse Width**

## 8.7.3 Freescale's Scalable Controller Area Network (FlexCAN)

**Table 34. FlexCAN Timing Parameters**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Baud Rate | $BR_{CAN}$ | — | 1 | Mbps |
| CAN Wakeup dominant pulse filtered | $T_{WAKEUP}$ | — | 2 | µs |
| CAN Wakeup dominant pulse pass | $T_{WAKEUP}$ | 5 | — | µs |

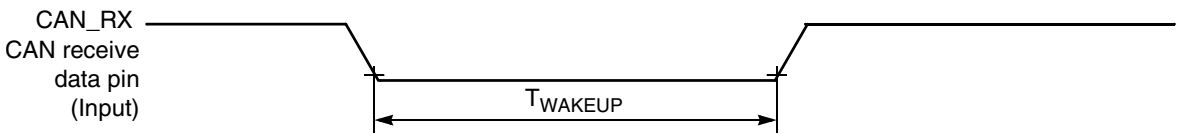



**Figure 21. Bus Wake-up Detection**

## 8.7.4 Inter-Integrated Circuit Interface ($I^2C$) Timing

**Table 35. $I^2C$ Timing**

| Characteristic | Symbol | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| SCL Clock Frequency | $f_{SCL}$ | 0 | 100 | 0 | 400 | kHz |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | $t_{HD}$; STA | 4 | — | 0.6 | — | µs |
| LOW period of the SCL clock | $t_{LOW}$ | 4.7 | — | 1.3 | — | µs |
| HIGH period of the SCL clock | $t_{HIGH}$ | 4 | — | 0.6 | — | µs |
| Set-up time for a repeated START condition | $t_{SU}$; STA | 4.7 | — | 0.6 | — | µs |
| Data hold time for $I_2C$ bus devices | $t_{HD}$; DAT | 0[1] | 3.45[2] | 0[3] | 0.9[1] | µs |
| Data set-up time | $t_{SU}$; DAT | 250[4] | — | 100[2, 5] | — | ns |
| Rise time of SDA and SCL signals | $t_r$ | — | 1000 | 20 +0.1$C_b$[6] | 300 | ns |
| Fall time of SDA and SCL signals | $t_f$ | — | 300 | 20 +0.1$C_b$[5] | 300 | ns |
| Set-up time for STOP condition | $t_{SU}$; STO | 4 | — | 0.6 | — | µs |
| Bus free time between STOP and START condition | $t_{BUF}$ | 4.7 | — | 1.3 | — | µs |
| Pulse width of spikes that must be suppressed by the input filter | $t_{SP}$ | N/A | N/A | 0 | 50 | ns |

1. The master mode $I^2C$ deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
3. Input signal Slew = 10ns and Output Load = 50pf
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode $I^2C$ bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode $I^2C$ bus specification) before the SCL line is released.
6. $C_b$ = total capacitance of the one bus line in pF.

## 9.2 Electrical Design Considerations

**CAUTION**

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the device:

- Provide a low-impedance path from the board power supply to each $V_{DD}$ pin on the device and from the board ground to each $V_{SS}$ (GND) pin.
- The minimum bypass requirement is to place 0.01–0.1µF capacitors positioned as near as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the $V_{DD}/V_{SS}$ pairs, including $V_{DDA}/V_{SSA}$. Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip $V_{DD}$ and $V_{SS}$ (GND) pins are as short as possible.
- Bypass the $V_{DD}$ and $V_{SS}$ with approximately 100 µF, plus the number of 0.1 µF ceramic capacitors.
- PCB trace lengths should be minimal for high-frequency signals.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the $V_{DD}$ and $V_{SS}$ circuits.
- Take special care to minimize noise levels on the $V_{REF}$, $V_{DDA}$, and $V_{SSA}$ pins.
- Using separate power planes for $V_{DD}$ and $V_{DDA}$ and separate ground planes for $V_{SS}$ and VSSA are recommended. Connect the separate analog and digital power and ground planes as near as possible to power supply outputs. If an analog circuit and digital circuit are powered by the same power supply, you should connect a small inductor or ferrite bead in serial with $V_{DDA}$ and $V_{SSA}$ traces.
- Physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. Place an analog ground trace around an analog signal trace to isolate it from digital traces.
- Because the flash memory is programmed through the JTAG/EOnCE port, SPI, SCI, or $I^2C$, the designer should provide an interface to this port if in-circuit flash programming is desired.
- If desired, connect an external RC circuit to the $\overline{\text{RESET}}$ pin. The resistor value should be in the range of 4.7 kΩ–10 kΩ; the capacitor value should be in the range of 0.22 µF–4.7 µF.

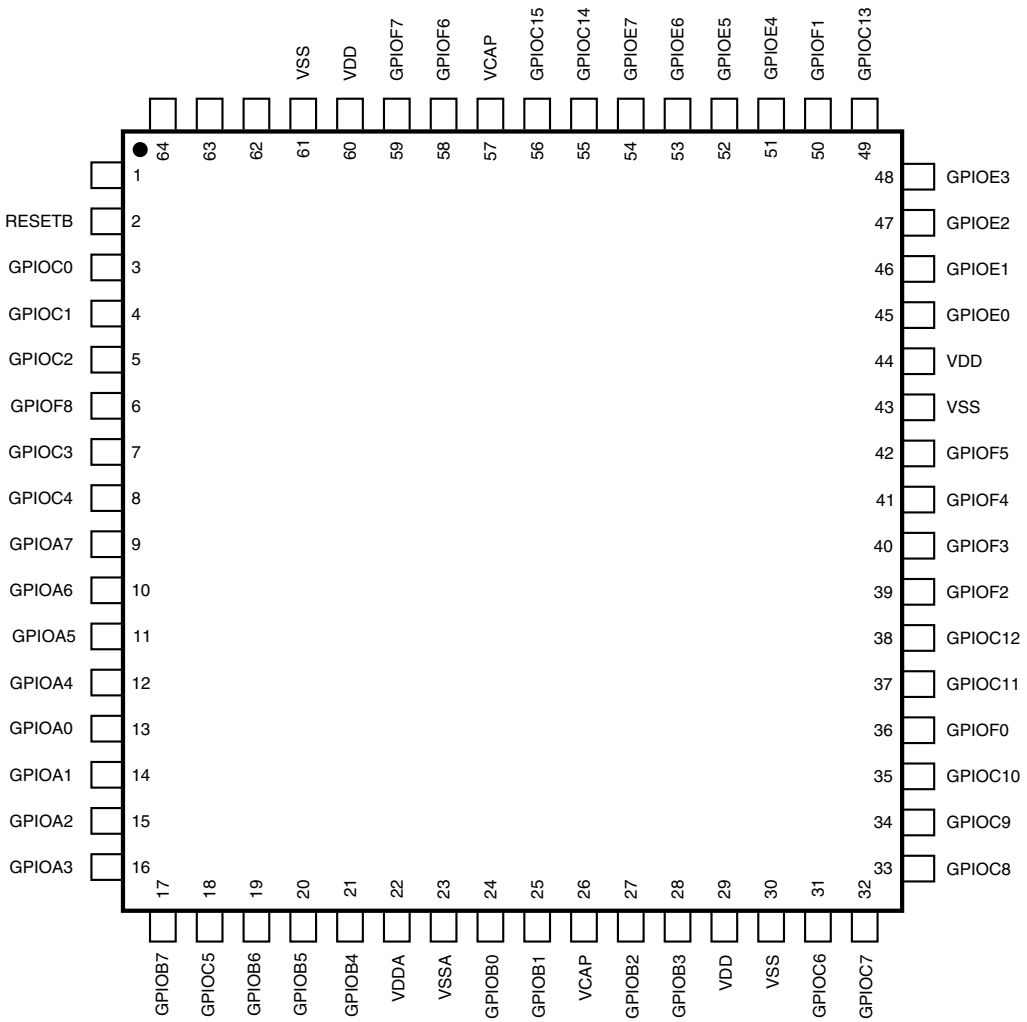



**Figure 23. 64-pin LQFP**

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