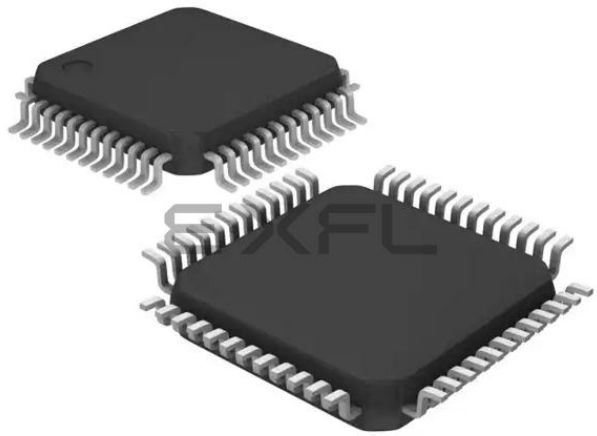


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800EX
Core Size	32-Bit Single-Core
Speed	60MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	39
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f84451vlf

1 Overview

1.1 MC56F844x/5x/7x Product Family

The following table highlights major features, including features that differ among members of the family. Features not listed are shared by all members of the family.

Table 1. 56F844x/5x/7x Family

Part Number	MC56F84																	
	789	**786**	**769**	**766**	**763**	**553**	**550**	**543**	**540**	**587**	**585**	**567**	**565**	**462**	**452**	**451**	**442**	**441**
Core frequency (MHz)	100	100	100	100	100	80	80	80	80	80	80	80	80	60	60	60	60	60
Flash memory (KB)	256	256	128	128	128	96	96	64	64	256	256	128	128	128	96	96	64	64
FlevNVM/ FlexRAM (KB)	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2
Total flash memory, including FlexNVM (KB)[1]	288	288	160	160	160	128	128	96	96	288	288	160	160	160	128	128	96	96
RAM (KB)	32	32	24	24	24	16	16	8	8	32	32	24	24	24	16	16	8	8
Memory resource protection	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
External Watchdog	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
12-bit Cyclic ADC channels	2x8 (300 ns)	2x8 (300 ns)	2x8 (300 ns)	2x8 (300 ns)	2x8 (300 ns)	2x8 (300 ns)	2x5 (300 ns)	2x8 (300 ns)	2x5 (300 ns)	2x8 (600 ns)	2x8 (600 ns)	2x8 (600 ns)	2x8 (600 ns)	2x8 (600 ns)	2x8 (600 ns)	2x5 (600 ns)	2x8 (600 ns)	2x5 (600 ns)
16-bit SAR ADC (with Temp Sensor) channels	1x 16	1x 10	1x 16	1x 10	1x8	1x8	0	1x8	0	1x 16	1x 10	1x 16	1x 10	0	1x8	0	1x8	0
PWMA with input capture:																		
High-resolution channels	1x8	1x8	1x8	1x8	1x8	1x8	1x6	1x8	1x6	0	0	0	0	0	0	0	0	0

Table continues on the next page...

- 32-bit arithmetic and logic multi-bit shifter
- Four 36-bit accumulators, including extension bits
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Bit reverse address mode, effectively supporting DSP and Fast Fourier Transform algorithms
- Full shadowing of the register stack for zero-overhead context saves and restores: nine shadow registers corresponding to the R0, R1, R2, R3, R4, R5, N, N3, and M01 address registers
- Instruction set supporting both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Enhanced bit manipulation instruction set
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- Priority level setting for interrupt levels
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging that is independent of processor speed

1.3 Operation Parameters

- Up to 60 MHz operation at -40 °C to 105 °C ambient temperature
- Single 3.3 V power supply
- Supply range: V_{DD} - V_{SS} = 2.7 V to 3.6 V, V_{DDA} - V_{SSA} = 2.7 V to 3.6 V

1.4 On-Chip Memory and Memory Protection

- Modified dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Internal flash memory with security and protection to prevent unauthorized access
- Memory resource protection (MRP) unit to protect supervisor programs and resources from user programs
- Programming code can reside in flash memory during flash programming
- The dual-ported RAM controller supports concurrent instruction fetches and data accesses, or dual data accesses, by the DSC core.
  - Concurrent accesses provide increased performance.
  - The data and instruction arrive at the core in the same cycle, reducing latency.
- On-chip memory
  - Up to 128 KW program/data flash memory
  - Up to 16 KW dual port data/program RAM

- Up to 16 KW FlexNVM, which can be used as additional program or data flash memory
- Up to 1 KW FlexRAM, which can be configured as enhanced EEPROM (used in conjunction with FlexNVM) or used as additional RAM

1.5 Interrupt Controller

- Five interrupt priority levels
  - Three user programmable priority levels for each interrupt source: level 0, 1, 2
  - Unmaskable level 3 interrupts include: illegal instruction, hardware stack overflow, misaligned data access, SWI3 instruction
  - Maskable level 3 interrupts include: EOnCE step counter, EOnCE breakpoint unit, EOnCE trace buffer
  - Lowest-priority software interrupt: level LP
- Support for nested interrupt: higher priority level interrupt request can interrupt lower priority interrupt subroutine
- Masking of interrupt priority level managed by the 56800EX core
- Two programmable fast interrupts that can be assigned to any interrupt source
- Notification to System Integration Module (SIM) to restart clock when in wait and stop states
- Ability to relocate interrupt vector table

1.6 Peripheral highlights

1.6.1 Enhanced Flex Pulse Width Modulator (eFlexPWM)

- Up to 12 output channels in each module
- 16 bits of resolution for center, edge aligned, and asymmetrical PWMs
- PWMA with accumulative fractional clock calculation
  - Accumulative fractional clock calculation improves the resolution of the PWM period and edge placement
  - Arbitrary PWM edge placement
  - Equivalent to 312 ps PWM frequency and duty-cycle resolution on average
- Each complementary pair can operate with its own PWM frequency base and deadtime values
  - 4 time base in each PWM module
  - Independent top and bottom deadtime insertion for each complementary pair
- PWM outputs can operate as complementary pairs or independent channels
- Independent control of both edges of each PWM output

1.6.7 Queued Serial Communications Interface (QSCI) Modules

- Operating clock up to two times CPU operating frequency
- Four-word-deep FIFOs available on both transmit and receive buffers
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit integer and 3-bit fractional baud rate selection
- Full-duplex or single-wire operation
- Programmable 8-bit or 9-bit data format
- Error detection capability
- Two receiver wakeup methods:
  - Idle line
  - Address mark
- 1/16 bit-time noise detection

1.6.8 Queued Serial Peripheral Interface (QSPI) Modules

- Maximum 25 Mbps baud rate
- Selectable baud rate clock sources for low baud rate communication
- Baud rate as low as Baudrate_Freq_in / 8192
- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Four-word-deep FIFOs available on transmit and receive buffers
- Programmable length transmissions (2 bits to 16 bits)
- Programmable transmit and receive shift order (MSB as first bit transmitted)

1.6.9 Inter-Integrated Circuit (I2C)/System Management Bus (SMBus) Modules

- Compatible with I2C bus standard
- Support for System Management Bus (SMBus) specification, version2
- Multi-master operation
- General call recognition
- 10-bit address extension
- Dual slave addresses
- Programmable glitch input filter

1.6.10 Flex Controller Area Network (FlexCAN) Module

- Clock source from PLL or XOSC/CLKIN

- All pins except JTAG and RESETB pins default to be GPIO inputs
- 2 mA / 9 mA source/sink capability
- Controllable output slew rate

1.7 Block Diagrams

The 56800EX core is based on a modified dual Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

The device's basic architecture appears in Figure 1 and Figure 2. Figure 1 illustrates how the 56800EX system buses communicate with internal memories and the IPBus interface and the internal connections among each unit of the 56800EX core. Figure 2 shows the peripherals and control blocks connected to the IPBus bridge. See the specific device's Reference Manual for details.

2 Signal groups

The input and output signals of the MC56F84xxx are organized into functional groups, as detailed in Table 2.

Table 2. Functional Group Pin Allocations

Functional Group	Number of Pins in 48LQFP	Number of Pins in 64LQFP	Number of Pins in 80LQFP	Number of Pins in 100LQFP
Power Inputs (V_{DD}, V_{DDA}, V_{CAP})	5	6	6	6
Ground (V_{SS}, V_{SSA})	4	4	4	4
Reset	1	1	1	1
eFlexPWM ports, not including fault pins	6	9	N/A	N/A
Queued Serial Peripheral Interface (QSPI) ports	5	6	8	15
Queued Serial Communications Interface (QSCI) ports	6	9	13	15
Inter-Integrated Circuit (I^2C) interface ports	4	6	6	6
12-bit Analog-to-Digital Converter (Cyclic ADC) inputs	10	16	16	16
16-bit Analog-to-Digital Converter (SAR ADC) inputs	2	8	10	16
Analog Comparator inputs/outputs	10/4	13/6	13/6	16/6
12-bit Digital-to-Analog output	1	1	1	1
Quad Timer Module (TMR) ports	6	9	11	13
Controller Area Network (FlexCAN)	2	2	2	2
Inter-Module Crossbar inputs/outputs	12/2	16/6	19/17	25/19
Clock inputs/outputs	2/2	2/2	2/3	2/3
JTAG / Enhanced On-Chip Emulation (EOnCE)	4	4	4	4

3 Ordering parts

3.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the following device numbers: MC56F84

4 Part identification

4.4 Example

This is an example part number: MC56F84789VLL

5 Terminology and guidelines

5.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

5.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

5.2 Definition: Operating behavior

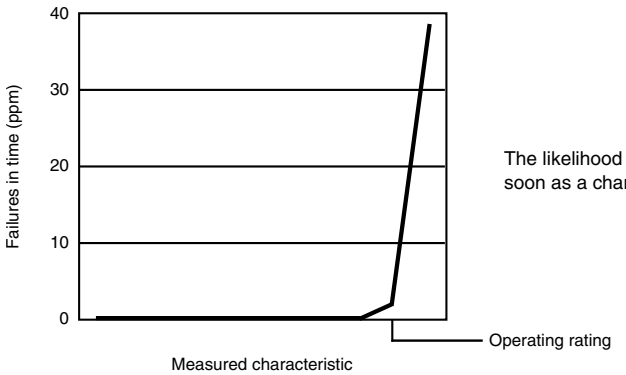
An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

5.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

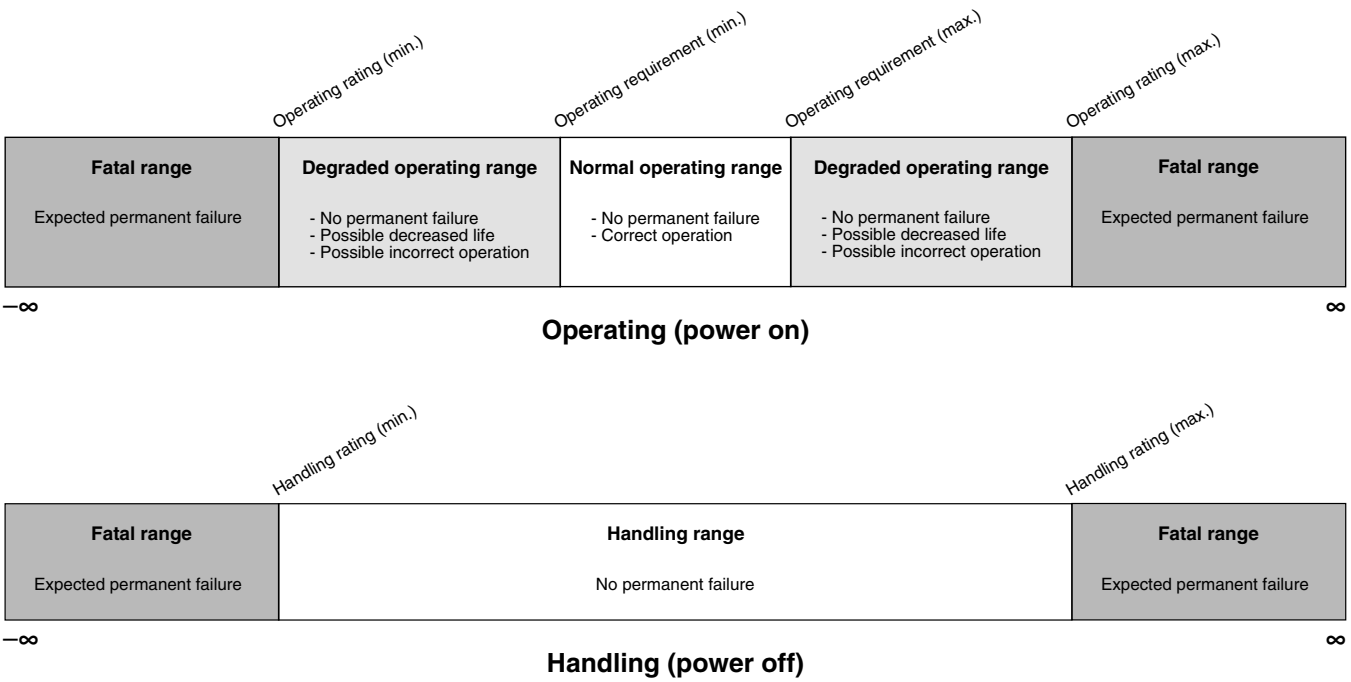
Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

5.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

5.6 Relationship between ratings and operating requirements



5.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

Absolute maximum ratings in Table 4 are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this chapter apply over the temperature range of -40°C to 105°C ambient temperature over the following supply ranges: VSS = VSSA = 0 V, VDD = VDDA = 3.0 V to 3.6 V, CL ≤ 50 pF, f_{OP} = 60 MHz.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

7.2 AC Electrical Characteristics

Tests are conducted using the input levels specified in Table 7. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in Figure 3.

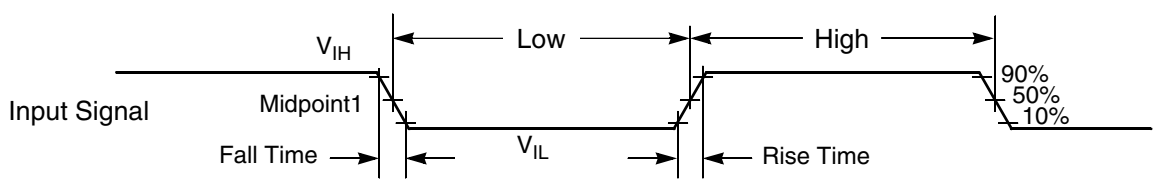


Figure 3. Input Signal Measurement References

Figure 4 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

7.5.2 Thermal attributes

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To account for $P_{I/O}$ in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is very small.

See Thermal Design Considerations for more detail on thermal design considerations.

Board type	Symbol	Description	48 LQFP	64 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	70	64	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	46	46	°C/W	1, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	57	52	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	39	39	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	23	28	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	17	15	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	3	°C/W	6

8.3.3 External Crystal or Resonator Requirement

Table 20. Crystal or Resonator Requirement

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation	f_{XOSC}	4	8	16	MHz

8.3.4 Relaxation Oscillator Timing

Table 21. Relaxation Oscillator Electrical Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
8 MHz Output Frequency[1] RUN Mode • 0°C to 105°C • -40°C to 105°C Standby Mode (IRC trimmed @ 8 MHz) • -40°C to 105°C		 7.84 7.76 TBD	 8 8 TBD	 8.16 8.24 TBD	 MHz kHz
8 MHz Frequency Variation RUN Mode Due to temperature • 0°C to 105°C • -40°C to 105°C Standby Mode			 +/-1.5 +/- 1.5 Unspecified	 +/-2 +/-3	 %
32 kHz Output Frequency[2] RUN Mode • -40°C to 105°C		 TBD	 32	 TBD	 kHz
32 kHz Output Frequency Variation RUN Mode Due to temperature • -40°C to 105°C			 +/-2.5	 +/-4	 %
Stabilization Time • 8 MHz output[3] • 32 kHz output[4]	tstab		 0.12 14.4	 0.4 16.2	 µs
Output Duty Cycle		48	50	52	%

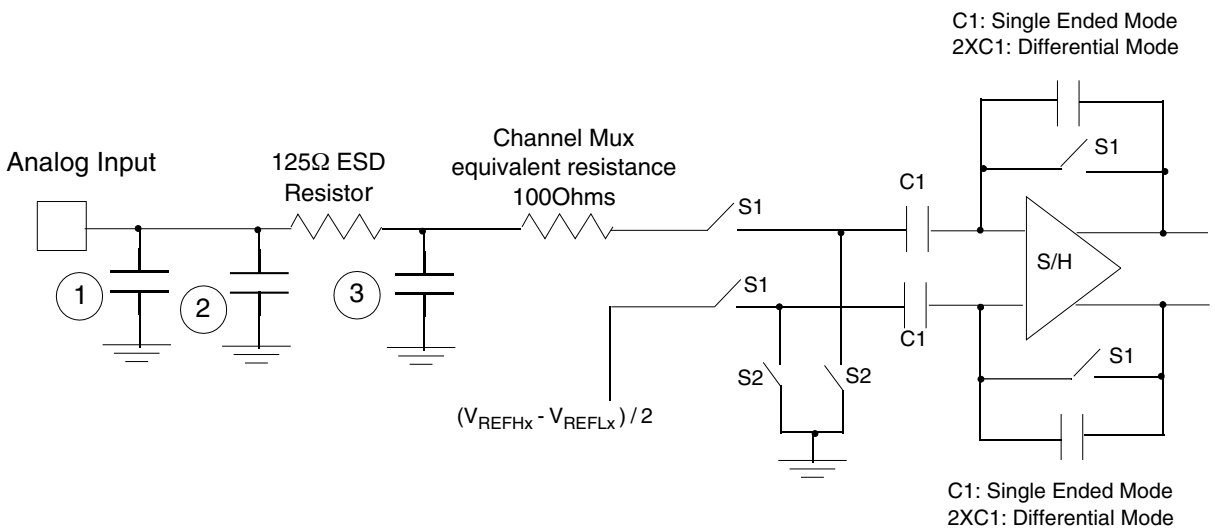
1. Frequency after application of 8 MHz trim
2. Frequency after application of 32 kHz trim
3. Standby to run mode transition
4. Power down to run mode transition

7. Offset over the conversion range of 0025 to 4080
8. Measured converting a 1 kHz input Full Scale sine wave
9. The current that can be injected into or sourced from an unselected ADC input without affecting the performance of the ADC

8.5.1.1 Equivalent Circuit for ADC Inputs

The following figure illustrates the ADC input circuit during sample and hold. S1 and S2 are always opened/closed at non-overlapping phases and operate at the ADC clock frequency. The following equation gives equivalent input impedance when the input is selected.

$$\frac{1}{(\text{ADC ClockRate}) \times 1.4 \times 10^{-12}} + 100ohm + 125ohm$$



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pF
3. 8 pF noise damping capacitor
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1.4pF for x1 gain; 2.8pf for x2 gain, and 5.6pf for x4 gain
5. S1 and S2 switch phases are non-overlapping and operate at the ADC clock frequency

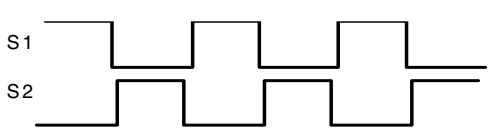


Figure 9. Equivalent Circuit for A/D Loading

8.5.2 16-bit SAR ADC electrical specifications

8.5.2.1 16-bit ADC operating conditions

Table 26. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	2.7	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD}-V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSA})	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high	Absolute	V_{DDA}	V_{DDA}	V_{DDA}	V	3
V_{REFL}	ADC reference voltage low	Absolute	V_{SSA}	V_{SSA}	V_{SSA}	V	4
V_{ADIN}	Input voltage		V_{SSA}	—	V_{DDA}	V	
C_{ADIN}	Input capacitance	• 16 bit modes • 8/10/12 bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance	12 bit modes f_{ADCK} < 4MHz	—	—	5	kΩ	5
f_{ADCK}	ADC conversion clock frequency	≤ 12 bit modes	1.0	—	18.0	MHz	6
f_{ADCK}	ADC conversion clock frequency	16 bit modes	2.0	—	12.0	MHz	6
C_{rate}	ADC conversion rate	≤ 12 bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	7
C_{rate}	ADC conversion rate	16 bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	7

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.
3. V_{REFH} is internally tied to V_{DDA}.
4. V_{REFL} is internally tied to V_{SSA}.
5. This resistance is external to MCU. The analog source resistance should be kept as low as possible in order to achieve the best results. The results in this datasheet were derived from a system which has <8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to <1ns.
6. To use the maximum ADC conversion clock frequency, the ADHSC bit should be set and the ADLPC bit should be clear.

Table 27. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
E_{FS}	Full-scale error	• 12 bit modes • <12 bit modes	— —	-4 -1.4	-5.4 -1.8	LSB[4]	$V_{ADIN} = V_{DDA}$ 5
E_Q	Quantization error	• 16 bit modes • 12 bit modes	— —	-1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16 bit single-ended mode • Avg=32 • Avg=4 12 bit single-ended mode • Avg=32 • Avg=1	 12.2 11.4 	 13.9 13.1 10.8 10.2	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16 bit single-ended mode • Avg=32 12 bit single-ended mode • Avg=32	 — —	 -85 -74	 — —	 dB dB	7
SFDR	Spurious free dynamic range	16 bit single-ended mode • Avg=32 12 bit single-ended mode • Avg=32	 78 	 90 78	 — —	 dB dB	7
E_{IL}	Input leakage error		$I_{In} \times R_{AS}$			mV	I_{In} = leakage current (refer to the device's voltage and current operating ratings)
	Temp sensor slope	–40°C to 105°C	—	1.715	—	mV/°C	
V_{TEMP25}	Temp sensor voltage	25°C	—	722	—	mV	8

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

Table 31. Timer Timing

Characteristic	Symbol	Min[1]	Max	Unit	See Figure
Timer input period	P_{IN}	2T + 6	—	ns	Figure 14
Timer input high/low period	P_{INHL}	1T + 3	—	ns	Figure 14
Timer output period	P_{OUT}	33	—	ns	Figure 14
Timer output high/low period	P_{OUTHL}	16.7	—	ns	Figure 14

1. T = clock cycle. For 60 MHz operation, T = 16.7 ns.

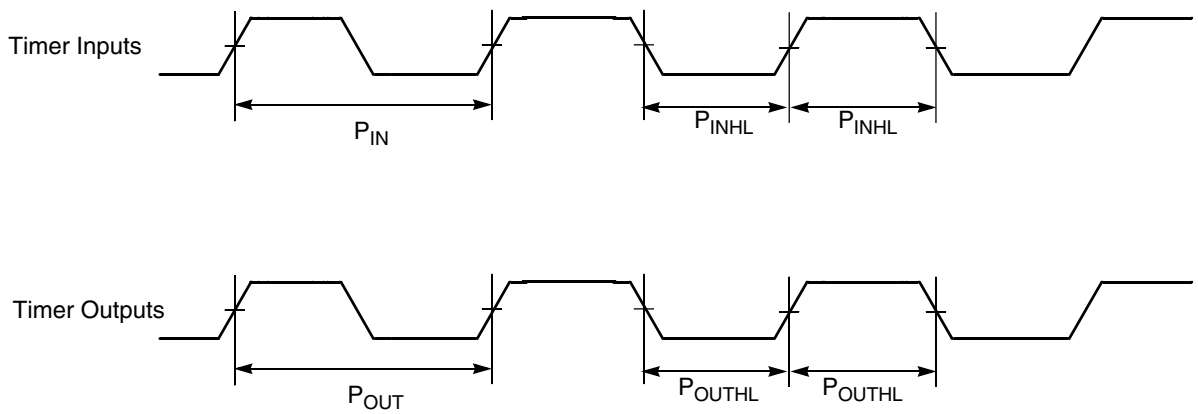


Figure 14. Timer Timing

8.7 Communication interfaces

8.7.1 Queued Serial Peripheral Interface (SPI) Timing

Parameters listed are guaranteed by design.

Table 32. SPI Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time	t_C				Figure 15
Master		55	—	ns	Figure 16
Slave		55	—	ns	Figure 17
					Figure 18
Enable lead time	t_{ELD}				Figure 18
Master		—	—	ns	
Slave		17.5	—	ns	
Enable lag time	t_{ELG}				Figure 18
Master		—	—	ns	
Slave		17.5	—	ns	

Table continues on the next page...

Table 32. SPI Timing (continued)

Characteristic	Symbol	Min	Max	Unit	See Figure
Clock (SCK) high time	t_{CH}				Figure 15
Master		27.6	—	ns	Figure 16
Slave		27.6	—	ns	Figure 17
					Figure 18
Clock (SCK) low time	t_{CL}				Figure 18
Master		27.6	—	ns	
Slave		27.6	—	ns	
Data set-up time required for inputs	t_{DS}				Figure 15
Master		27.6	—	ns	Figure 16
Slave		1	—	ns	Figure 17
					Figure 18
Data hold time required for inputs	t_{DH}				Figure 15
Master		1	—	ns	Figure 16
Slave		3	—	ns	Figure 17
					Figure 18
Access time (time to data active from high-impedance state)	t_A				Figure 18
Slave		5	—	ns	
Disable time (hold time to high-impedance state)	t_D				Figure 18
Slave		5	—	ns	
Data valid for outputs	t_{DV}				Figure 15
Master		—	8.3	ns	Figure 16
Slave (after enable edge)		—	25	ns	Figure 17
					Figure 18
Data invalid	t_{DI}				Figure 15
Master		0	—	ns	Figure 16
Slave		0	—	ns	Figure 17
					Figure 18
Rise time	t_R				Figure 15
Master		—	1	ns	Figure 16
Slave		—	1	ns	Figure 17
					Figure 18
Fall time	t_F				Figure 15
Master		—	1	ns	Figure 16
Slave		—	1	ns	Figure 17
					Figure 18

9.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the device:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the device and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place 0.01–0.1µF capacitors positioned as near as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are as short as possible.
- Bypass the V_{DD} and V_{SS} with approximately 100 µF, plus the number of 0.1 µF ceramic capacitors.
- PCB trace lengths should be minimal for high-frequency signals.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF}, V_{DDA}, and V_{SSA} pins.
- Using separate power planes for V_{DD} and V_{DDA} and separate ground planes for V_{SS} and VSSA are recommended. Connect the separate analog and digital power and ground planes as near as possible to power supply outputs. If an analog circuit and digital circuit are powered by the same power supply, you should connect a small inductor or ferrite bead in serial with V_{DDA} and V_{SSA} traces.
- Physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. Place an analog ground trace around an analog signal trace to isolate it from digital traces.
- Because the flash memory is programmed through the JTAG/EOnCE port, SPI, SCI, or I^2C, the designer should provide an interface to this port if in-circuit flash programming is desired.
- If desired, connect an external RC circuit to the $\overline{\text{RESET}}$ pin. The resistor value should be in the range of 4.7 kΩ–10 kΩ; the capacitor value should be in the range of 0.22 µF–4.7 µF.

64 LQFP	48 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
11	—	GPIOA5	GPIOA5	ANA5&ANC9			
12	8	GPIOA4	GPIOA4	ANA4&ANC8&CMPD_IN0			
13	9	GPIOA0	GPIOA0	ANA0&CMPA_IN3	CMPC_O		
14	10	GPIOA1	GPIOA1	ANA1&CMPA_IN0			
15	11	GPIOA2	GPIOA2	ANA2&VREFHA&CMPA_IN1			
16	12	GPIOA3	GPIOA3	ANA3&VREFLA&CMPA_IN2			
17	—	GPIOB7	GPIOB7	ANB7&ANC15&CMPB_IN2			
18	13	GPIOC5	GPIOC5	DACO	XB_IN7		
19	—	GPIOB6	GPIOB6	ANB6&ANC14&CMPB_IN1			
20	—	GPIOB5	GPIOB5	ANB5&ANC13&CMPC_IN2			
21	14	GPIOB4	GPIOB4	ANB4&ANC12&CMPC_IN1			
22	15	VDDA	VDDA				
23	16	VSSA	VSSA				
24	17	GPIOB0	GPIOB0	ANB0&CMPB_IN3			
25	18	GPIOB1	GPIOB1	ANB1&CMPB_IN0			
26	19	VCAP	VCAP				
27	20	GPIOB2	GPIOB2	ANB2&VREFHB&CMPC_IN3			
28	21	GPIOB3	GPIOB3	ANB3&VREFLB&CMPC_IN0			
29	—	VDD	VDD				
30	22	VSS	VSS				
31	23	GPIOC6	GPIOC6	TA2	XB_IN3	CMP_REF	
32	24	GPIOC7	GPIOC7	SS0_B	TXD0		
33	25	GPIOC8	GPIOC8	MISO0	RXD0	XB_IN9	
34	26	GPIOC9	GPIOC9	SCK0	XB_IN4		
35	27	GPIOC10	GPIOC10	MOSI0	XB_IN5	MISO0	
36	28	GPIOF0	GPIOF0	XB_IN6	TB2	SCK1	
37	29	GPIOC11	GPIOC11	CANTX	SCL1	TXD1	
38	30	GPIOC12	GPIOC12	CANRX	SDA1	RXD1	
39	—	GPIOF2	GPIOF2	SCL1	XB_OUT6		
40	—	GPIOF3	GPIOF3	SDA1	XB_OUT7		
41	—	GPIOF4	GPIOF4	TXD1	XB_OUT8		
42	—	GPIOF5	GPIOF5	RXD1	XB_OUT9		
43	31	VSS	VSS				
44	32	VDD	VDD				
45	33	GPIOE0	GPIOE0	PWMA_0B			
46	34	GPIOE1	GPIOE1	PWMA_0A			
47	35	GPIOE2	GPIOE2	PWMA_1B			
48	36	GPIOE3	GPIOE3	PWMA_1A			
49	37	GPIOC13	GPIOC13	TA3	XB_IN6	EWM_OUT_B	
50	38	GPIOF1	GPIOF1	CLKO1	XB_IN7	CMPD_O	
51	39	GPIOE4	GPIOE4	PWMA_2B	XB_IN2		

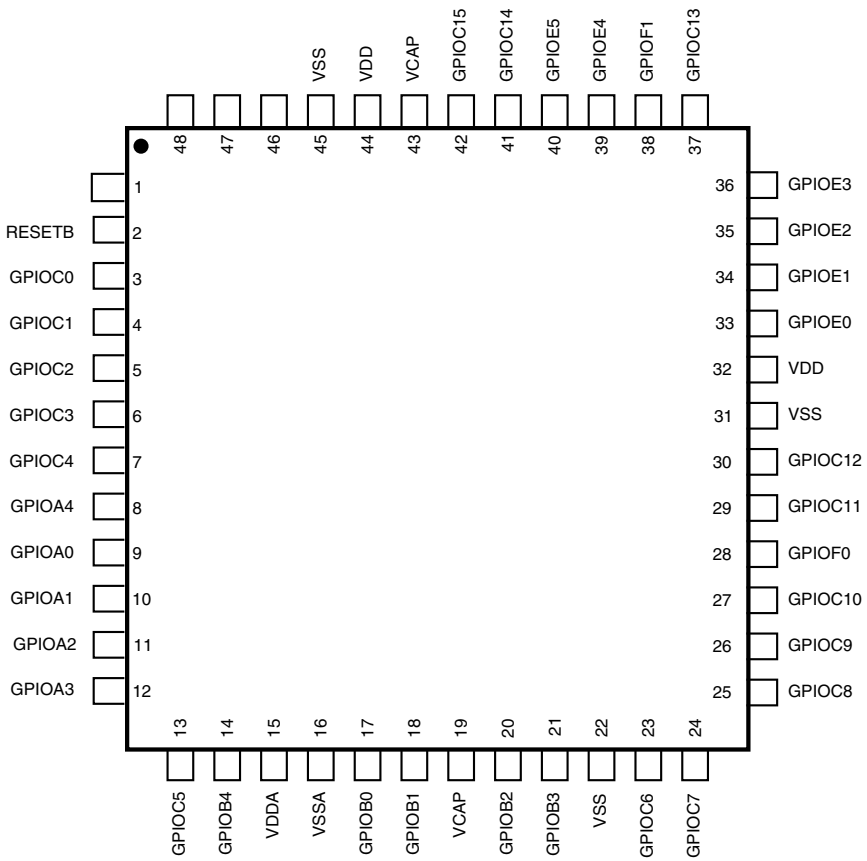


Figure 24. 48-pin LQFP

12 Product Documentation

The documents listed in Table 36 are required for a complete description and proper design with the device. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, or online at http://www.freescale.com.

Table 36. Device Documentation

Topic	Description	Document Number
DSP56800E/DSP56800EX Reference Manual	Detailed description of the 56800EX family architecture, 32-bit digital signal controller core processor, and the instruction set	DSP56800ERM
MC56F844xx Reference Manual	Detailed functional description and programming model	MC56F844XXRM
Serial Bootloader User Guide	Detailed description of the Serial Bootloader in the DSC family of devices	TBD
MC56F844xx Data Sheet	Electrical and timing specifications, pin descriptions, and package information (this document)	MC56F844XX
MC56F84xxx Errata	Details any chip issues that might be present	MC56F84XXX_0N27E

13 Revision History

The following table summarizes changes to this document since the release of the previous version.

Table 37. Revision History

Rev.	Date	Substantial Changes
2	06/2012	This is the first publicly released version of this document.