# Zilog - Z8018110FEC00TR Datasheet

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z80180 |
| Number of Cores/Bus Width | 1 Core, 8-Bit |
| Speed | 10MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 5.0V |
| Operating Temperature | -40°C ~ 100°C (TA) |
| Security Features | - |
| Package / Case | 100-QFP |
| Supplier Device Package | 100-QFP |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8018110fec00tr |

## PIN DESCRIPTION

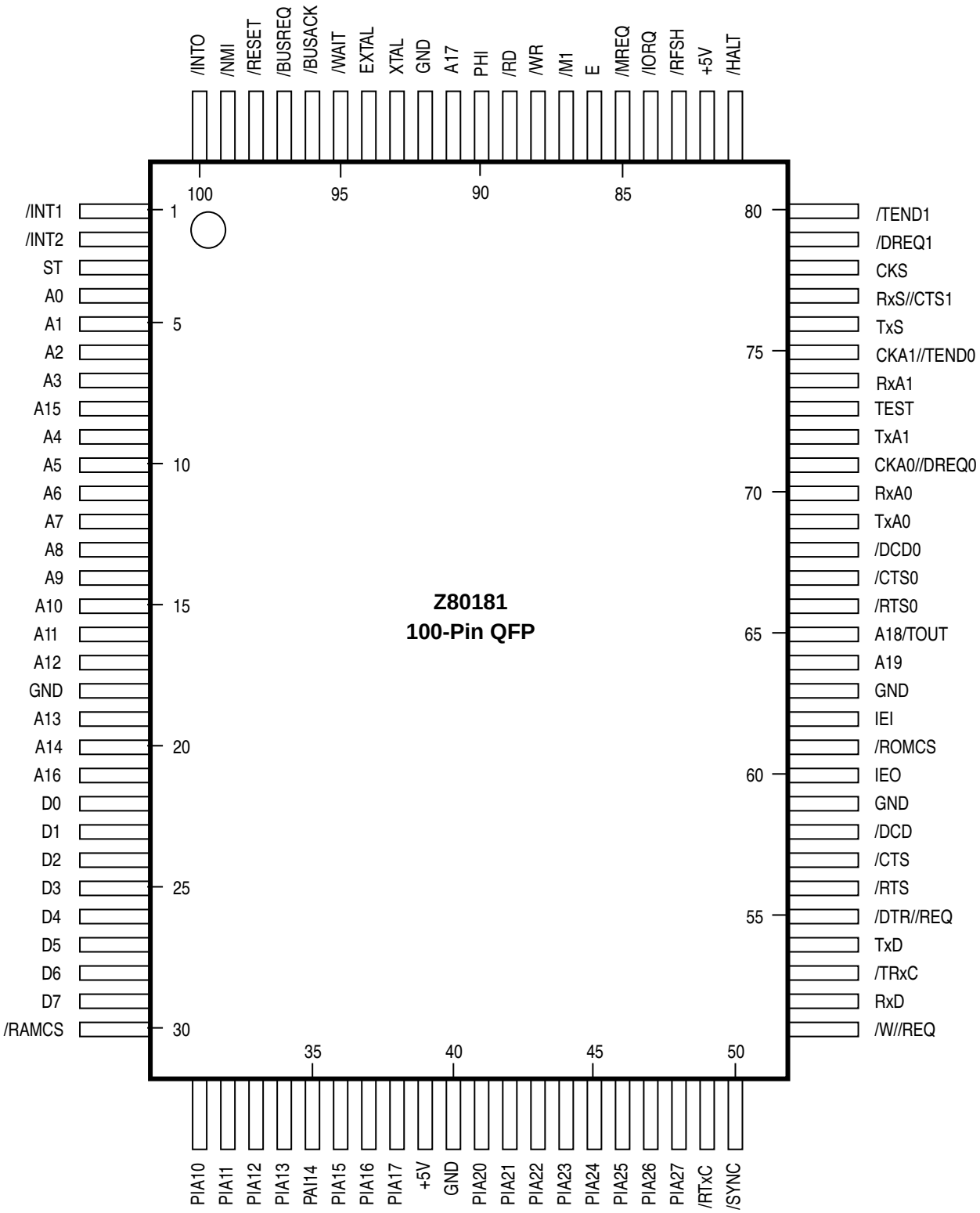



**Figure 2. 100-Pin QFP Pin Configuration**

## PERIPHERAL SIGNALS

| Pin Name | Pin Number | Input/Output, Tri-State | Function |
|---|---|---|---|
| RXA0, RXA1 | 70, 74 | In, Active 1 | **ASCI Receive Data 0 and 1.** These signals are the receive data to the ASCI channels. |
| TXA0, TXA1 | 69, 72 | Out, Active 1 | **ASCI Transmit Data 0 and 1.** These signals are the receive data to the ASCI channels. Transmit data changes are with respect to the falling edge of the transmit clock. |
| /RTS0 | 66 | Out, Active 0 | **Request to Send 0.** This is a programmable modem control signal for ASCI channel 0. |
| /DCD0 | 68 | In, Active 0 | **Data Carrier Detect 0.** This is a programmable modem control signal for ASCI channel 0. |
| /CTS0 | 67 | In, Active 0 | **Clear To Send 0.** This is a programmable modem control signal for ASCI channel 0. |
| /CTS1/RXS | 77 | In, Active 0 | **Clear To Send 0/Clocked Serial Receive Data.** This is a programmable modem control signal for ASCI channel 0. Also, this signal becomes receive data for the CSIO channel under program control. On power-on Reset, this pin is set as RxS. |
| CKA0//DREQ0 | 71 | I/O, Active 1 | **Asynchronous Clock0/DMAC0 Request.** This pin is the transmit and receive clock for the Asynchronous channel 0. Also, under program control, this pin is used to request a DMA transfer from DMA channel 0. DMA0 monitors this input to determine when an external device is ready for a read or write operation. On power-on Reset, this pin is initialized as CKA0. |
| CKA1//TEND0 | 75 | I/O, Active 1 | **Asynchronous Clock1/DMAC0 Transfer End.** This pin is the transmit and receive clock for the Asynchronous channel 1. Also, under program control, this pin becomes /TEND0 and is asserted during the last write cycle of the DMA0 operation and is used to indicate the end of the block transfer. On power-on Reset, this pin initializes as CKA1. |
| /TEND1 | 80 | Out, Active 0 | **DMAC1 Transfer End.** This pin is asserted during the last write cycle of the DMA1 operation and is used to indicate the end of the block transfer. |
| CKS | 78 | I/O, Active 1 | **CSIO Clock.** This line is the clock for the CSIO channel. |
| TXS | 76 | Out, Active 1 | **CSI/O Tx Data.** This line carries the transmit data from the CSIO channel. |
| /DREQ1 | 79 | In, Active 0 | **DMAC1 Request.** This pin is used to request a DMA transfer from DMA channel 1. DMA1 monitors this input to determine when an external device is ready for a read or write operation. |

Each of the Counter/Timer Channels, designated Channels 0-3, have an 8-bit prescaler (when used in timer mode) and its own 8-bit counter to provide a wide range of count resolution. Each of the channels have their own Clock/Trigger input to quantify the counting process and an output to indicate zero crossing/timeout conditions. These signals are multiplexed with the Parallel Interface Adapter 1 (PIA1). With only one interrupt vector programmed into the logic unit, each channel can generate a unique interrupt vector in response to the interrupt acknowledge cycle.

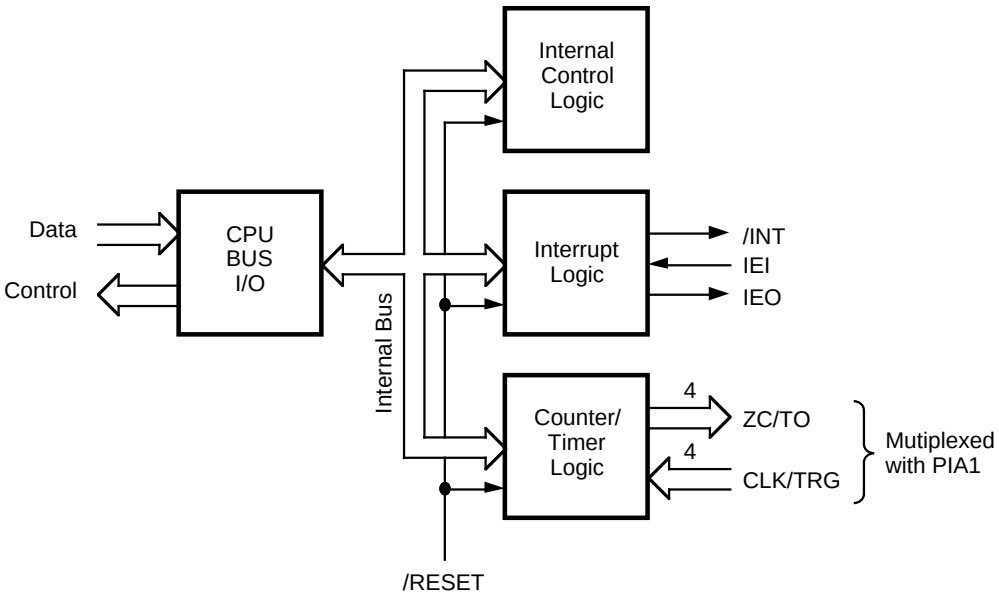



**Figure 5. CTC Block Diagram**

## Parallel Interface Adapter (PIA)

The SAC has two 8-bit Parallel Interface Adapter (PIA) Ports. The ports are referred to as PIA1 and PIA2. Each port has two associated control registers; a Data Register and a register to determine each bit's direction (input or output). PIA1 is multiplexed with the CTC I/O pins. When the CTC I/O feature is selected, the CTC I/O functions override the PIA1 feature. Mode Selection is made through the System Configuration Register (Address: EDh; Bit D0). PIA1 has Schmitt-triggered inputs to have a better noise margin. These ports are inputs after reset.

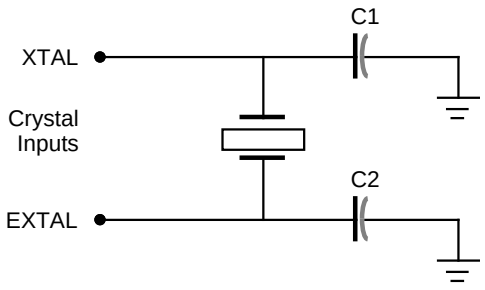
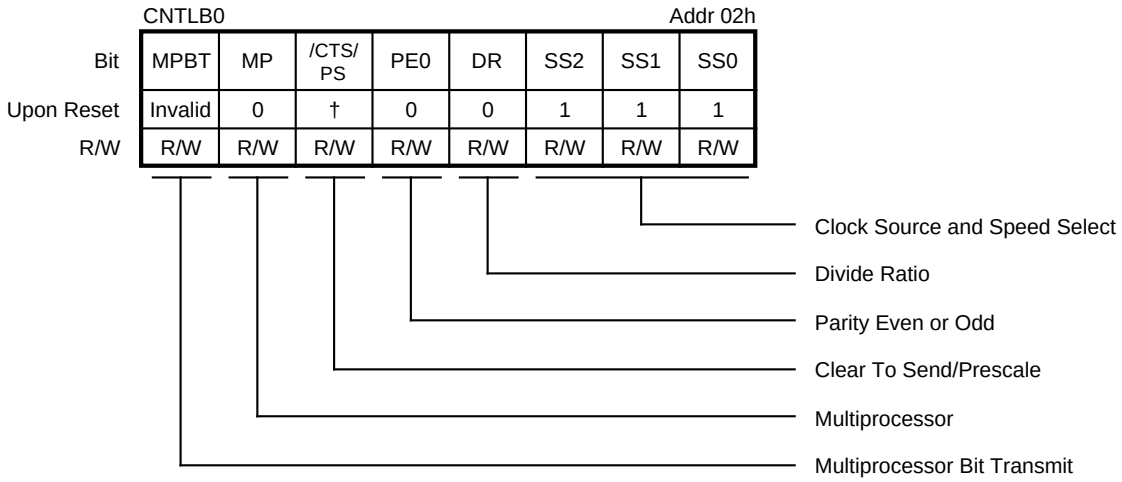



**Figure 6. Circuit Configuration For Crystal**

## Clock Generator

The SAC uses the Z181 MPU's on-chip clock generator to supply system clock. The required clock is easily generated by connecting a crystal to the external terminals (XTAL, EXTAL). The clock output runs at half the crystal frequency. The system clock inputs of the SCC and the CTC are internally connected to the PHI output of the Z181 MPU.

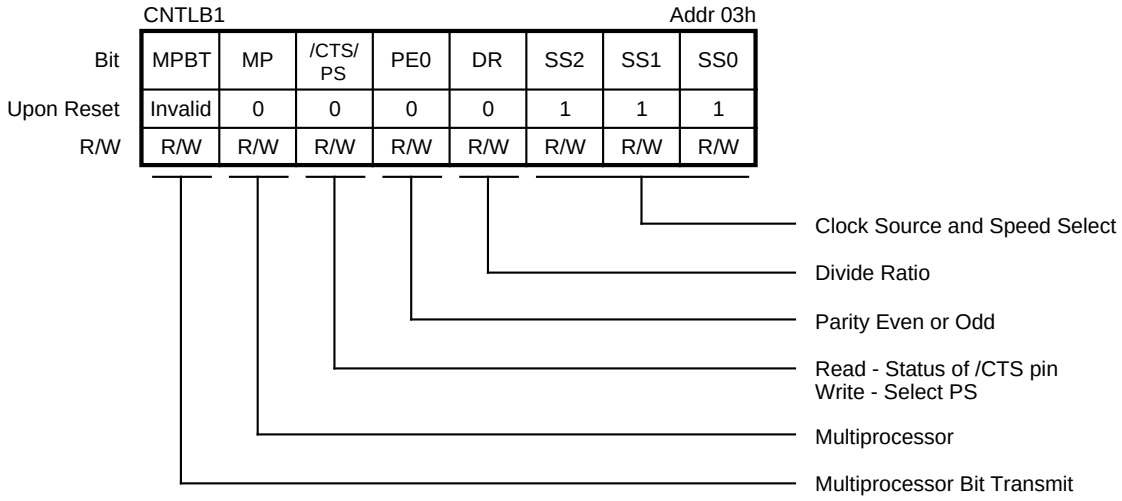



† /CTS - Depending on the condition of /CTS pin.
PS - Cleared to 0.

| General Divide Ratio SS, 2, 1, 0 | PS = 0 (Divide Ratio = 10) DR = 0 (x16) | DR = 1 (x64) | PS = 1 (Divide Ratio = 30) DR = 0 (x16) | DR = 1 (x64) |
|---|---|---|---|---|
| 000 | Ø ÷ 160 | Ø ÷ 640 | Ø ÷ 480 | Ø ÷ 1920 |
| 001 | Ø ÷ 320 | Ø ÷ 1280 | Ø ÷ 960 | Ø ÷ 3840 |
| 010 | Ø ÷ 640 | Ø ÷ 2580 | Ø ÷ 1920 | Ø ÷ 7680 |
| 011 | Ø ÷ 1280 | Ø ÷ 5120 | Ø ÷ 3840 | Ø ÷ 15360 |
| 100 | Ø ÷ 2560 | Ø ÷ 10240 | Ø ÷ 7680 | Ø ÷ 30720 |
| 101 | Ø ÷ 5120 | Ø ÷ 20480 | Ø ÷ 15360 | Ø ÷ 61440 |
| 110 | Ø ÷ 10240 | Ø ÷ 40960 | Ø ÷ 30720 | Ø ÷ 122880 |
| 111 | External Clock (Frequency < Ø ÷ 40) | | | |

**Figure 9. ASCI Control Register B (Ch. 0)**

## ASCI CHANNELS CONTROL REGISTERS (Continued)




| General Divide Ratio SS, 2, 1, 0 | PS = 0 (Divide Ratio = 10) DR = 0 (x16) | DR = 1 (x64) | PS = 1 (Divide Ratio = 30) DR = 0 (x16) | DR = 1 (x64) |
|---|---|---|---|---|
| 000 | Ø ÷ 160 | Ø ÷ 640 | Ø ÷ 480 | Ø ÷ 1920 |
| 001 | Ø ÷ 320 | Ø ÷ 1280 | Ø ÷ 960 | Ø ÷ 3840 |
| 010 | Ø ÷ 640 | Ø ÷ 2580 | Ø ÷ 1920 | Ø ÷ 7680 |
| 011 | Ø ÷ 1280 | Ø ÷ 5120 | Ø ÷ 3840 | Ø ÷ 15360 |
| 100 | Ø ÷ 2560 | Ø ÷ 10240 | Ø ÷ 7680 | Ø ÷ 30720 |
| 101 | Ø ÷ 5120 | Ø ÷ 20480 | Ø ÷ 15360 | Ø ÷ 61440 |
| 110 | Ø ÷ 10240 | Ø ÷ 40960 | Ø ÷ 30720 | Ø ÷ 122880 |
| 111 | External Clock (Frequency < Ø ÷ 40) | | | |

**Figure 10. ASCI Control Register B (Ch. 1)**

## ASCI CHANNELS CONTROL REGISTERS (Continued)

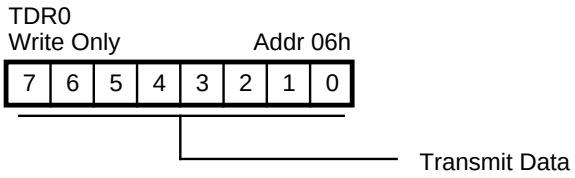



**Figure 13. ASCI Transmit Data Register (Ch. 0)**

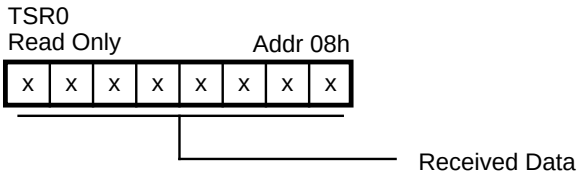



**Figure 15. ASCI Receive Data Register (Ch. 0)**

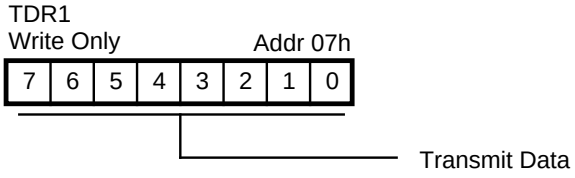



**Figure 14. ASCI Transmit Data Register (Ch. 1)**

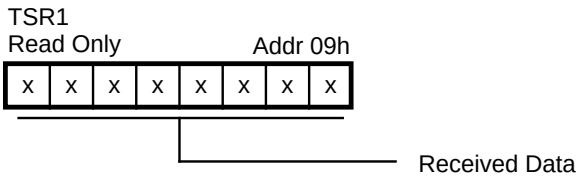
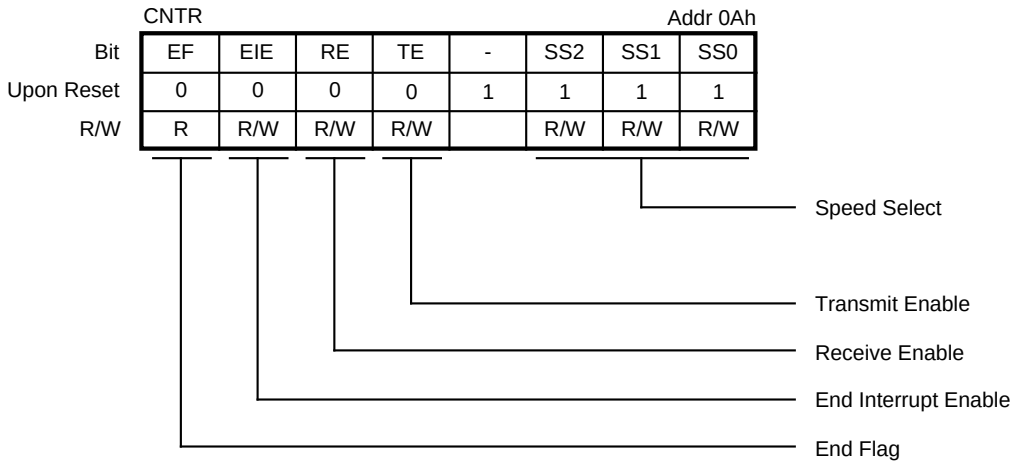



**Figure 16. ASCI Receive Data Register (Ch. 1)**

## CSI/O Registers




| SS2, 1, 0 | Baud Rate |
|---|---|
| 000 | Ø ÷ 20 |
| 001 | Ø ÷ 40 |
| 010 | Ø ÷ 80 |
| 011 | Ø ÷ 100 |

| SS2, 1, 0 | Baud Rate |
|---|---|
| 100 | Ø ÷ 320 |
| 101 | Ø ÷ 640 |
| 110 | Ø ÷ 1280 |
| 111 | External Clock (Frequency < Ø ÷ 20) |

**Figure 17. CSI/O Control Register**

### Time Constant Word

Before a channel can start counting, it must receive a time constant word. The time constant value may be anywhere between 1 and 256, with "0" being accepted as a count of 256 (Figure 47).

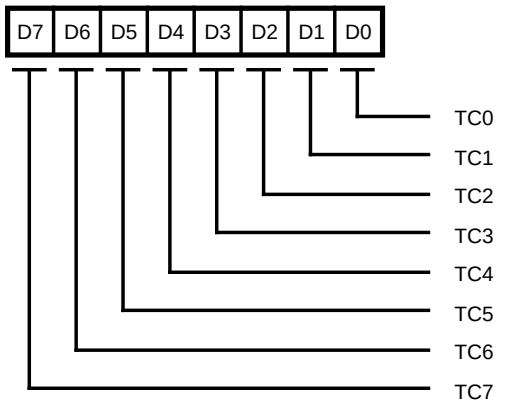



**Figure 47. CTC Time Constant Word**

### Interrupt Vector Word

If one or more of the CTC channels have interrupt enabled, then the Interrupt Vector Word is programmed. Only the five most significant bits of this word are programmed, and bit D0 must be "0". Bits D2-D1 are automatically modified by the CTC channels after responding with an interrupt vector (Figure 48).

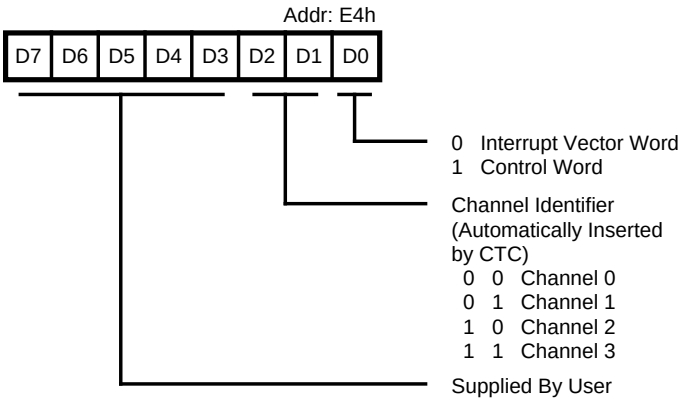



**Figure 48. CTC Interrupt Vector Word**

## SCC REGISTERS

For more detailed information, please refer to the Z8030/ Z8530 SCC Technical Manual.

**Note:**
The Address for the Control/Status Register is E8h. The Address for the Data Register is E9h.

### Read Registers

The SCC contains eight read registers. To read the contents of a register (rather than RR0), the program must first initialize a pointer to WR0 in exactly the same manner as a write operation. The next I/O read cycle will place the contents of the selected read registers onto the data bus (Figure 49).

**Table 2. SCC Read Registers**

| Bit | Description |
|---|---|
| RR0 | Transmit and Receive buffer status and external status. |
| RR1 | Special Receive Condition status. |
| RR2 | Interrupt vector (modified if VIS Bit in WR9 is set). |
| RR3 | Interrupt pending bits. |
| RR6 | SDLC FIFO byte counter lower byte (only when enabled). |

| Bit | Description |
|---|---|
| RR7 | SDLC FIFO byte count and status (only when enabled). |
| RR8 | Receive buffer. |
| RR10 | Miscellaneous status bits. |
| RR12 | Lower byte of baud rate. |
| RR13 | Upper byte of baud rate generator time constant. |
| RR15 | External Status interrupt information. |

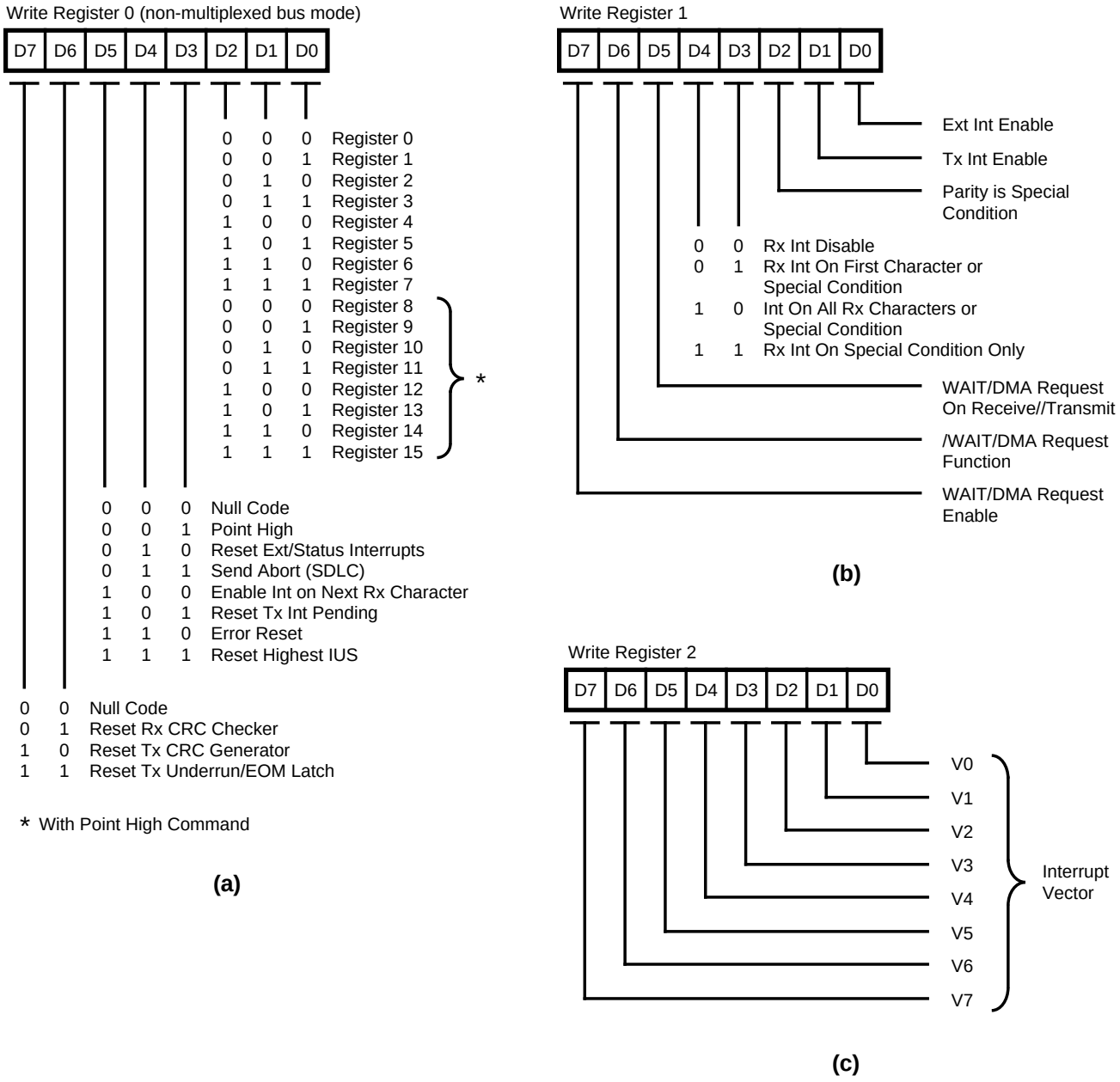



**Figure 50. Write Register Bit Functions**

## PIA Control Registers

PIA1 Data Direction Register (P1DDR, I/O Address E0h), PIA1 Data Port (P1DP, I/O address E1h), PIA2 Data Direction Register (P2DDR, I/O Address E2h) and PIA2 Data Register (P2DP, I/O Address E3h). These four registers are shown in Figures 51-54. Note that if the CTC/PIA bit in the System Configuration Register is set to one, the CTC I/O functions override the PIA1 function, and programming of P1DDR is ignored.

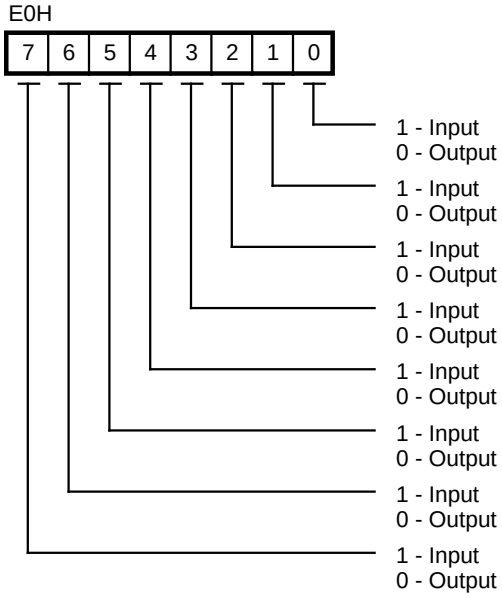



**Figure 51. PIA 1 Data Direction Register**

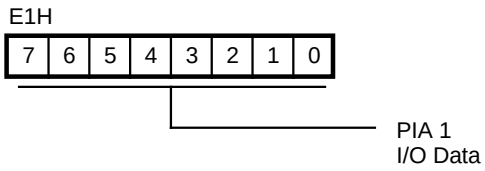



**Figure 52. PIA 1 Data Register**

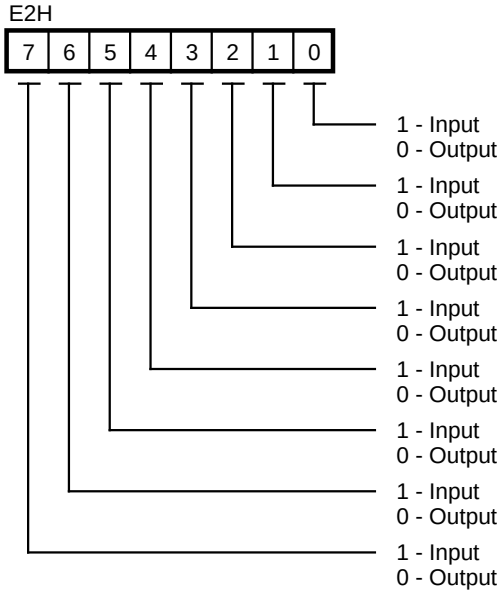



**Figure 53. PIA 2 Data Direction Register**

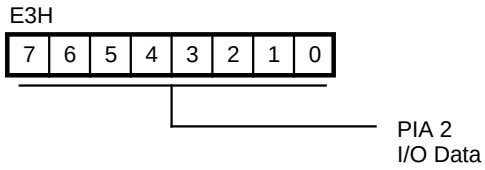



**Figure 54. PIA 2 Data Register**

The Data Port is the register to/from the 8-bit parallel port. At power on Reset, they are initialized to 1.

The Data Direction Register has eight control bits. Individual bits specify each bit's direction. When the bit is set to a "1", the bit becomes an input, otherwise it is an output. On reset, these registers are initialized to 1, resulting in all lines being inputs.

## REGISTERS FOR SYSTEM CONFIGURATION

There are four registers to determine system configuration with the Z181. These registers are: RAM upper boundary address register (RAMUBR, I/O address EAh), RAM lower boundary address register (RAMLBR, I/O address EBh), ROM address boundary register (ROMBR, I/O address ECh) and System Configuration Register (SCR, I/O address EDh).

### ROM Address Boundary Register (ROMBR, I/O Address ECh)

This register specifies the address range for the /ROMCS signal. When accessed memory addresses are less than or equal to the value programmed in this register, the /ROMCS signal is asserted (Figure 55).

The A18 signal from the CPU is obtained before it is multiplexed with "TOUT". This signal can be forced to "1" (inactive state) by setting Bit D5 of the System Configuration Register, to allow the user to overlay the RAM area over the ROM area. At power-up reset, this register contains all 1's so that /ROMCS is asserted for all addresses.

### RAM Lower Boundary Address Register (RAMLBR, I/O Address EBh) and RAM Upper Boundary Address Register (RAMUBR, I/O Address EAh)

These two registers specify the address range for the /RAMCS signal. When accessed memory addresses are less than or equal to the value programmed in the RAMUBR and greater than or equal to the value programmed in the RAMLBR, /RAMCS is asserted. (Figure 13) The A18 signal from the CPU is taken before it is multiplexed with "$T_{OUT}$". In the case that these register are programmed to overlap, /ROMCS takes priority over /RAMCS (/ROMCS is asserted and /RAMCS is inactive).

Chip Select signals are going active for the address range:

/ROMCS: (ROMBR) ≥ A19-A12 ≥ 0
/RAMCS: (RAMUBR) ≥ A19-A12 > (RAMLBR)

These registers are set to "FFh" at power-on Reset, and the boundary addresses of ROM and RAM are the following:

ROM lower boundary address
(fixed) = 00000h

ROM upper boundary address
(ROMBR register) = 0FFFFFh

RAM lower boundary address
(RAMLBR register) = 0FFFFFh

RAM upper boundary address
(RAMUBR register) = 0FFFFFh

Since /ROMCS takes priority over /RAMCS, the latter will never be asserted until the value in the ROMBR and RAMLBR registers are re-initialized to lower values.

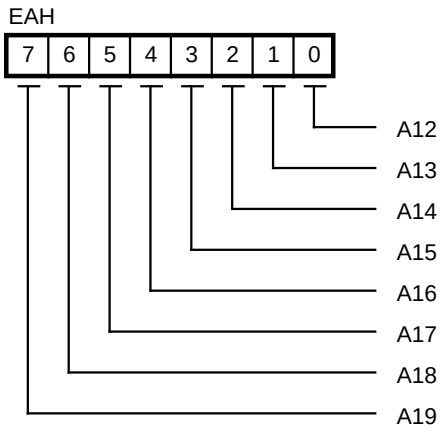



**Figure 55. RAM Upper Boundary Register**

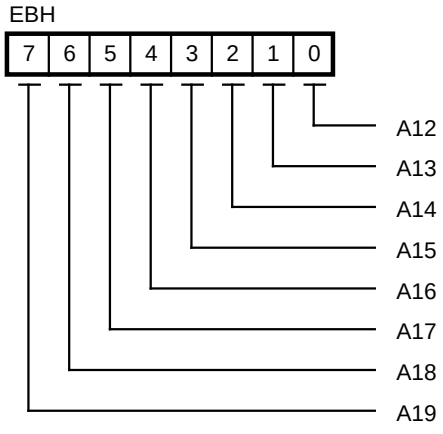



**Figure 56. RAM Lower Boundary Register**

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Voltage on $V_{CC}$ with respect to $V_{SS}$ | –0.3V to +7.0V |
| Voltages on all inputs with respect to $V_{SS}$ | –0.3V to $V_{CC}$ +0.3V |
| Storage Temperature | –65°C to +150°C |
| Operating Ambient Temperature | See Ordering Information |

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## STANDARD TEST CONDITIONS

The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin (Figure 59).

Available operating temperature range is: E = –40°C to +100°C

Voltage Supply Range: +4.50V ≤ Vcc ≤ + 5.50V

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 150 pF for the data bus and 100 pF for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points). Maximum capacitive load for CLK is 125 pF.

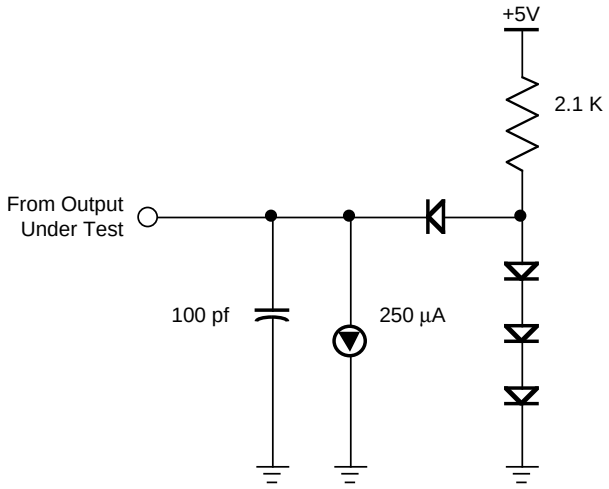
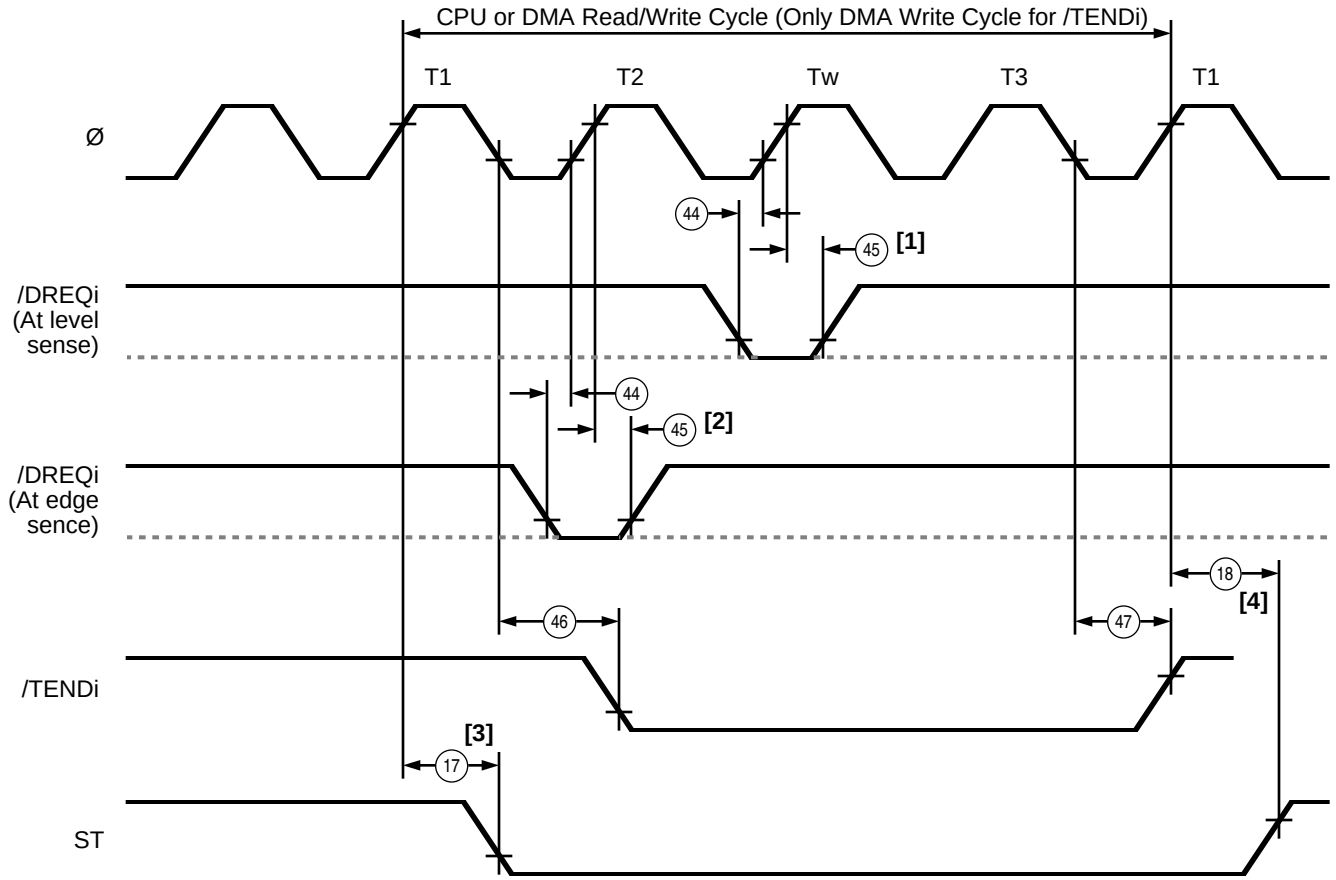



**Figure 59. Standard Test Circuit**

## AC CHARACTERISTICS (Continued)
Z180 MPU Timing




DMA Control Signals
[1] tDRQS and tDRQH are specified for the rising edge of clock followed by T3.
[2] tDRQS and tDRQH are specified for the rising edge of clock.
[3] DMA cycle starts.
[4] CPU cycle starts.

**Figure 63. DMA Control Signals**

## AC CHARACTERISTICS (Continued)
Z180 MPU Timing

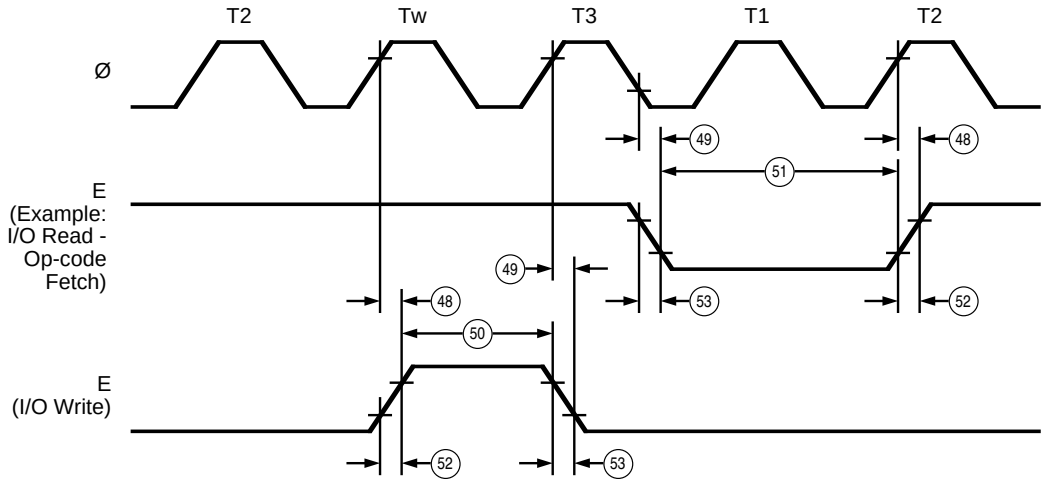



**Figure 65. E Clock Timing**
(Minimum timing example of PWEL and PWEH)

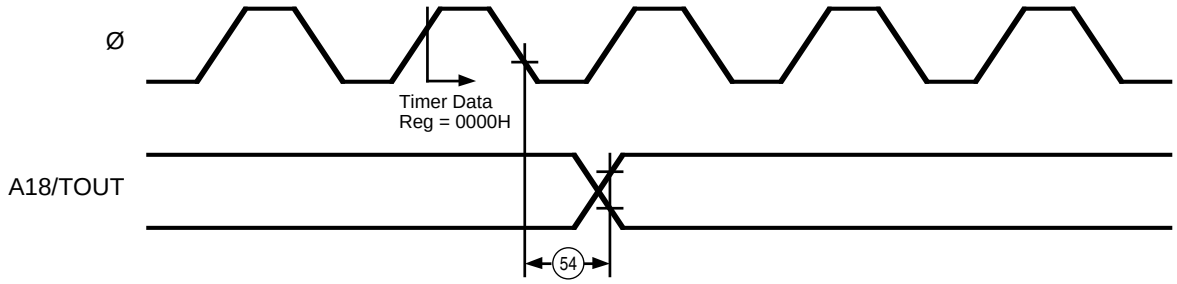



**Figure 66. Timer Output Timing**

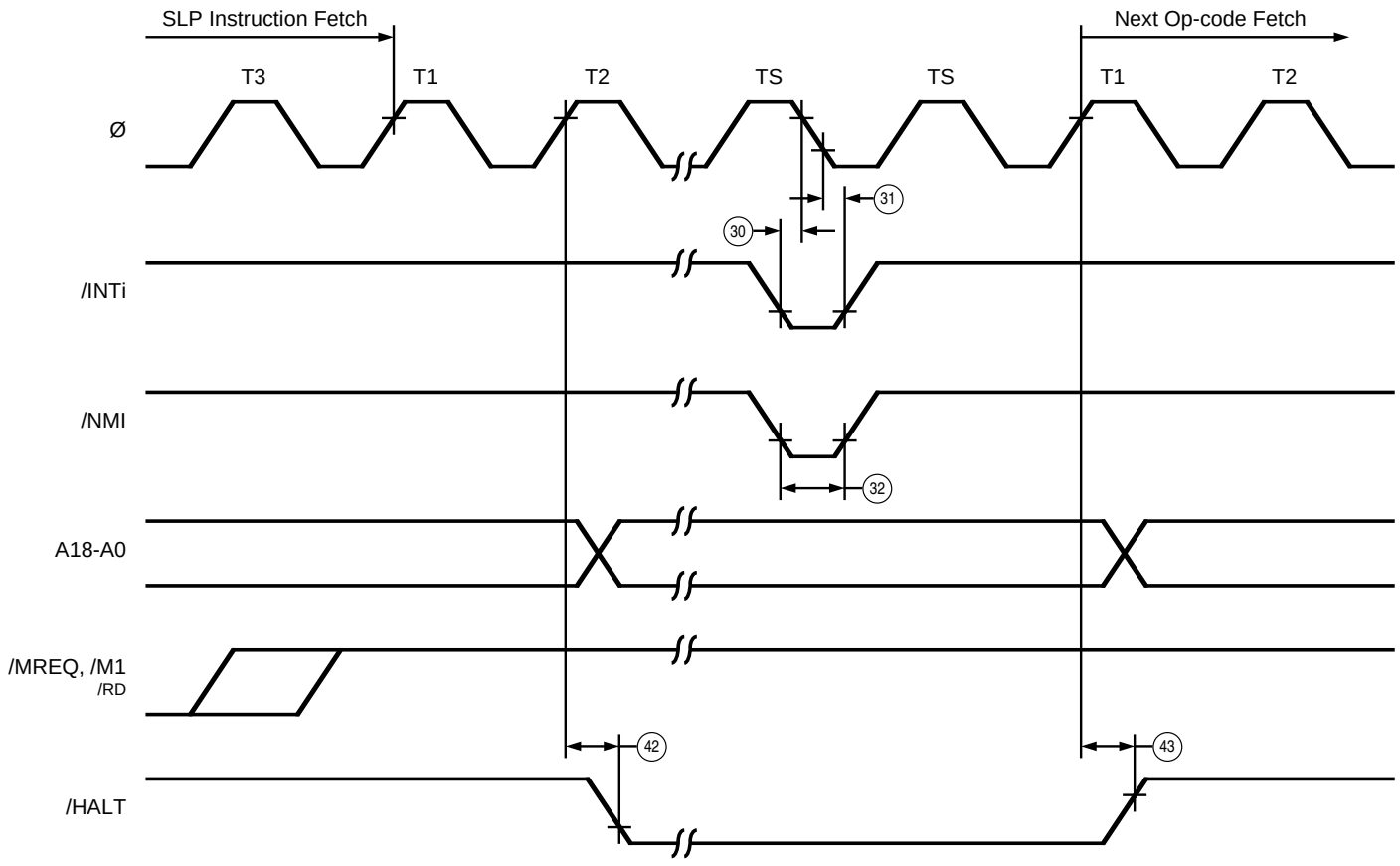



**Figure 67. SLP Execution Cycle**

## AC CHARACTERISTICS (Continued)
Z180™ MPU Timing

**Table A. Z180 CPU &180 Peripherals Timing** (Continued)

| No | Symbol | Parameter | Z8018110 Min | Z8018110 Max | Unit |
|---|---|---|---|---|---|
| 47 | tTED2 | Clock Fall to /TENDi Rise Delay | | 50 | ns |
| 48 | tED1 | Clock Rise to E Rise Delay | | 60 | ns |
| 49 | tED2 | Clock Edge to E Fall Delay | | 60 | ns |
| 50 | PWEH | E Pulse Width (High) | 55 | | ns |
| 51 | PWEL | E Pulse Width (Low) | 110 | | ns |
| 52 | tEr | Enable Rise Time | | 20 | ns |
| 53 | tEf | Enable Fall Time | | 20 | ns |
| 54 | tTOD | Clock Fall to Timer Output Delay | | 150 | ns |
| 55 | tSTDI | CSI/O Tx Data Delay Time (Internal Clock Operation) | | 150 | ns |
| 56 | tSTDE | CSI/O Tx Data Delay Time (External Clock Operation) | | 7.5tcyc+150 | ns |
| 57 | tSRSI | CSI/O Rx Data Setup Time (Internal Clock Operation) | 1 | | tcyc |
| 58 | tSRHI | CSI/O Rx Data Hold Time (Internal Clock Operation) | 1 | | tcyc |
| 59 | tSRSE | CSI/O Rx Data Setup Time (External Clock Operation) | 1 | | tcyc |
| 60 | tSRHE | CSI/O Rx Data Hold Time (External Clock Operation) | 1 | | tcyc |
| 61 | tRES | /RESET Setup Time to Clock Fall | 80 | | ns |
| 62 | tREH | /RESET Hold Time from Clock Fall | 50 | | ns |
| 63 | tOSC | Oscillator Stabilization Time | | 20 | ms |
| 64 | tEXr | External Clock Rise Time (EXTAL) | | 25 | ns |
| 65 | tEXf | External Clock Fall Time (EXTAL) | | 25 | ns |
| 66 | tRr | /RESET Rise Time | | 50 | ns |
| 67 | tRf | /RESET Fall Time | | 50 | ns |
| 68 | tIr | Input Rise Time (Except EXTAL, /RESET) | | 100 | ns |
| 69 | tIf | Input Fall Time (Except EXTAL, /RESET) | | 100 | ns |
| 70 | TdCS(A) | Address Valid to /ROMCS, /RAMCS Valid Delay | | 20 | ns |

## AC CHARACTERISTICS (Continued)
SCC System Timing

**Table E. SCC System Timing Parameters**

| No | Symbol | Parameter | Z8018110 Min | Z8018110 Max | Unit | Note |
|---|---|---|---|---|---|---|
| 1 | TdRxC(REQ) | /RxC to /W//REQ Valid | 8 | 12 | TcC | [E2] |
| 2 | TdRxC(W) | /RxC to Wait inactive | 8 | 14 | TcC | [E1,2] |
| 3 | TdRxC(SY) | /RxC to /SYNC Valid | 4 | 7 | TcC | [E2] |
| 4 | TdRxC(INT) | /RxC to /INT Valid | 10 | 16 | TcC | [E1,2] |
| 5 | TdTxC(REQ) | /TxC to /W//REQ Valid | 5 | 8 | TcC | [E3] |
| 6 | TdTxC(W) | /TxC to Wait inactive | 5 | 11 | TcC | [E1,3] |
| 7 | TdRxC(DRQ) | /TxC to /DTR//REQ Valid | 4 | 7 | TcC | [E3] |
| 8 | TdTxC(INT) | /TxC to /INT Valid | 6 | 10 | TcC | [E1,3] |
| 9 | TdSY(INT) | /SYNC to /INT Valid | 2 | 6 | TcC | [E1] |
| 10 | TdEXT(INT) | /DCD or /CTS to /INT Valid | 2 | 6 | TcC | [E1] |

**Notes for Table E:**
[E1] Open-drain output, measured with open-drain test load.
[E2] /RXC is /RTxC or /TRxC, whichever is supplying the receiver clock.
[E3] /TXC is /TRxC or /RTxC, whichever is supplying the transmitter clock.

## AC CHARACTERISTICS (Continued)
PIA General-Purpose I/O Port Timing

Figure 73 shows the timing for the PIA ports. Parameters referenced in this figure appear in Table F.

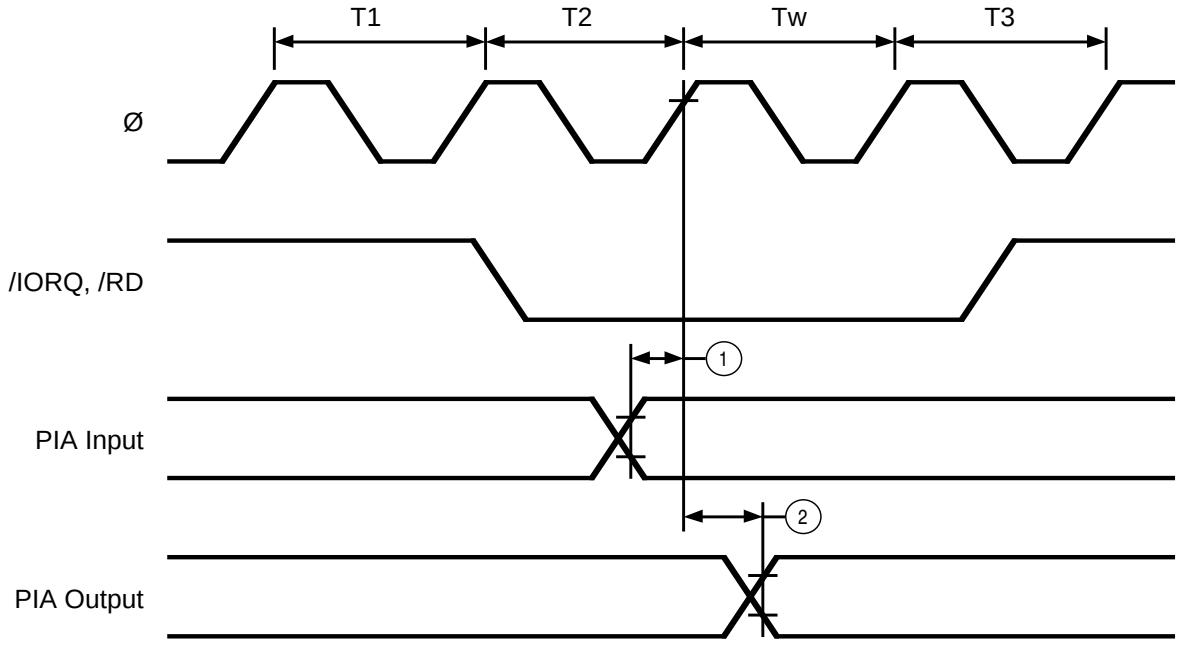



**Figure 73. PIA Timing**

**Table F. PIA General-Purpose I/O Timing Parameters**

| No | Symbol | Parameter | Z8018110 Min | Z8018110 Max | Unit |
|---|---|---|---|---|---|
| 1 | TsPIA(C) | PIA Data Setup time to Clock Rise | 10 | | ns |
| 2 | TdCr(PIA) | Clock Rise to PIA Data Valid Delay | | 50 | ns |

## AC CHARACTERISTICS (Continued)
### Interrupt Daisy-Chain Timing

Figure 74 shows the interrupt daisy-chain timing. Parameters referenced in this figure appear in Table G.

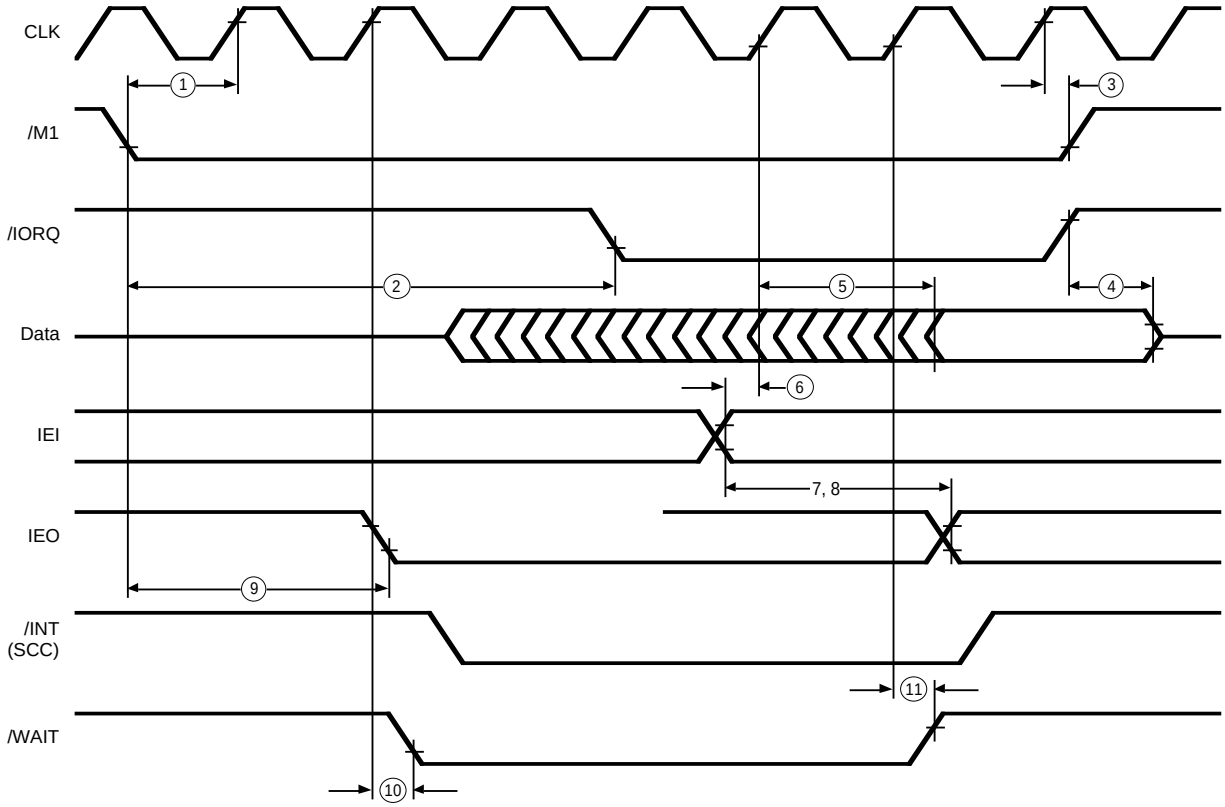
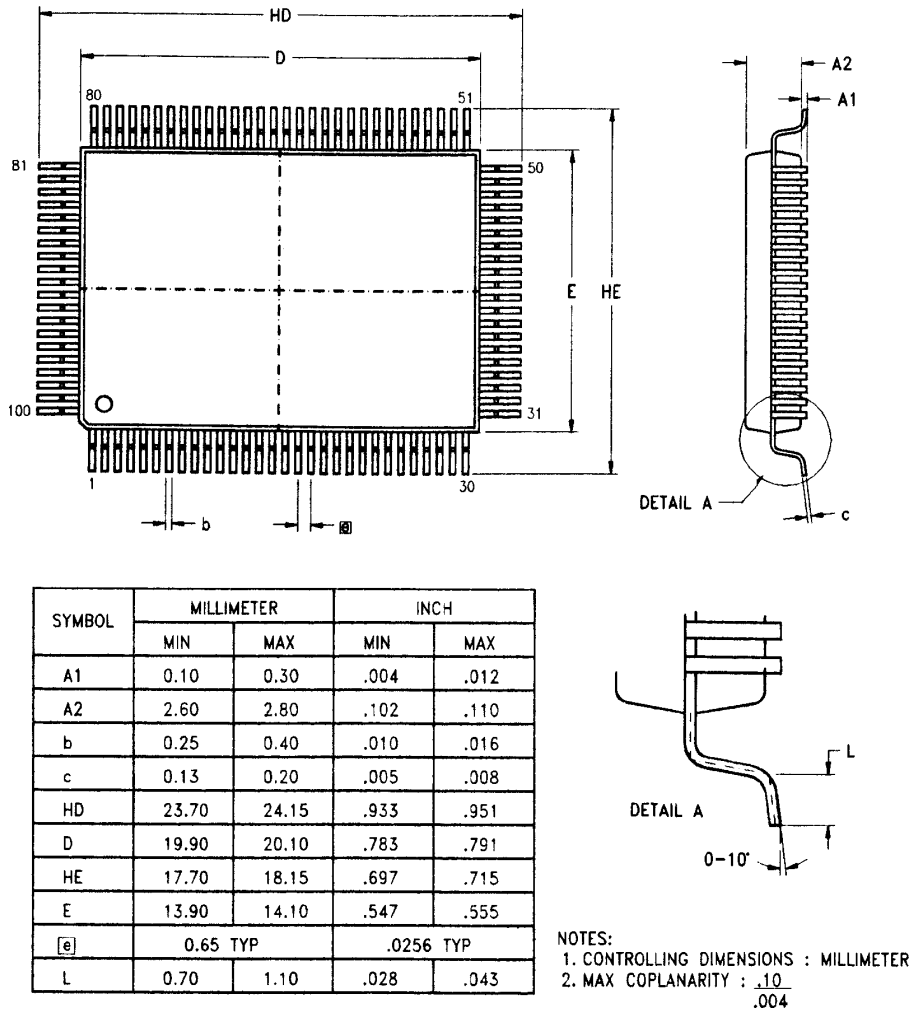



**Figure 74. Interrupt Daisy-Chain Timing**

**Table G. Interrupt Daisy-Chain Timing Parameters**

| No | Symbol | Parameter | Z8018110 Min | Z8018110 Max | Unit |
|---|---|---|---|---|---|
| 1 | TsM1(Cr) | /M1 Fall to Clock Rise Setup Time | 20 | | ns |
| 2 | TsM1(IO)INTA | /M1 Fall to /IORQ Fall Setup Time (During INTACK Cycle) | 2TcC | | ns |
| 3 | Th | Hold Time | 0 | | |
| 4 | TdM1r(DOz) | /M1 Rise to Data Out Float Delay | 0 | | ns |
| 5 | TdCr(DO) | Clock Rise to Data Out Delay | | | |
| 6 | TsIEI(TW4) | IEI to $T_{W4}$ Rise Setup Time | 95 | | ns |
| 7 | TdIElf(IEOf) | IEI Fall to IEO Fall Delay | | | |
| 8 | TdIElr(IEOr) | IEO Rise to IEO Rise Delay | | | |
| 9 | TdM1f(IEOf) | /M1 Fall to IEO Fall Delay | | | |
| 10 | TdCWA(f)INTA | Clock Rise to /WAIT Fall Delay | | | |
| 11 | TdCWA(r)INTA | Clock Rise to /WAIT Rise Delay | | | |

## PACKAGE INFORMATION




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A1 | 0.10 | 0.30 | .004 | .012 |
| A2 | 2.60 | 2.80 | .102 | .110 |
| b | 0.25 | 0.40 | .010 | .016 |
| c | 0.13 | 0.20 | .005 | .008 |
| HD | 23.70 | 24.15 | .933 | .951 |
| D | 19.90 | 20.10 | .783 | .791 |
| HE | 17.70 | 18.15 | .697 | .715 |
| E | 13.90 | 14.10 | .547 | .555 |
| e | 0.65 TYP | | .0256 TYP | |
| L | 0.70 | 1.10 | .028 | .043 |

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. MAX COPLANARITY : .10 / .004

**100-Pin QFP Package Diagram**

## ORDERING INFORMATION

### Z80181 (10 MHz)

**Extended Temperature**

100-Pin QFP

Z8018110FEC

### Package

**Longer Lead Time**

F = Plastic Quad Flat Pack

### Temperature

**Longer Lead Time**

E = –40°C to +100°C

### Environmental

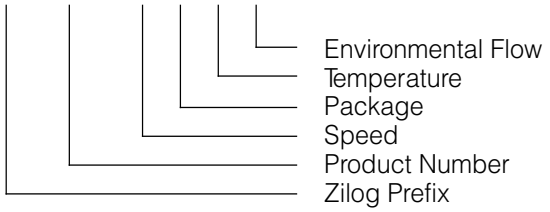
C = Plastic Standard

### Speed

10 = 10 MHz

### Example:

**Z 80181 10 F E C** is a Z80181, 10 MHz, QFP, –40°C to +100°C, Plastic Standard Flow



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