Renesas Electronics America Inc - R5F10NLEDFB#30 Datasheet

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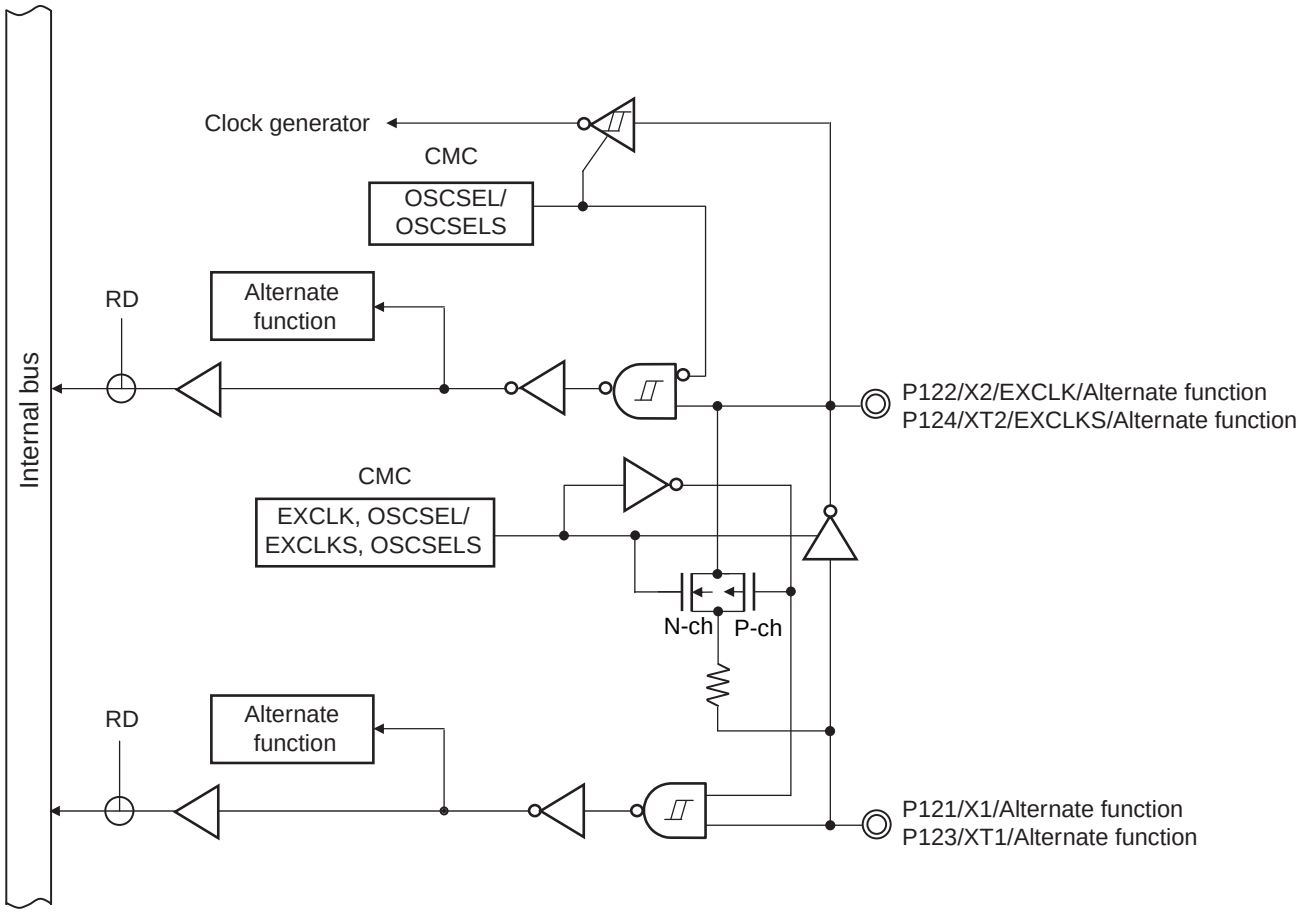
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, IrDA, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 5.5V
Data Converters	A/D 4x10b, 4x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10nledfb-30

Figure 2-3. Pin Block Diagram for Pin Type 2-2-1



Remark For alternate functions, see **2.1 Port Function**.

4.3.8 Peripheral I/O redirection register (PIOR0)

This register is used to specify whether to enable or disable the peripheral I/O redirect function.

This function is used to switch ports to which alternate functions are assigned.

Use the PIOR0 register to assign a port to the function to redirect and enable the function.

In addition, can be changed the settings for redirection until its function enable operation.

The PIOR0 register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Figure 4-8. Format of Peripheral I/O Redirection Register (PIOR0)

Address: F0077H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIOR0	0	0	0	PIOR04	PIOR03	PIOR02	PIOR01	PIOR00

Bit	Function	100-pin		80-pin		64-pin	
		Setting value		Setting value		Setting value	
		0	1	0	1	0	1
PIOR04	INTP0[Note]	P137	P70	P137	P70	P137	P70
	INTP1	P125	P71	P125	P71	P125	P71
	INTP2	P07	P72	P07	P72	P07	P72
	INTP3	P05	P73	P05	P73	P05	P73
	INTP4	P04	P74	P04	P74	P06	P74
	INTP5	P02	P75	P02	P75	P30	–
	INTP6	P41	P76	P41	P76	P13	–
	INTP7	P42	P77	–	P77	P16	–
PIOR03	PCLBUZ0	P43	P33	–	P33	P43	P74
	PCLBUZ1	P41	P32	P41	P32	P125	P73
	RTCOUT	P150	P62	P150	P62	P43	P62
PIOR02	SO10/TXD1	P04	P82	P04	P82	P14	–
	SI10/RXD1/SDA10	P03	P81	P03	P81	P13	–
	SCK10/SCL10	P02	P80	P02	P80	P12	–
PIOR01	SO00/TXD0	P07	P17	P07	P17	P07	P17
	SI00/RXD0/SDA00	P06	P16	P06	P16	P06	P16
	SCK00/SCL00	P05	P15	P05	P15	P05	P15
PIOR00	TI00/TO00	P43	P60	–	P60	P43	P60
	TI01/TO01	P41	P61	P41	P61	P72	P61
	TI02/TO02	P07	P62	P07	P62	P07	P62
	TI03/TO03	P06	P127	P06	P127	P06	P127
	TI04/TO04	P05	P126	P05	P126	P05	P126
	TI05/TO05	P04	P125	P04	P125	P125	–
	TI06/TO06	P03	P31	P03	P31	P31	–
	TI07/TO07	P02	P30	P02	P30	P30	–

Note Uses a battery backup function and the P137 pin is enabled when supplying power from VBAT. When the INTP0 function is assigned to P70, note that the interrupt function is disabled when supplying power from VBAT.

6.3.4 Sub clock operation mode control register (SCMC)

This register is used to set the operating mode of the XT1/P123 and XT2/EXCLKS/P124 pins, and to select the gain of the oscillator.

After release from an RTC power-on reset or a reset from any other source, the SCMC register can be written only once by an 8-bit memory manipulation instruction. This register can be read by an 8-bit memory manipulation instruction.

Generation of the RTC power-on reset signal clears this register to 00H. This register is not reset by other reset sources (including the power-on reset of the internal V_{DD} power supply).

Figure 6 - 5 Format of Sub clock operation mode control register (SCMC)

Address: F0384H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SCMC	0	0	EXCLKS	OSCSELS	0	AMPHS1	AMPHS0	0

EXCLKS	OSCSELS	Subsystem clock pin operation mode	XT1/P123 pin	XT2/EXCLKS/P124 pin
0	0	Input port mode	Input port	
0	1	XT1 oscillation mode	Crystal oscillator connection	
1	0	Input port mode	Input port	
1	1	External clock input mode	Input port	External clock input

AMPHS1	AMPHS0	XT1 oscillator oscillation mode selection
0	0	Low-power consumption oscillation (default)
0	1	Normal oscillation
1	0	Ultra-low power consumption oscillation
1	1	Setting prohibited

Note The EXCLKS, OSCSELS, AMPHS1, and AMPHS0 bits are only initialized by an RTC power-on reset; they retain their values following a reset due to another source (including the power-on reset of the internal V_{DD} power supply).

Caution 1. After the CPU is released from the reset state, the SCMC register can be written only once by an 8-bit memory manipulation instruction. When using the SCMC register with its initial value (00H), be sure to set the register to 00H after a reset ends in order to prevent malfunction due to a program loop.

Caution 2. After the CPU is released from the reset state, set the SCMC register before XT1 oscillation is started as set by the sub clock operation status control register (SCSC).

Caution 3. Specify the settings for the AMPHS1 and AMPHS0 bits while f_{IH} is selected as f_{CLK} after a reset ends (before f_{CLK} is switched to f_{MX}).

Caution 4. Count the f_{XT} oscillation stabilization time by using software.

Caution 5. After the CPU is released from the reset state following writing to the SCMC register and then a reset other than an RTC power-on reset, set the same value as the value before the reset to prevent incorrect operation in the case of an endless loop or runaway execution.

Caution 6. The XT1 oscillator is a circuit with low amplification in order to achieve low-power consumption. Note the following points when designing the circuit.

• Pins and circuit boards include parasitic capacitance. Therefore, perform oscillation evaluation using a circuit board to be actually used and confirm that there are no problems.

• When using the ultra-low power consumption oscillation (AMPHS1, AMPHS0 = 1, 0) as the mode of the XT1 oscillator, evaluate the resonators described in 6.7 Resonator and Oscillator Constants.

• Make the wiring between the XT1 and XT2 pins and the resonators as short as possible, and minimize the parasitic capacitance and wiring resistance. Note this particularly when the ultra-low

8.3.7 Timer channel start register m (TSm)

The TSm register is a trigger register that is used to initialize timer count register mn (TCRmn) and start the counting operation of each channel.

When a bit of this register is set to 1, the corresponding bit of timer channel enable status register m (TEm) is set to 1. The TSmn, TSHm1, TSHm3 bits are immediately cleared when operation is enabled (TEmn, TEHm1, TEHm3 = 1), because they are trigger bits.

The TSm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TSm register can be set with a 1-bit or 8-bit memory manipulation instruction with TSmL.

Reset signal generation clears this register to 0000H.

Figure 8-18. Format of Timer Channel Start register m (TSm)

Address: F01B2H, F01B3H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSm	0	0	0	0	TSHm3	0	TSHm1	0	TSm7	TSm6	TSm5	TSm4	TSm3	TSm2	TSm1	TSm0

TSHm3	Trigger to enable operation (start operation) of the higher 8-bit timer when channel 3 is in the 8-bit timer mode
0	No trigger operation
1	The TEHm3 bit is set to 1 and the count operation becomes enabled. The TCRm3 register count operation start in the interval timer mode in the count operation enabled state (see **Table 8-5** in **8.5.2 Start timing of counter**).

TSHm1	Trigger to enable operation (start operation) of the higher 8-bit timer when channel 1 is in the 8-bit timer mode
0	No trigger operation
1	The TEHm1 bit is set to 1 and the count operation becomes enabled. The TCRm1 register count operation start in the interval timer mode in the count operation enabled state (see **Table 8-5** in **8.5.2 Start timing of counter**).

TSmn	Operation enable (start) trigger of channel n
0	No trigger operation
1	The TEmn bit is set to 1 and the count operation becomes enabled. The TCRmn register count operation start in the count operation enabled state varies depending on each operation mode (see **Table 8-5** in **8.5.2 Start timing of counter**). This bit is the trigger to enable operation (start operation) of the lower 8-bit timer for TSm1 and TSm3 when channel 1 or 3 is in the 8-bit timer mode.

Cautions 1. Be sure to clear bits 15 to 12, 10, 8 to "0"

2. When switching from a function that does not use TImn pin input to one that does, the following wait period is required from when timer mode register mn (TMRmn) is set until the TSmn (TSHm1, TSHm3) bit is set to 1.

When the TImn pin noise filter is enabled (TNFENnm = 1): Four cycles of the operation clock (f_{MCK})

When the TImn pin noise filter is disabled (TNFENnm = 0): Two cycles of the operation clock (f_{MCK})

Remarks 1. When the TSm register is read, 0 is always read.

2. m: Unit number (m = 0), n: Channel number (n = 0 to 7)

8.8.3 Operation as input pulse interval measurement

The count value can be captured at the TImn valid edge and the interval of the pulse input to TImn can be measured. In addition, the count value can be captured by using software operation (TSmn = 1) as a capture trigger while the TEmn bit is set to 1.

The pulse interval can be calculated by the following expression.

TImn input pulse interval = Period of count clock × ((10000H × TSRmn: OVF) + (Capture value of TDRmn + 1))

Caution The TImn pin input is sampled using the operating clock selected with the CKSmn bit of timer mode register mn (TMRmn), so an error of up to one operating clock cycle occurs.

Timer count register mn (TCRmn) operates as an up counter in the capture mode.

When the channel start trigger bit (TSmn) of timer channel start register m (TSm) is set to 1, the TCRmn register counts up from 0000H in synchronization with the count clock.

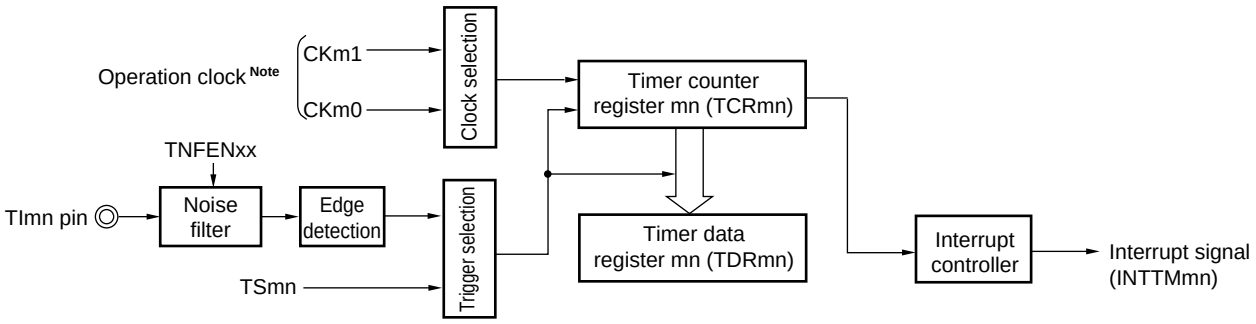
When the TImn pin input valid edge is detected, the count value of the TCRmn register is transferred (captured) to timer data register mn (TDRmn) and, at the same time, the TCRmn register is cleared to 0000H, and the INTTMmn is output. If the counter overflows at this time, the OVF bit of timer status register mn (TSRmn) is set to 1. If the counter does not overflow, the OVF bit is cleared. After that, the above operation is repeated.

As soon as the count value has been captured to the TDRmn register, the OVF bit of the TSRmn register is updated depending on whether the counter overflows during the measurement period. Therefore, the overflow status of the captured value can be checked.

If the counter reaches a full count for two or more periods, it is judged to be an overflow occurrence, and the OVF bit of the TSRmn register is set to 1. However, a normal interval value cannot be measured for the OVF bit, if two or more overflows occur.

Set the STSmn2 to STSmn0 bits of the TMRmn register to 001B to use the valid edges of TImn as a start trigger and a capture trigger.

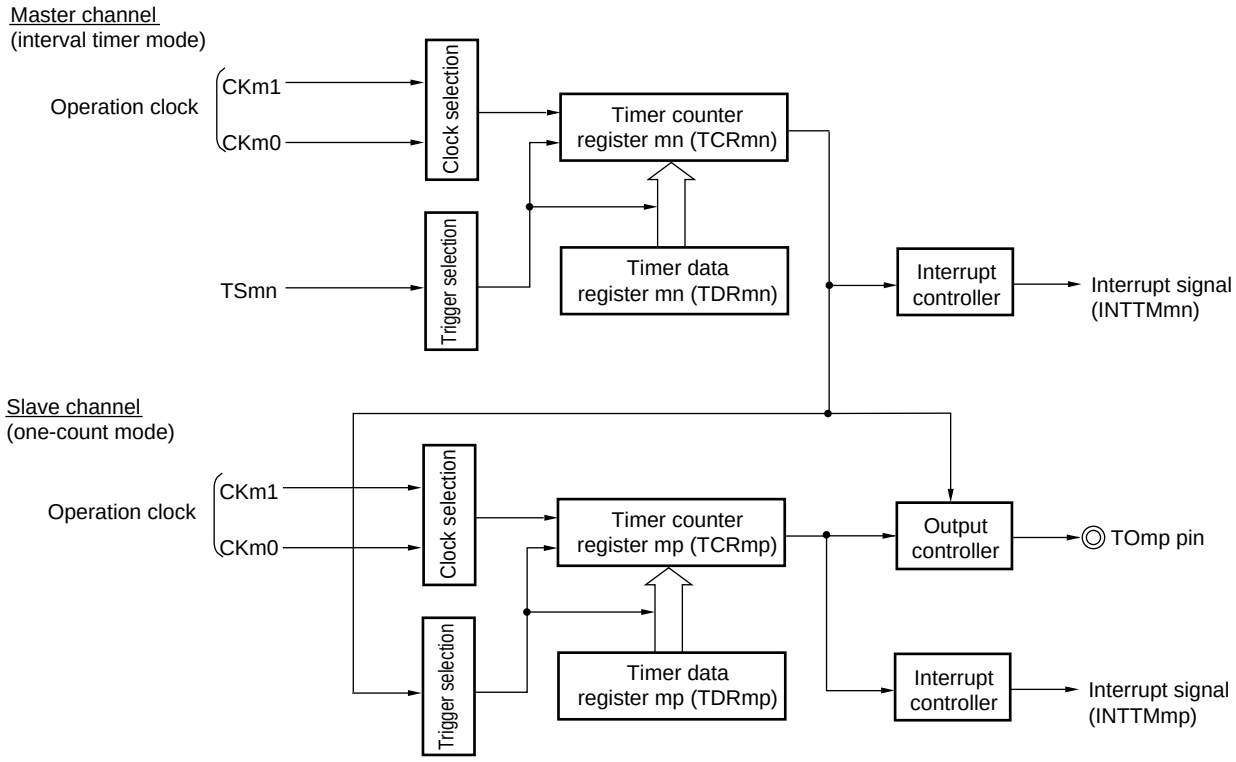
Figure 8-53. Block Diagram of Operation as Input Pulse Interval Measurement



Note When channels 1 and 3, the clock can be selected from CKm0, CKm1, CKm2 and CKm3.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

Figure 8-70. Block Diagram of Operation as PWM Function



Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4, 6)
p: Slave channel number (n < p ≤ 7)

9.2.18 RTC control register 1 (RCR1)

The RCR1 register is used in both calendar count mode and in binary count mode.
Bits AIE, PIE, and PES are updated synchronously with the count source. When the RCR1 register is modified, check that all the bits have been updated before proceeding to the next processing.

Figure 9 - 31 Format of RTC Control Register 1 (RCR1)

Address: F05A3H After reset: Undefined R/W

Symbol	7	6	5	4	3	2	1	0
RCR1	PES				RTCOS	PIE	0	AIE

PES	Periodic Interrupt Select
0110	A periodic interrupt is generated every 1/256 second.
0111	A periodic interrupt is generated every 1/128 second.
1000	A periodic interrupt is generated every 1/64 second.
1001	A periodic interrupt is generated every 1/32 second.
1010	A periodic interrupt is generated every 1/16 second.
1011	A periodic interrupt is generated every 1/8 second.
1100	A periodic interrupt is generated every 1/4 second.
1101	A periodic interrupt is generated every 1/2 second.
1110	A periodic interrupt is generated every 1 second.
1111	A periodic interrupt is generated every 2 seconds.
Other than above	No periodic interrupts are generated.
These bits specify the period for the periodic interrupt. A periodic interrupt is generated with the period specified by these bits.	

RTCOS	RTCOUT Output Select
0	RTCOUT outputs 1 Hz.
1	RTCOUT outputs 64 Hz.
This bit selects the RTCOUT output period. The RTCOS bit must be rewritten while count operation is stopped (the RCR2.START bit is 0) and RTCOUT output is disabled (the RCR2.RTCOE bit is 0). When the RTCOUT is output to an external pin, the RCR2.RTCOE bit must be enabled. About I/O ports, refer to **CHAPTER 4 PORT FUNCTIONS**.	

PIE	Periodic Interrupt Control
0	A periodic interrupt request is disabled.
1	A periodic interrupt request is enabled.
This bit enables or disabled a periodic interrupt.	

AIE	Alarm Interrupt Control
0	An alarm interrupt request is disabled.
1	An alarm interrupt request is enabled.
This bit enables or disables alarm interrupt requests.	

<R> **Caution Be sure to set the RCKSEL bit to 0.**
This register can only be accessed with an 8-bit memory manipulation instruction.

9.2.19 RTC control register 2 (RCR2)

(1) In calendar count mode:

The RCR2 register is related to hours mode, automatic adjustment function, enabling the RTCOUT output, 30-second adjustment, RTC software reset, and controlling count operation.

Figure 9 - 32 Format of RTC Control Register 2 (RCR2)(In calendar count mode)

Address: F05A5H After reset: Undefined R/W

Symbol	7	6	5	4	3	2	1	0
RCR2	CNTMD	HR24	AADJP	AADJE	RTCOE	ADJ30	RESET	START

CNTMD	Count Mode Select
0	The calendar count mode.
1	The binary count mode.
This bit specifies whether the RTC count mode is operated in calendar count mode or in binary count mode. When setting the count mode, execute an RTC software reset and start again from the initial settings. This bit is updated synchronously with the count source, and its value is fixed before the RTC software reset is completed. For details on initial settings, refer to section 9.3.1, Outline of initial settings of registers after power on.	

HR24	Hours Mode
0	The RTC operates in 12-hour mode.
1	The RTC operates in 24-hour mode.
This bit specifies whether the RTC will operate in 12- or 24-hour mode. Use the START bit to stop counting by the counters before changing the value of the HR24 bit. Do not stop counting (write 0 to the START bit) and change the value of the HR24 bit at the same time.	

AADJP	Automatic Adjustment Period Select
0	The RADJ.ADJ[5:0] setting value is adjusted from the count value of the prescaler every minute.
1	The RADJ.ADJ[5:0] setting value is adjusted from the count value of the prescaler every 10 seconds.
This bit selects the automatic-adjustment period. Set the plus–minus bits (RADJ.PMADJ) to 00b (adjustment is not performed) before changing the value of the AADJP bit. The AADJP bit is set to 0 by an RTC software reset.	

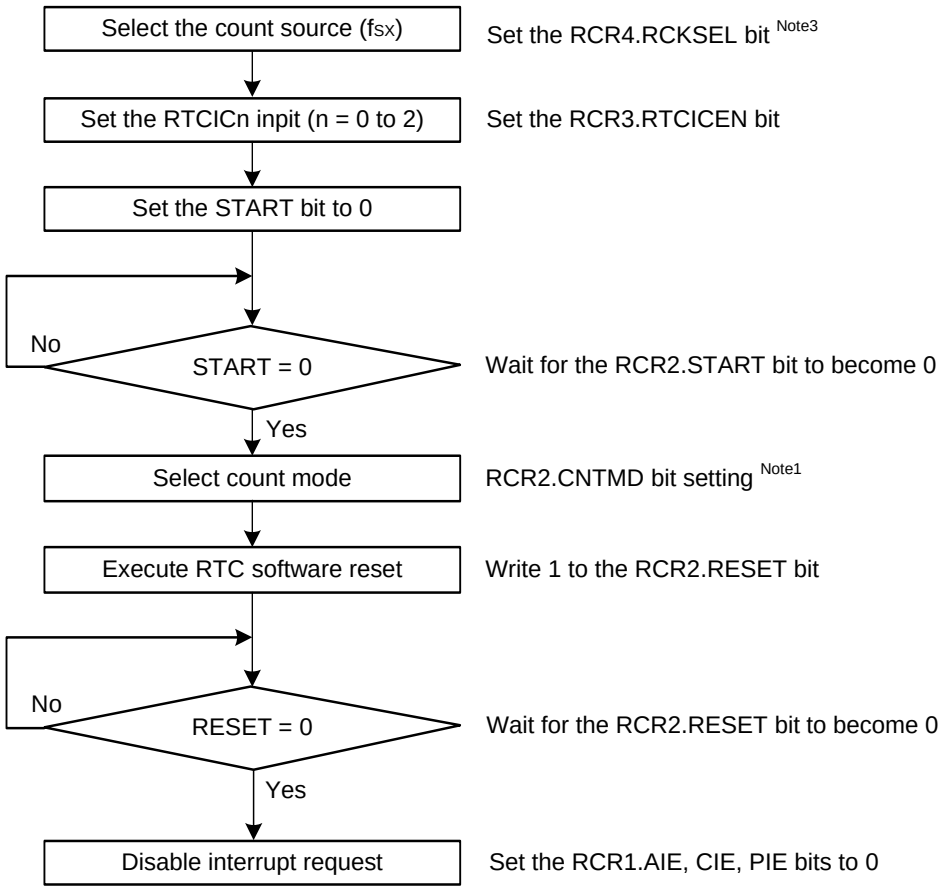
AADJE	Automatic Adjustment Control
0	Automatic adjustment is disabled.
1	Automatic adjustment is enabled.
This bit controls (enables or disables) automatic adjustment. Set the plus–minus bits (RADJ.PMADJ) to 00b (adjustment is not performed) before changing the value of the AADJE bit. The AADJE bit is set to 0 by an RTC software reset.	

RTCOE	RTCOUT Output Control
0	RTCOUT output disabled.
1	RTCOUT output enabled.
This bit enables output of a 1-Hz/64-Hz clock signal from the RTCOUT pin. Use the START bit to stop counting by the counters before changing the value of the RTCOE bit. Do not stop counting (write 0 to the START bit) and change the value of the RTCOE bit at the same time. When RTCOUT is to be output from an external pin, enable the RTCOE bit and set up the port control for the pin.	

9.6.7 Stop procedure

The realtime clock with independent power supply of RL78/I1C is operating from the product power-on.
When it is not used, stop it according to following procedure shown in Figure 9 - 67.

Figure 9 - 67 Stop Setting Procedure



Note 1. This step is not necessary if the count mode has been set concurrently with setting the START bit to 0.
Note 2. Rewriting the RCR2 register with a way of read-modify-writing is prohibited.
Note 3. Be sure to clear the RCR4.RCKSEL bit to 0.

<R>

9.6.8 Caution of shortwave detection function

When supply voltage from the V_{DD} or VBAT type supply voltage pins is shut off, the shortwave detection (RTCICn) function cannot be used.

18.3.1 Peripheral enable register 0 (PER0)

PER0 is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When serial array unit 0 is used, be sure to set bit 2 (SAU0EN) of this register to 1.

When serial array unit 1 is used, be sure to set bit 3 (SAU1EN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears the PER0 register to 00H.

Figure 18-5. Format of Peripheral Enable Register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	7	<6>	<5>	<4>	<3>	<2>	1	<0>
PER0	0	IRDAEN	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN

SAUmEN	Control of serial array unit m input clock supply
0	Stops supply of input clock. • SFR used by the serial array unit m cannot be written. The read value is 00H. However, the SFR is not initialized. Notes 1, 2
1	Enables input clock supply. • SFR used by serial array unit m can be read/written.

Notes 1. To initialize the serial array unit 1 and the SFR used by the serial array unit 1, use bit 3 (SAU1RES) of PRR0.

2. To initialize the serial array unit 0 and the SFR used by the serial array unit 0, use bit 2 (SAU0RES) of PRR0.

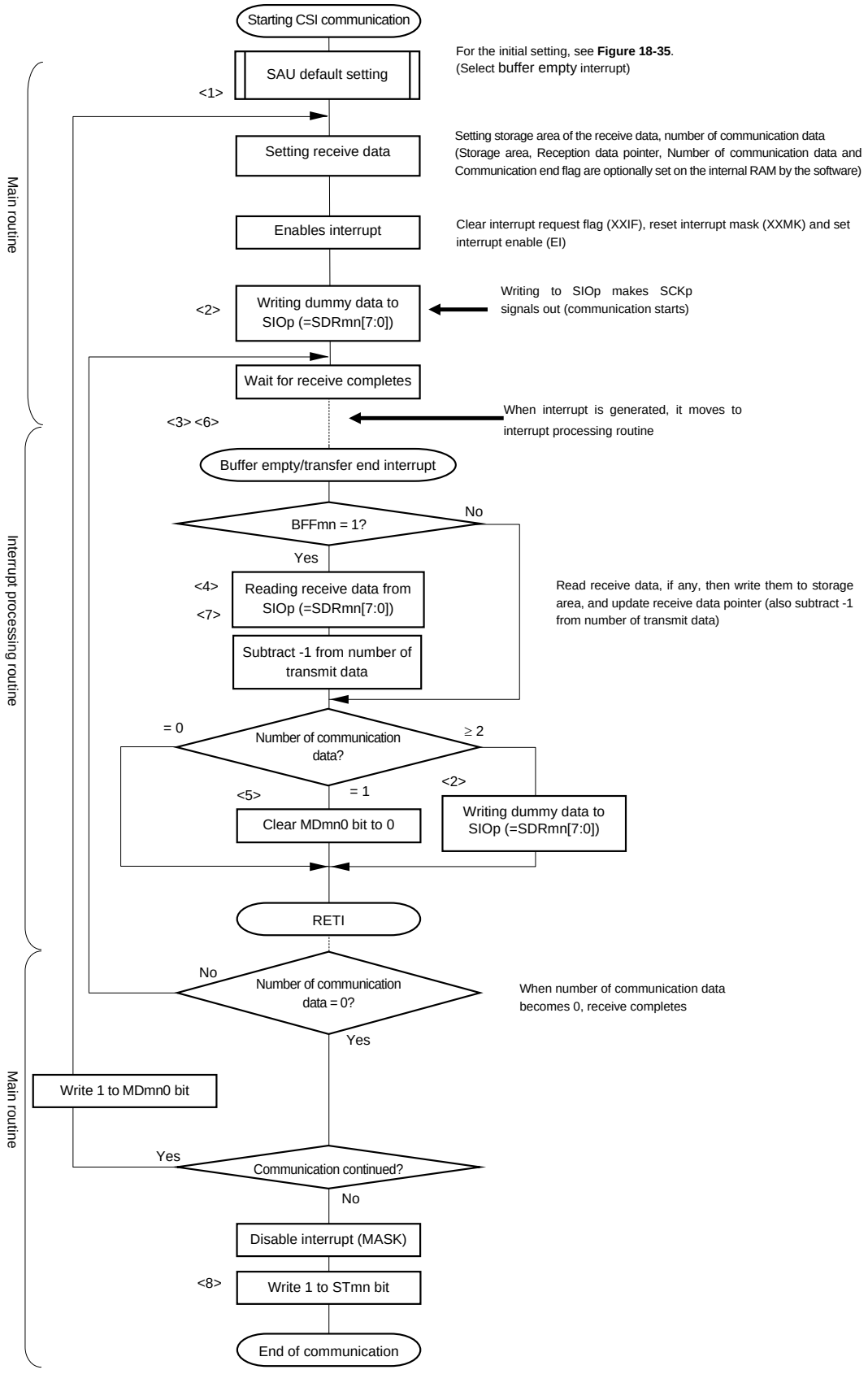
Cautions 1. When setting serial array unit m, be sure to first set the following registers with the SAUmEN bit set to 1. If SAUmEN = 0, writing to a control register of serial array unit m is ignored, and, even if the register is read, only the default value is read (except for the input switch control register (ISC), noise filter enable register 0 (NFEN0), port input mode registers 0, 1, 3, 5, 8 (PIM0, PIM1, PIM3, PIM5, PIM8), port output mode registers 0, 1, 3, 5, 8 (POM0, POM1, POM3, POM5, POM8), port mode registers 0, 1, 3, 5, 8 (PM0, PM1, PM3, PM5, PM8), and port registers 0, 1, 3, 5, 8 (P0, P1, P3, P5, P8)).

- **Serial clock select register m (SPSm)**
- **Serial mode register mn (SMRmn)**
- **Serial communication operation setting register mn (SCRmn)**
- **Serial data register mn (SDRmn)**
- **Serial flag clear trigger register mn (SIRmn)**
- **Serial status register mn (SSRmn)**
- **Serial channel start register m (SSm)**
- **Serial channel stop register m (STm)**
- **Serial channel enable status register m (SEm)**
- **Serial output enable register m (SOEm)**
- **Serial output level register m (SOLm)**
- **Serial output register m (SOm)**
- **Serial standby control register m (SSCm)**

2. Be sure to clear bits 7 and 1 to “0”.

Remark m: Unit number (m = 0, 1), n:Channel number (n = 0 to 3)

Figure 18-41. Flowchart of Master Reception (in Continuous Reception Mode)



Remark <1> to <8> in the figure correspond to <1> to <8> in **Figure 18-40 Timing Chart of Master Reception (in Continuous Reception Mode)**.

(1) Register setting

Figure 18-58. Example of Contents of Registers for Slave Reception of 3-Wire Serial I/O (CSI00, CSI10, CSI30) (1/2)

(a) Serial mode register mn (SMRmn)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKSmn	CCSmn						STSmn		SISmn0				MDmn2	MDmn1	MDmn0
	0/1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Operation clock (f_{MCK}) of channel n
0: Prescaler output clock CKm0 set by the SPSm register
1: Prescaler output clock CKm1 set by the SPSm register

Interrupt source of channel n
0: Transfer end interrupt

(b) Serial communication operation setting register mn (SCRmn)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXEmn	RXEmn	DAPmn	CKPmn		EOCmn	PTCmn1	PTCmn0	DIRmn		SLCmn1	SLCmn0			DLSmn1	DLSmn0
	0	1	0/1	0/1	0	0	0	0	0/1	0	0	0	0	1	1	0/1

Selection of the data and clock phase (For details about the setting, see **18.3 Registers Controlling Serial Array Unit**.)

Selection of data transfer sequence
0: Inputs/outputs data with MSB first
1: Inputs/outputs data with LSB first.

Setting of data length
0: 7-bit data length
1: 8-bit data length

(c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDRmn	0000000 Baud rate setting							0	Receive data							

SIOp

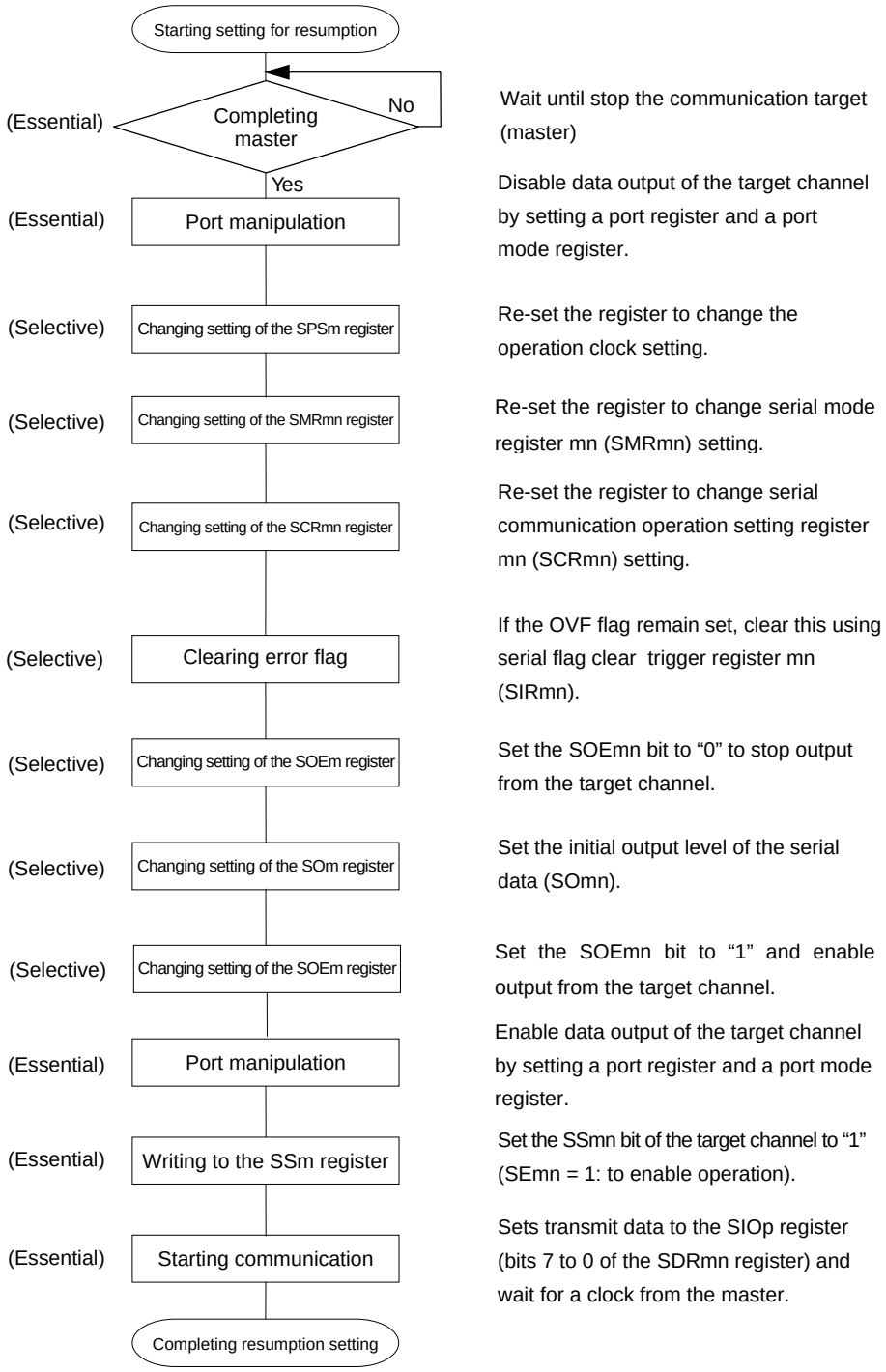
(d) Serial output register m (SOm) …The Register that not used in this mode.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<R> SOm						CKOm2		CKOm0						SOm2		SOm0
	0	0	0	0	1	×	1	×	0	0	0	0	1	×	1	×

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: CSI number (p = 00, 10, 30), mn = 00, 02, 12

2. ☐: Setting is fixed in the CSI slave transmission mode, ▒: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

Figure 18-67. Procedure for Resuming Slave Transmission/Reception



Cautions 1. Be sure to set transmit data to the SIOp register before the clock from the master is started.

2. If PER0 is rewritten while stopping the master transmission and the clock supply is stopped, wait until the transmission target (master) stops or transmission finishes, and then perform initialization instead of restarting the transmission.

(1) Register setting

Figure 18-108. Example of Contents of Registers for Data Transmission of Simplified I²C (IIC00, IIC10, IIC30) (1/2)

(a) Serial mode register mn (SMRmn) … Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKSmn	CCSmn						STSmn		SISmn0				MDmn2	MDmn1	MDmn0
	0/1	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

(b) Serial communication operation setting register mn (SCRmn) … Do not manipulate the bits of this register, except the TXEmn and RXEmn bits, during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXEmn	RXEmn	DAPmn	CKPmn		EOCmn	PTCmn1	PTCmn0	DIRmn		SLCmn1	SLCmn0			DLSmn1	DLSmn0
	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1 Note 1	1

(c) Serial data register mn (SDRmn) (lower 8 bits: SIOr) … During data transmission/reception, valid only lower 8-bits (SIOr)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDRmn	Baud rate setting Note 2							0	Transmit data setting							
									SIOr							

(d) Serial output register m (SOm) … Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOm						CKOm2		CKOm0						SOm2		SOm0
	0	0	0	0	1	0/1 Note3	1	0/1 Note3	0	0	0	0	1	0/1 Note3	1	0/1 Note3

(e) Serial output enable register m (SOEm) … Do not manipulate this register during data transmission/reception.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm														SOEm2		SOEm0
	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Notes 1. Only provided for the SCR00 register. This bit is fixed to 1 for the other registers.

2. Because the setting is completed by address field transmission, setting is not required.

3. The value varies depending on the communication data during communication operation.

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), r: IIC number (r = 00, 10, 30), mn = 00, 02, 12

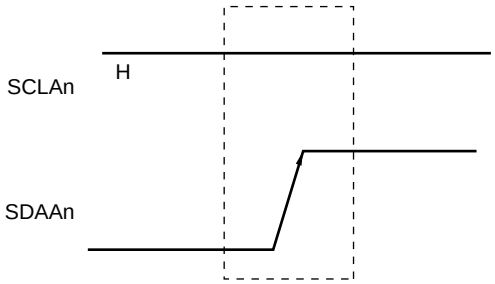
2. ☐: Setting is fixed in the IIC mode, ▒: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

19.5.5 Stop condition

When the SCLAn pin is at high level, changing the SDAAn pin from low level to high level generates a stop condition.

A stop condition is a signal that the master device generates to the slave device when serial transfer has been completed. When the device is used as a slave, stop conditions can be detected.

Figure 19-20. Stop Condition

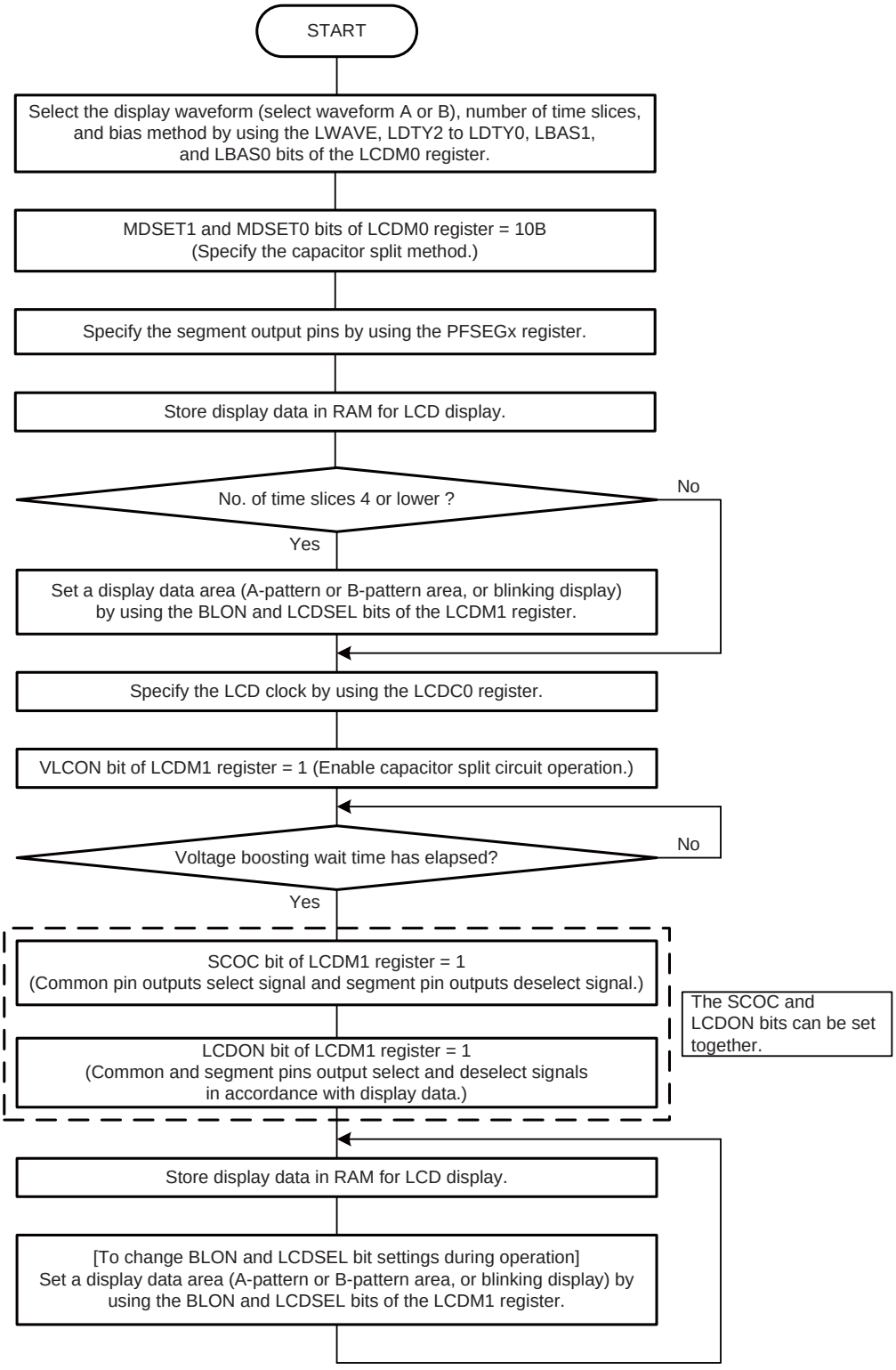


A stop condition is generated when bit 0 (SPTn) of IICA control register n0 (IICCTLn0) is set to 1. When the stop condition is detected, bit 0 (SPDn) of the IICA status register n (IICSn) is set to 1 and INTIICAn is generated when bit 4 (SPIEn) of the IICCTLn0 register is set to 1.

Remark n = 0

(3) Capacitor split method

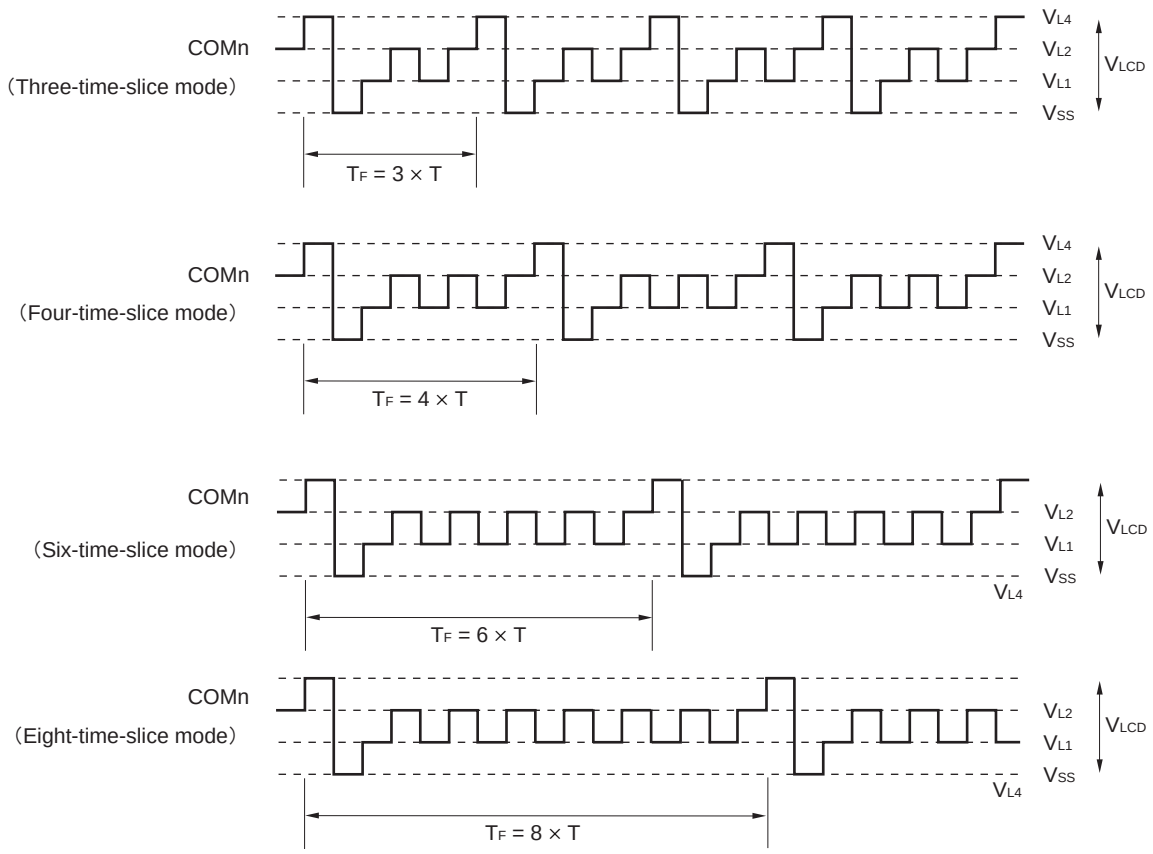
Figure 21-18. Capacitor Split Method Setting Procedure



Caution For the specifications of the voltage boosting wait time, see CHAPTER 41 ELECTRICAL SPECIFICATIONS.

Figure 21-23. Common Signal Waveforms (2/3)

(c) 1/3 bias method



T: One LCD clock period T_F: Frame frequency

< Example of calculation of LCD frame frequency (When four-time-slice mode is used) >

LCD clock: $32768/2^7$ = 256 Hz (When setting to LCDC0 = 06H)

LCD frame frequency: 64 Hz

CHAPTER 30 BATTERY BACKUP FUNCTION

30.1 Functions of Battery Backup

This function monitors the supply voltage at the V_{DD} pin, and switches the internal power supply and the power supply for ΔΣ A/D converter from the dedicated battery backup power pin (VBAT pin) when the voltage at the V_{DD} pin falls below the detection voltage. The mode used to supply the internal power and the power supply for ΔΣ A/D converter from the VBAT pin is referred to as battery backup mode. Even if power supply from the V_{DD} pin is cut off due to a power outage, operation of battery backup mode can be continued by switching to battery backup mode by hardware.

Table 30-1. Peripheral Circuit Operation State during Battery Backup (1/2)

Item			When operating CPU with the power of V_{DD} pin supplied	When operating CPU with the power of VBAT pin supplied
System clock			Clock supply operation to CPU	
	Main system clock		Operable	
	Subsystem clock		Operable when RTCPOR does not occur	
	f_{IL}		Operable	
CPU			Continuous operation	
Code flash memory			Continuous operation	Continuous operation[Note 1]
<R> Data flash memory			Operable	Operation disabled[Note 6]
RAM			Continuous operation	
Port	Internal V_{DD} port	P20 to P25, P150 to P152[Note 5]	Operable	
		P137, P121, P122	Operable	
	EV_{DD} port	Other than P20 to P25, P137, P121 to P124, P150 to P152	Operable	Operable when the power of EV_{DD} pin is supplied[Note 2] Not operable when the power of EV_{DD} pin is shut down[Note 3]
	VRTC port	P123, P124	Operable when RTCPOR does not occur	
Timer array unit			Operable	
Independent power supply RTC			Operable when RTCPOR does not occur	
Frequency measurement circuit			Operable	
Battery backup function			Continuous operation	
12-bit interval timer			Operable	
8-bit interval timer				
Watchdog timer				
Clock output/buzzer output				
10-bit A/D converter				
24-bit ΔΣ A/D converter			Operable	Operable[Note 4]
Temperature sensor			Operable	
Serial array unit				
IrDA				
Serial interface (IICA)				

(**Notes** are listed on the next page.)

Figure 35-2. Format of User Option Byte (000C1H/010C1H) (1/2)

Address: 000C1H/010C1H[Note]

7	6	5	4	3	2	1	0
VPOC2	VPOC1	VPOC0	1	LVIS1	LVIS0	LVIMDS1	LVIMDS0

- LVD setting (interrupt & reset mode)

Detection voltage			Option byte setting value						
V_{LVDH}		V_{LVDL}	VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge	Falling edge						LVIMDS1	LVIMDS0
1.98 V	1.94 V	1.84 V	0	0	1	1	0	1	0
2.09 V	2.04 V					0	1		
3.13 V	3.06 V					0	0		
2.61 V	2.55 V	2.45 V		1	0	1	0		
2.71 V	2.65 V					0	1		
3.75 V	3.67 V					0	0		
2.92 V	2.86 V	2.75 V		1	1	1	0		
3.02 V	2.96 V					0	1		
4.06 V	3.98 V					0	0		
–			Setting of values other than above is prohibited.						

- LVD setting (reset mode)

Detection voltage		Option byte setting value						
V_{LVD}		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge						LVIMDS1	LVIMDS0
1.77 V	1.73 V	0	0	0	1	0	1	1
1.88 V	1.84 V		0	1	1	1		
1.98 V	1.94 V		0	1	1	0		
2.09 V	2.04 V		0	1	0	1		
2.50 V	2.45 V		1	0	1	1		
2.61 V	2.55 V		1	0	1	0		
2.71 V	2.65 V		1	0	0	1		
2.81 V	2.75 V		1	1	1	1		
2.92 V	2.86 V		1	1	1	0		
3.02 V	2.96 V		1	1	0	1		
3.13 V	3.06 V		0	1	0	0		
3.75 V	3.67 V		1	0	0	0		
4.06 V	3.98 V		1	1	0	0		
–		Setting of values other than above is prohibited.						

Note Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

Caution Be sure to set bit 4 to "1".

Remarks 1. For LVD setting, see **29.1 Functions of Voltage Detector**.

2. The detection voltage is a typical value. For details, see **41.6.5 LVD circuit characteristics.**