Renesas Electronics America Inc - R5F10NLEDFB#50 Datasheet

What is "Embedded - Microcontrollers"?

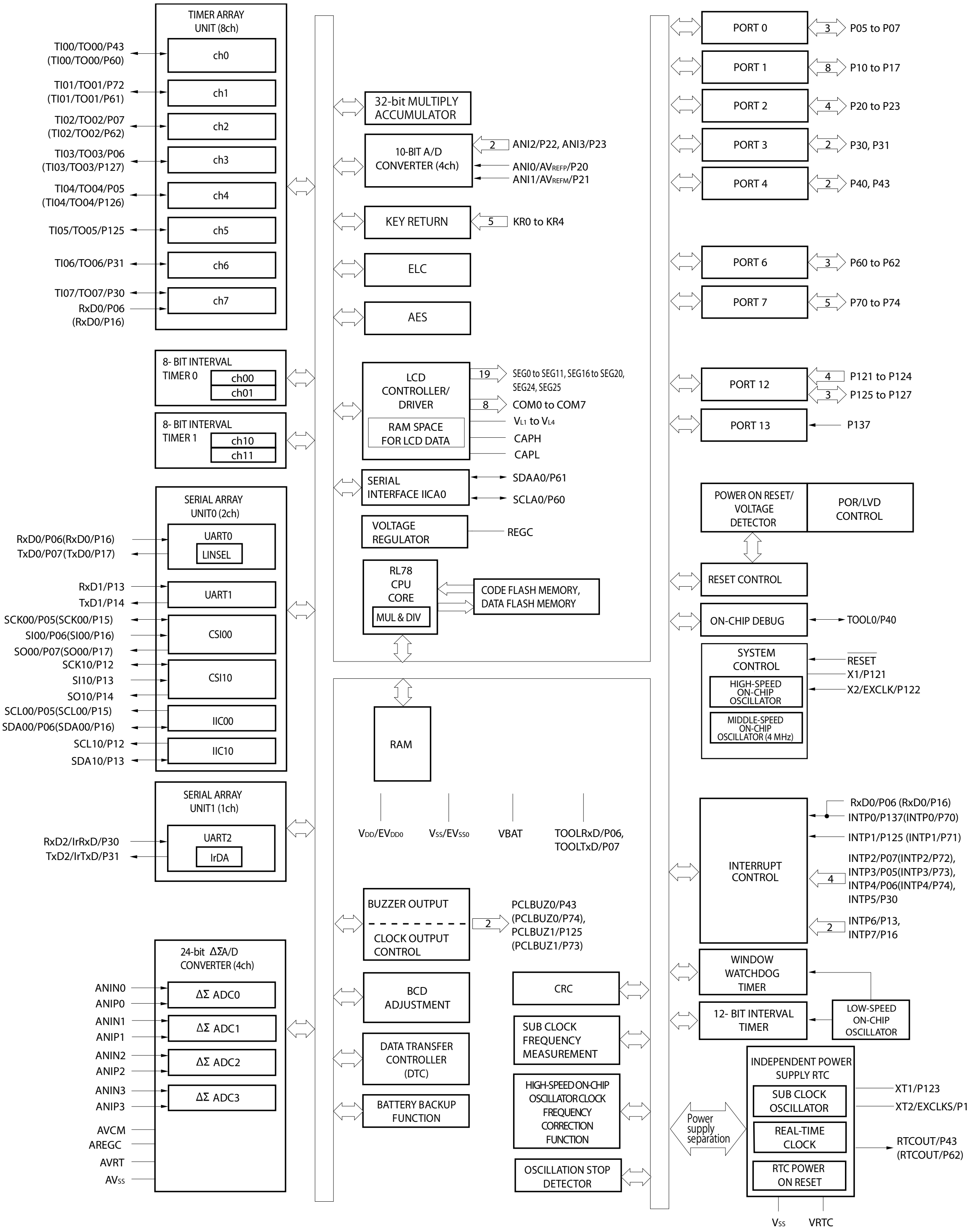
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, IrDA, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 5.5V
Data Converters	A/D 4x10b, 4x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10nledfb-50

1.5 Block Diagram

1.5.1 64-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR0). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR0)**.

2.3 Connection of Unused Pins

Table 2-3 shows the connections of unused pins.

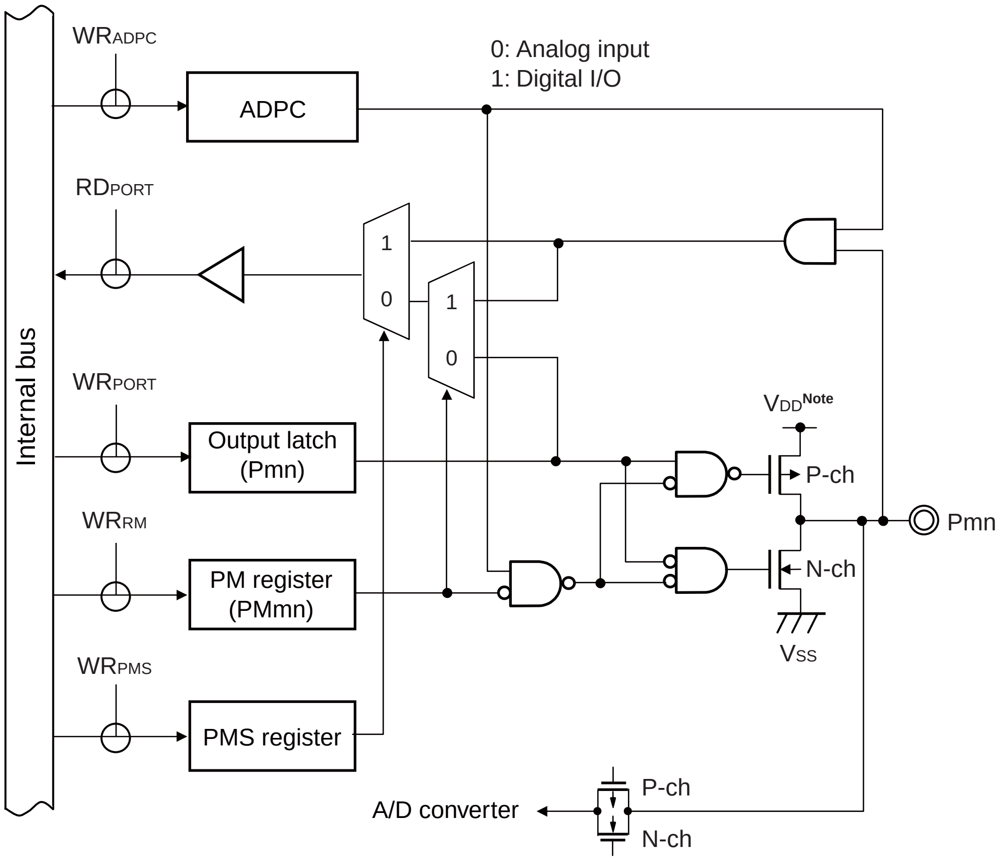
Remark The pins mounted depend on the product. See **1.3 Pin Configuration (Top View)** and **2.1 Port Function List.**

Table 2-3. Connection of Unused Pins (1/2)

Pin Name	I/O	Recommended Connection of Unused Pins
P02 to P07	I/O	Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P10 to P17		<When setting to port I/O> Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open. <When setting to segment output> Leave open.
P20 to P25		Input: Independently connect to V_{DD} or V_{SS} via a resistor. In addition, individually connect to V_{SS} via a resistor when using a battery backup function. Output: Leave open.
P30 to P37		<When setting to port I/O> Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open. <When setting to segment output> Leave open.
P40/TOOL0		Input: Independently connect to EV_{DD0} via a resistor or leave open. Output: Leave open.
P41 to P43		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P50 to P57		<When setting to port I/O> Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open. <When setting to segment output> Leave open.
P60 to P62		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Set the port's output latch to 0 and leave the pin open, or set the port's output latch to 1 and independently connect the pin to EV_{DD0} or EV_{SS0} via a resistor.

Remark For the products that do not have an EV_{DD0} or EV_{SS0} pin, replace EV_{DD0} with V_{DD}, and replace EV_{SS0} with V_{SS}.

Figure 2-4. Pin Block Diagram for Pin Type 4-3-3



Note Either V_{DD} or V_{BAT} selected by the battery backup function.

6.3.9 Peripheral enable registers 0, 1, 2 (PER0, PER1, PER2)

These registers are used to enable or disable supplying the clock to the peripheral hardware. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.
To use the peripheral functions below, which are controlled by these registers, set (1) the bit corresponding to each function before specifying the initial settings of the peripheral functions.

- Timer array unit
- Serial array unit 0
- Serial array unit 1
- Serial interface IICA0
- 10-bit A/D converter
- IrDA
- 24-bit ΔΣ A/D converter
- DTC
- Frequency measurement circuit
- Independent power supply real-time clock
- 32-bit multiplier and accumulator
- Oscillation stop detection circuit
- 12-bit interval timer

The PER0, PER1, and PER2 registers can be set by a 1-bit or an 8-bit memory manipulation instruction.
Reset signal generation clears these registers to 00H.

8.3.8 Timer channel stop register m (TTm)

The TTm register is a trigger register that is used to stop the counting operation of each channel.

When a bit of this register is set to 1, the corresponding bit of timer channel enable status register m (TEm) is cleared to 0. The TTmn, TTHm1, TTHm3 bits are immediately cleared when operation is stopped (TEmn, TTHm1, TTHm3 = 0), because they are trigger bits.

The TTm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TTm register can be set with a 1-bit or 8-bit memory manipulation instruction with TTmL.

Reset signal generation clears this register to 0000H.

Figure 8-19. Format of Timer Channel Stop register m (TTm)

Address: F01B4H, F01B5H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TTm	0	0	0	0	TTHm3	0	TTHm1	0	TTm7	TTm6	TTm5	TTm4	TTm3	TTm2	TTm1	TTm0

TTHm3	Trigger to stop operation of the higher 8-bit timer when channel 3 is in the 8-bit timer mode
0	No trigger operation
1	TEHm3 bit is cleared to 0 and the count operation is stopped.

TTHm1	Trigger to stop operation of the higher 8-bit timer when channel 1 is in the 8-bit timer mode
0	No trigger operation
1	TEHm1 bit is cleared to 0 and the count operation is stopped.

TTmn	Operation stop trigger of channel n
0	No trigger operation
1	TEmn bit clear to 0, to be count operation stop enable status. This bit is the trigger to stop operation of the lower 8-bit timer for TTm1 and TTm3 when channel 1 or 3 is in the 8-bit timer mode.

Caution Be sure to clear bits 15 to 12, 10, 8 of the TTm register to "0".

Remarks 1. When the TTm register is read, 0 is always read.

2. m: Unit number (m = 0),n: Channel number (n = 0 to 7)

CHAPTER 12 8-BIT INTERVAL TIMER

The 8-bit interval timer has two 8-bit timers (channel 0 and channel 1) which operate independently. These timers can be connected to operate as a 16-bit timer.
The 8-bit interval timer contains two units, 8-bit interval timer_0 and 8-bit interval timer_1, which have the same function. This chapter describes these units as the 8-bit interval timer unless there are differences among them.

12.1 Overview

The 8-bit interval timer is an 8-bit timer that operates using the f_{SX} or f_{IL} clock that is asynchronous with the CPU. Table 12 - 1 lists the 8-Bit Interval Timer Specifications and Figure 12 - 1 shows the 8-Bit Interval Timer Block Diagram.

Table 12 - 1 8-Bit Interval Timer Specifications

Item	Description
Count source (operating clock)	• f_{SX}, $f_{SX}/2$, $f_{SX}/4$, $f_{SX}/8$, $f_{SX}/16$, $f_{SX}/32$, $f_{SX}/64$, $f_{SX}/128$ • f_{IL}, $f_{IL}/2$, $f_{IL}/4$, $f_{IL}/8$, $f_{IL}/16$, $f_{IL}/32$, $f_{IL}/64$, $f_{IL}/128$
Operating mode	• 8-bit counter mode Channel 0 and channel 1 operate independently as an 8-bit counter • 16-bit counter mode Channel 0 and channel 1 are connected to operate as a 16-bit counter
Interrupt	• Output when the counter matches the compare value

17.3.2 Procedure for switching from normal operation mode to neutral missing mode

Figure 17-22 shows the procedure for switching from normal operation (with anti-tamper) (a total of three: current channel 0, voltage channel 1, and current channel 2 operate) to neutral missing mode (only current channel 0 operates), in single-phase two-wire mode.

In neutral missing mode, there are cases when only current channel 0 operates and only current channel 2 operates. Use the same procedure when switching the mode.

Figure 17-22. Procedure for Switching from Normal Operation Mode to Neutral Missing Mode

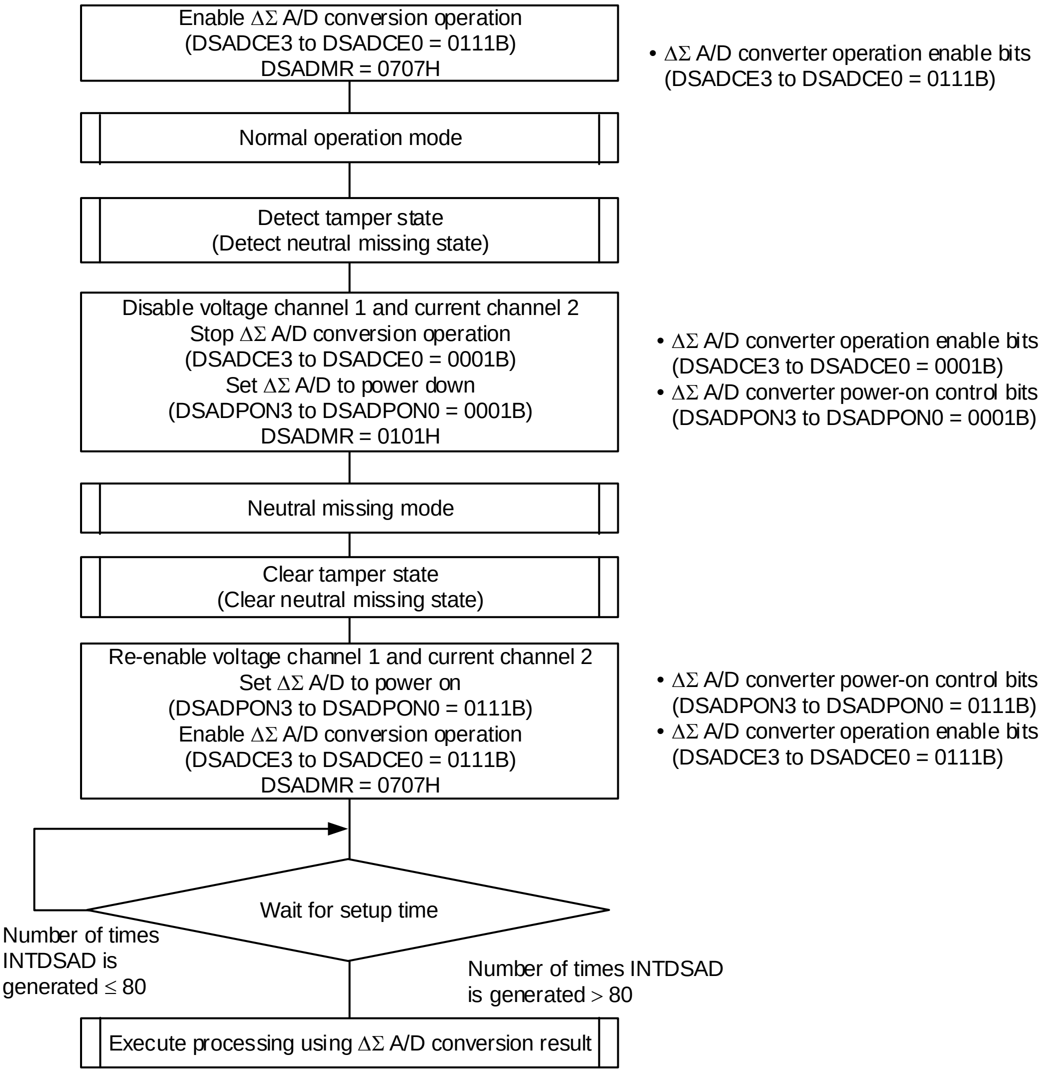
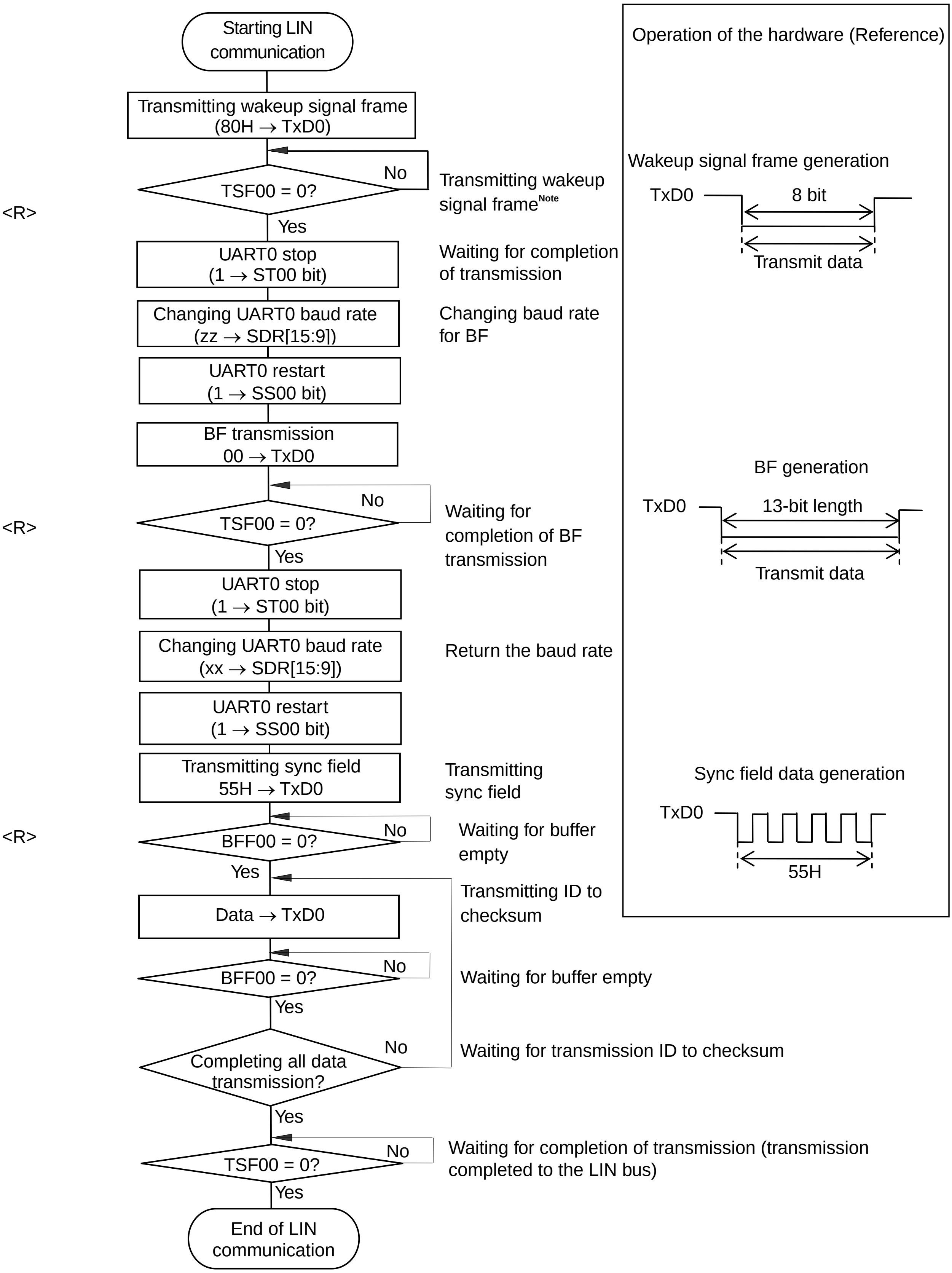

Enable ΔΣ A/D conversion operation
(DSADCE3 to DSADCE0 = 0111B)
DSADMR = 0707H
• ΔΣ A/D converter operation enable bits
(DSADCE3 to DSADCE0 = 0111B)
Normal operation mode
Detect tamper state
(Detect neutral missing state)
Disable voltage channel 1 and current channel 2
Stop ΔΣ A/D conversion operation
(DSADCE3 to DSADCE0 = 0001B)
Set ΔΣ A/D to power down
(DSADPON3 to DSADPON0 = 0001B)
DSADMR = 0101H
• ΔΣ A/D converter operation enable bits
(DSADCE3 to DSADCE0 = 0001B)
• ΔΣ A/D converter power-on control bits
(DSADPON3 to DSADPON0 = 0001B)
Neutral missing mode
Clear tamper state
(Clear neutral missing state)
Re-enable voltage channel 1 and current channel 2
Set ΔΣ A/D to power on
(DSADPON3 to DSADPON0 = 0111B)
Enable ΔΣ A/D conversion operation
(DSADCE3 to DSADCE0 = 0111B)
DSADMR = 0707H
• ΔΣ A/D converter power-on control bits
(DSADPON3 to DSADPON0 = 0111B)
• ΔΣ A/D converter operation enable bits
(DSADCE3 to DSADCE0 = 0111B)
Wait for setup time
Number of times
INTDSAD is
generated ≤ 80
Number of times INTDSAD
is generated > 80
Execute processing using ΔΣ A/D conversion result

Figure 18-100. Flowchart for LIN Transmission


Starting LIN communication
Transmitting wakeup signal frame (80H → TxD0)
TSF00 = 0?
No
Yes
<R>
Transmitting wakeup signal frame[Note]
UART0 stop (1 → ST00 bit)
Waiting for completion of transmission
Changing UART0 baud rate (zz → SDR[15:9])
Changing baud rate for BF
UART0 restart (1 → SS00 bit)
BF transmission 00 → TxD0
TSF00 = 0?
No
Yes
<R>
Waiting for completion of BF transmission
UART0 stop (1 → ST00 bit)
Changing UART0 baud rate (xx → SDR[15:9])
Return the baud rate
UART0 restart (1 → SS00 bit)
Transmitting sync field 55H → TxD0
Transmitting sync field
BFF00 = 0?
No
Yes
<R>
Waiting for buffer empty
Data → TxD0
Transmitting ID to checksum
BFF00 = 0?
No
Yes
Waiting for buffer empty
Completing all data transmission?
No
Yes
Waiting for transmission ID to checksum
TSF00 = 0?
No
Yes
Waiting for completion of transmission (transmission completed to the LIN bus)
End of LIN communication
Operation of the hardware (Reference)
Wakeup signal frame generation
TxD0
8 bit
Transmit data
BF generation
TxD0
13-bit length
Transmit data
Sync field data generation
TxD0
55H

Note When LIN-bus start from sleep status only

Remark Default setting of the UART is complete, and the flow from the transmission enable status.

19.3.6 IICA control register n1 (IICCTLn1)

This register is used to set the operation mode of I^{2}C and detect the statuses of the SCLAn and SDAAn pins.

The IICCTLn1 register can be set by a 1-bit or 8-bit memory manipulation instruction. However, the CLDn and DADn bits are read-only.

Set the IICCTLn1 register, except the WUPn bit, while operation of I^{2}C is disabled (bit 7 (IICEn) of IICA control register n0 (IICCTLn0) is 0).

Reset signal generation clears this register to 00H.

Figure 19-10. Format of IICA Control Register n1 (IICCTLn1) (1/2)

Address: F0231H After reset: 00H R/W[Note 1]

Symbol	<7>	6	<5>	<4>	<3>	<2>	1	<0>
IICCTLn1	WUPn	0	CLDn	DADn	SMCn	DFCn	0	PRSn

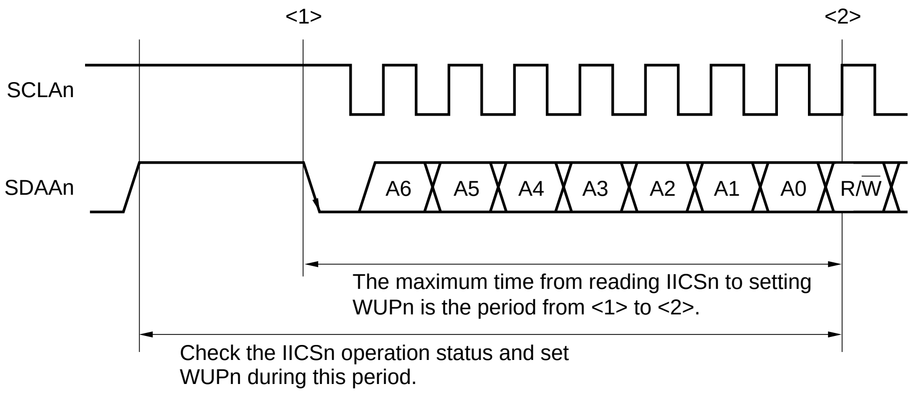
WUPn	Control of address match wakeup
0	Stops operation of address match wakeup function in STOP mode.
1	Enables operation of address match wakeup function in STOP mode.

To shift to STOP mode when WUPn = 1, execute the STOP instruction at least three clocks of f_{MCK} after setting (1) the WUPn bit (see **Figure 19-23 Flow When Setting WUPn = 1**).
Clear (0) the WUPn bit after the address has matched or an extension code has been received. The subsequent communication can be entered by the clearing (0) WUPn bit. (The wait must be released and transmit data must be written after the WUPn bit has been cleared (0).)
The interrupt timing when the address has matched or when an extension code has been received, while WUPn = 1, is identical to the interrupt timing when WUPn = 0. (A delay of the difference of sampling by the clock will occur.) Furthermore, when WUPn = 1, a stop condition interrupt is not generated even if the SPIEn bit is set to 1.

Condition for clearing (WUPn = 0)	Condition for setting (WUPn = 1)
• Cleared by instruction (after address match or extension code reception)	• Set by instruction (when the MSTSn, EXCn, and COIn bits are “0”, and the STDn bit also “0” (communication not entered))[Note 2]

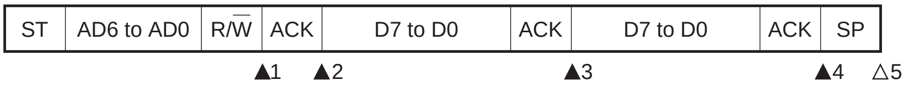
Notes 1. Bits 4 and 5 are read-only.

2. The status of the IICA status register n (IICSn) must be checked and the WUPn bit must be set during the period shown below.


<1>
<2>
SCLAn
SDAAn
A6
A5
A4
A3
A2
A1
A0
R/$\overline{W}$
The maximum time from reading IICSn to setting WUPn is the period from <1> to <2>.
Check the IICSn operation status and set WUPn during this period.

Remark n = 0

(ii) When WTIMn = 1



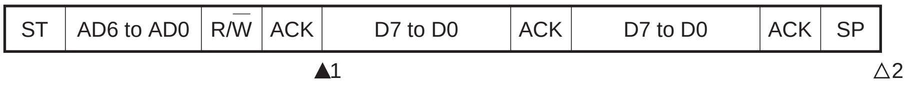
▲1: IICSn = 0110×010B
▲2: IICSn = 0010×110B
▲3: IICSn = 0010×100B
▲4: IICSn = 0010××00B
△5: IICSn = 00000001B

Remark ▲: Always generated
△: Generated only when SPIEn = 1
×: Don’t care

(6) Operation when arbitration loss occurs (no communication after arbitration loss)

When the device is used as a master in a multi-master system, read the MSTSn bit each time interrupt request signal INTIICAn has occurred to check the arbitration result.

(a) When arbitration loss occurs during transmission of slave address data (when WTIMn = 1)



▲1: IICSn = 01000110B
△2: IICSn = 00000001B

Remark ▲: Always generated
△: Generated only when SPIEn = 1

Remark n = 0

20.3.3 Reception

In reception, the IR frame data is converted to the UART frame data through the IrDA and is input to the SAU.

Low-level data is output when the IRRXINV bit is 0 and a high-level pulse is detected, and high-level data is output when no pulse is detected for 1-bit period. Note that a pulse shorter than 1.41 μs, which is the minimum pulse width, is identified as a low signal.

20.3.4 Selecting high-level pulse width

When the pulse width should be shorter than the bit rate × 3/16 for transmission, applicable IRCKS2 to IRCKS0 bit settings (minimum pulse width) and the corresponding high-level pulse widths shown in Table 20-4 can be used.

Table 20-4. IRCKS2 to IRCKS0 Bit Settings

f_{CLK} [MHz]	Item	<Upper Row> Bit Rate [kbps] <Lower Row> Bit Rate × 3/16 [μs]					
		2.4	9.6	19.2	38.4	57.6	115.2
		78.13	19.53	9.77	4.87	3.26	1.63
1	IRCKS2 to IRCKS0	001	001	001	–[Note 1]	–[Note 1]	–[Note 1]
	High-level pulse width [μs]	2.00	2.00	2.00	–[Note 1]	–[Note 1]	–[Note 1]
2	IRCKS2 to IRCKS0	010	010	010	010	010	–[Note 1]
	High-level pulse width [μs]	2.00	2.00	2.00	2.00	2.00	–[Note 1]
3	IRCKS2 to IRCKS0	011	011	011	011	011	–[Note 1]
	High-level pulse width [μs]	2.67	2.67	2.67	2.67	2.67	–[Note 1]
4	IRCKS2 to IRCKS0	011	011	011	011	011	000[Note 2]
	High-level pulse width [μs]	2.00	2.00	2.00	2.00	2.00	1.50
6	IRCKS2 to IRCKS0	100	100	100	100	100	000[Note 2]
	High-level pulse width [μs]	2.67	2.67	2.67	2.67	2.67	1.50
8	IRCKS2 to IRCKS0	100	100	100	100	100	000[Note 2]
	High-level pulse width [μs]	2.00	2.00	2.00	2.00	2.00	1.50
12	IRCKS2 to IRCKS0	101	101	101	101	101	000[Note 2]
	High-level pulse width [μs]	2.67	2.67	2.67	2.67	2.67	1.50
16	IRCKS2 to IRCKS0	101	101	101	101	101	000[Note 2]
	High-level pulse width [μs]	2.00	2.00	2.00	2.00	2.00	1.50
24	IRCKS2 to IRCKS0	110	110	110	110	110	000[Note 2]
	High-level pulse width [μs]	2.67	2.67	2.67	2.67	2.67	1.50
32	IRCKS2 to IRCKS0	110	110	110	110	110	000[Note 2]
	High-level pulse width [μs]	2.00	2.00	2.00	2.00	2.00	1.50

Notes 1. "–" indicates that the communication specification cannot be satisfied.

2. The pulse width cannot be shorter than the bit rate × 3/16.

Figure 21-2. Format of LCD Mode Register 0 (LCDM0) (2/2)

Address: FFF40H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
LCDM0	MDSET1	MDSET0	LWAVE	LDTY2	LDTY1	LDTY0	LBAS1	LBAS0

LBAS1	LBAS0	LCD display bias mode selection
0	0	1/2 bias method
0	1	1/3 bias method
1	0	1/4 bias method
1	1	Setting prohibited

Cautions 1. Do not rewrite the LCDM0 value while the SCOC bit of the LCDM1 register = 1.

2. When “Static” is selected (LDTY2 to LDTY0 bits = 000B), be sure to set the LBAS1 and LBAS0 bits to the default value (00B). Otherwise, the operation will not be guaranteed.

3. Only the combinations of display waveform, number of time slices, and bias method shown in Table 21-4 are supported.
Combinations of settings not shown in Table 21-4 are prohibited.

Table 21-4. Combinations of Display Waveform, Time Slices, Bias Method, and Frame Frequency

Display Mode			Set Value						Driving Voltage Generation Method		
Display Waveform	Number of Time Slices	Bias Mode	LWAVE	LDTY2	LDTY1	LDTY0	LBAS1	LBAS0	External Resistance Division	Internal Voltage Boosting	Capacitor Split
Waveform A	8	1/4	0	1	0	1	1	0	○ (24 to 128 Hz)	○ (24 to 64 Hz)	×
Waveform A	6	1/4	0	1	0	0	1	0	×	○ (32 to 86 Hz)	×
Waveform A	8	1/3	0	1	0	1	0	1	○ (32 to 128 Hz)	○ (32 to 64 Hz)	○ (32 to 128 Hz)
Waveform A	6	1/3	0	1	0	0	0	1	○ (32 to 128 Hz)	○ (32 to 86 Hz)	○ (32 to 128 Hz)
Waveform A	4	1/3	0	0	1	1	0	1	○ (24 to 128 Hz)	○ (24 to 128 Hz)	○ (24 to 128 Hz)
Waveform A	3	1/3	0	0	1	0	0	1	○ (32 to 128 Hz)	○ (32 to 128 Hz)	○ (32 to 128 Hz)
Waveform A	3	1/2	0	0	1	0	0	0	○ (32 to 128 Hz)	×	×
Waveform A	2	1/2	0	0	0	1	0	0	○ (24 to 128 Hz)	×	×
Waveform A	Static		0	0	0	0	0	0	○ (24 to 128 Hz)	×	×
Waveform B	8	1/4	1	1	0	1	1	0	○ (24 to 128 Hz)	○ (24 to 64 Hz)	×
Waveform B	8	1/3	1	1	0	1	0	1	○ (32 to 128 Hz)	○ (32 to 64 Hz)	○ (32 to 128 Hz)
Waveform B	6	1/3	1	1	0	0	0	1	○ (32 to 128 Hz)	○ (32 to 86 Hz)	○ (32 to 128 Hz)
Waveform B	4	1/3	1	0	1	1	0	1	○ (24 to 128 Hz)	○ (24 to 128 Hz)	○ (24 to 128 Hz)
Waveform B	3	1/3	1	0	1	0	0	1	○ (32 to 128 Hz)	○ (32 to 128 Hz)	○ (32 to 128 Hz)

Remark ○: Supported
×: Not supported

24.3.4 External interrupt rising edge enable register (EGP0, EGP1), External interrupt falling edge enable register (EGN0, EGN1)

These registers specify the valid edge for INTP0 to INTP7 and RTCIC0 to RTCIC2.

The EGP0, EGP1, EGN0 and EGN1 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 24-5. Format of External Interrupt Rising Edge Enable Register (EGP0, EGP1) and External Interrupt Falling Edge Enable Register (EGN0, EGN1)

Address: FFF38H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP0	EGP7	EGP6	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0

Address: FFF39H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN0	EGN7	EGN6	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0

Address: FFF3AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP1	0	EGP14	EGP13	EGP12	0	0	0	0

Address: FFF3BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN1	0	EGN14	EGN13	EGN12	0	0	0	0

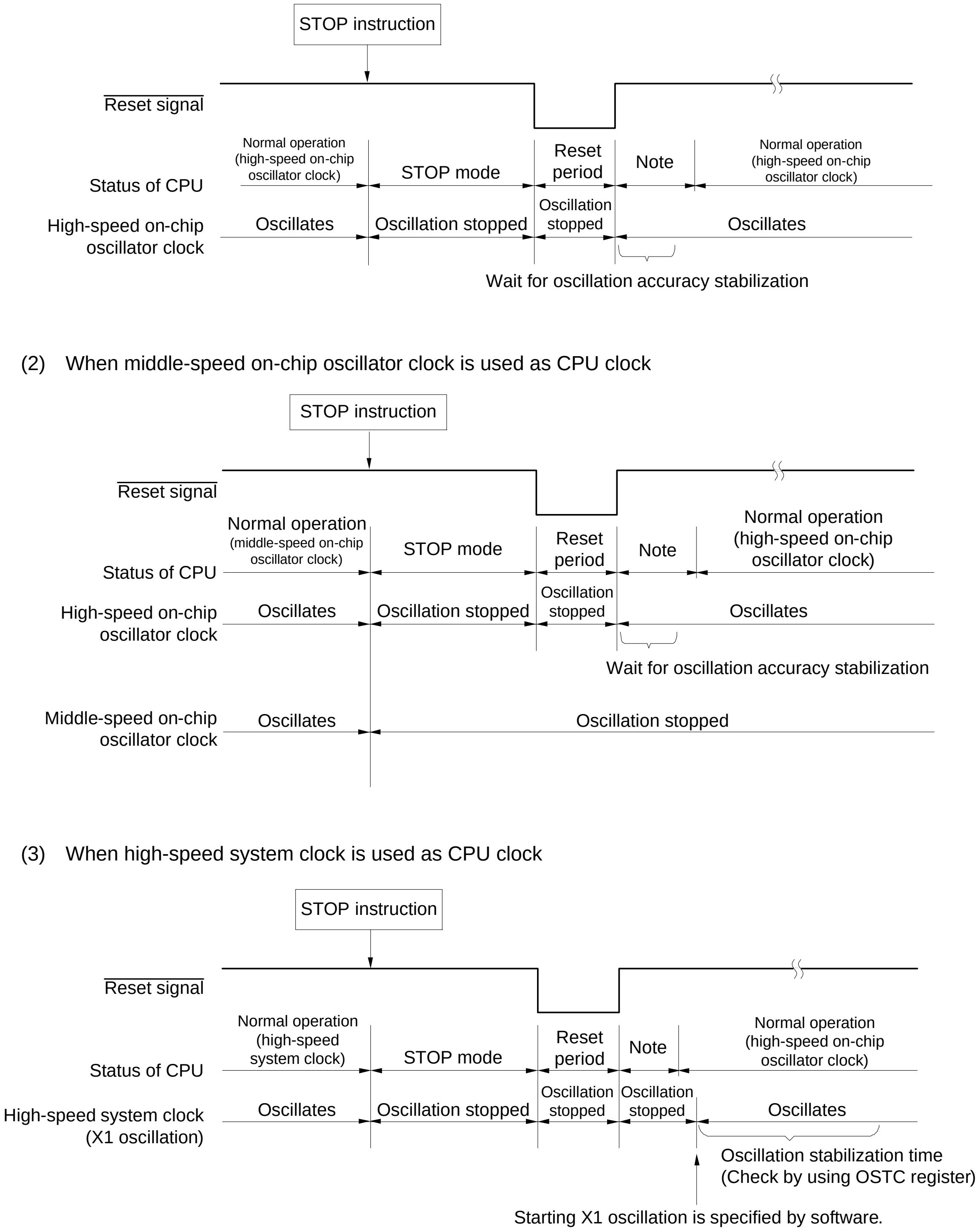
<R>

EGPn	EGNn	INTP0 to INTP7 and RTCIC0 to RTCIC2 pin valid edge selection (n = 0 to 7, 12 to 14)
0	0	Edge detection disabled
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

(b) Release by reset signal generation

When the reset signal is generated, STOP mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

Figure 26 - 4 STOP Mode Release by Reset



(1) When high-speed on-chip oscillator clock is used as CPU clock

STOP instruction
Reset signal
Status of CPU
Normal operation (high-speed on-chip oscillator clock)
STOP mode
Reset period
Note
Normal operation (high-speed on-chip oscillator clock)
High-speed on-chip oscillator clock
Oscillates
Oscillation stopped
Oscillation stopped
Oscillates
Wait for oscillation accuracy stabilization

(2) When middle-speed on-chip oscillator clock is used as CPU clock

STOP instruction
Reset signal
Status of CPU
Normal operation (middle-speed on-chip oscillator clock)
STOP mode
Reset period
Note
Normal operation (high-speed on-chip oscillator clock)
High-speed on-chip oscillator clock
Oscillates
Oscillation stopped
Oscillation stopped
Oscillates
Wait for oscillation accuracy stabilization
Middle-speed on-chip oscillator clock
Oscillates
Oscillation stopped

(3) When high-speed system clock is used as CPU clock

STOP instruction
Reset signal
Status of CPU
Normal operation (high-speed system clock)
STOP mode
Reset period
Note
Normal operation (high-speed on-chip oscillator clock)
High-speed system clock (X1 oscillation)
Oscillates
Oscillation stopped
Oscillation stopped
Oscillation stopped
Oscillates
Oscillation stabilization time (Check by using OSTC register)
Starting X1 oscillation is specified by software.

Note For the reset processing time, see **CHAPTER 27 RESET FUNCTION**.
For the reset processing time of the power-on-reset circuit (POR) and voltage detector (LVD), see **CHAPTER 28 POWER-ON-RESET CIRCUIT**.

Table 30-1. Peripheral Circuit Operation State during Battery Backup (2/2)

Item		When operating CPU with the power of V_{DD} pin supplied	When operating CPU with the power of VBAT pin supplied
LCD controller/driver		Operable	
Data transfer controller (DTC)			
Event link controller (ELC)			
Power-on-reset function		Continuous operation	
RTC power-on-reset function		Continuous operation	
Voltage detection function	Internal power supply voltage (Internal V_{DD})	Operable	
	V_{DD}, VBAT, VRTC, EXLVD Pin voltage	Operable	
External interrupt	INTP0	Operable	
	INTP1 to INTP7	Operable	Operable when the power of EV_{DD} pin is supplied[Note 2]. Not operable when the power of EV_{DD} pin is shut down.
	RTCIC0 to RTCIC2	Operable	
Key interrupt input		Operable	
CRC operation function			
32-bit multiplier and multiplyaccumulator			
RAM parity error detection function			
RAM guard function			
SFR guard function			
Illegal-memory access detection function			
AES function			

Notes 1. The self-programming function cannot be used.

2. When supplying the power from outside to the EV_{DD} pin, it is recommended to backup the V_{DD} and VBAT pins or the VRTC pin with the diode ORing.

3. When the power of EV_{DD} is not supplied, set GDIDIS0 to 1.

4. The ΔΣ A/D converter operable in the backup mode is limited up to 3 channels.

5. RTCIC0, RTCIC1, and RTCIC2 pins are included.

<R> **6.** When power supply switching by the battery backup function occurs, access to the data flash memory is prohibited.

- The power is supplied from the V_{DD} pin at startup of the power supply. MCU remains reset even when the power is supplied to the VBAT pin earlier than the V_{DD} pin.
- The battery backup function is stopped by default. The battery backup mode must be set by the software after startup of the power supply.
- If the V_{DD} pin voltage is lower than the detection voltage, the internal power and the power supply for ΔΣ A/D converter can be switched from the V_{DD} supply to the VBAT supply. When the V_{DD} pin voltage is recovered higher than the detection voltage, the internal power and the power supply for ΔΣ A/D converter can be switched from the VBAT supply to the V_{DD} supply.
- Under the condition of $\text{VBAT} \geq V_{DD}$, the software enables to switch the internal power and the power supply for ΔΣ A/D converter from the VBAT supply to the V_{DD} supply.

<R>

Table 39-4. Relationship between Operation Mode and Register Name

Operation Mode	Multiplication Result Register Name			
	Bits 63 to 48	Bits 47 to 32	Bits 31 to 16	Bits 15 to 0
Multiplication mode (unsigned)	MULR3	MULR2	MULR1	MULR0
Multiplication mode (signed)				
Multiply-accumulation mode (unsigned)				
Multiply-accumulation mode (signed)				

The operation result (multiplication) is stored for the multiplication, and the operation result (accumulation) is stored for the multiply-accumulation. Additionally, the accumulation initial value can be set for the multiply-accumulation.

Table 39-5. Details of Storing of Operation Modes and Multiplication Result Registers

Operation Mode	Setting	Operation Result
Multiplication mode (unsigned)	–	MULR3 to MULR0: Multiplication (unsigned)
Multiplication mode (signed)	–	MULR3 to MULR0: Multiplication (signed)
Multiply-accumulation mode (unsigned)	MULR3 to MULR0: Accumulation initial value (unsigned)	MULR3 to MULR0: Accumulation value (unsigned)
Multiply-accumulation mode (signed)	MULR3 to MULR0: Accumulation initial value (signed)	MULR3 to MULR0: Accumulation value (signed)

If exceeding the maximum value of the value range that can be handled in 64 bit (= overflow), or if dropping below the minimum value (= underflow), the value is reversed, and the values plus overflow/underflow values are stored in the MULR3 to MULR0 registers.

■ Unsigned

- In case of overflow

  Processing) 2^{64} + MULR[63:0]

  Example)

  FFFF FFFF FFFF FFFFh + 0000 0000 0000 0001h = 0000 0000 0000 0000h

■ Signed

- In case of overflow

  Processing) 2^{63} + MULR[62:0]

  Example)

  7FFF FFFF FFFF FFFFh + 0000 0000 0000 0001h = 8000 0000 0000 0000h

- In case of underflow

  Processing) -2^{63} + MULR[62:0]

  Example)

  8000 0000 0000 0000h + FFFF FFFF FFFF FFFFh = 7FFF FFFF FFFF FFFFh

Table 40-5. Operation List (7/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	**Note 2**		Z	AC	CY
8-bit operation	ADDC	A, #byte	2	1	–	A, CY ← A+byte+CY	×	×	×
		saddr, #byte	3	2	–	(saddr), CY ← (saddr) +byte+CY	×	×	×
		A, rv [Note 3]	2	1	–	A, CY ← A + r + CY	×	×	×
		r, A	2	1	–	r, CY ← r + A + CY	×	×	×
		A, !addr16	3	1	4	A, CY ← A + (addr16)+CY	×	×	×
		A, ES:!addr16	4	2	5	A, CY ← A + (ES, addr16)+CY	×	×	×
		A, saddr	2	1	–	A, CY ← A + (saddr)+CY	×	×	×
		A, [HL]	1	1	4	A, CY ← A+ (HL) + CY	×	×	×
		A, ES:[HL]	2	2	5	A,CY ← A+ (ES, HL) + CY	×	×	×
		A, [HL+byte]	2	1	4	A, CY ← A+ (HL+byte) + CY	×	×	×
		A, ES:[HL+byte]	3	2	5	A,CY ← A+ ((ES, HL)+byte) + CY	×	×	×
		A, [HL+B]	2	1	4	A, CY ← A+ (HL+B) +CY	×	×	×
		A, ES:[HL+B]	3	2	5	A,CY ← A+((ES, HL)+B)+CY	×	×	×
		A, [HL+C]	2	1	4	A, CY ← A+ (HL+C)+CY	×	×	×
		A, ES:[HL+C]	3	2	5	A,CY ← A+ ((ES, HL)+C)+CY	×	×	×
	SUB	A, #byte	2	1	–	A, CY ← A – byte	×	×	×
		saddr, #byte	3	2	–	(saddr), CY ← (saddr) – byte	×	×	×
		A, r [Note 3]	2	1	–	A, CY ← A – r	×	×	×
		r, A	2	1	–	r, CY ← r – A	×	×	×
		A, !addr16	3	1	4	A, CY ← A – (addr16)	×	×	×
		A, ES:!addr16	4	2	5	A, CY ← A – (ES, addr16)	×	×	×
		A, saddr	2	1	–	A, CY ← A – (saddr)	×	×	×
		A, [HL]	1	1	4	A, CY ← A – (HL)	×	×	×
		A, ES:[HL]	2	2	5	A,CY ← A – (ES, HL)	×	×	×
		A, [HL+byte]	2	1	4	A, CY ← A – (HL+byte)	×	×	×
		A, ES:[HL+byte]	3	2	5	A,CY ← A – ((ES, HL)+byte)	×	×	×
		A, [HL+B]	2	1	4	A, CY ← A – (HL+B)	×	×	×
		A, ES:[HL+B]	3	2	5	A,CY ← A – ((ES, HL)+B)	×	×	×
		A, [HL+C]	2	1	4	A, CY ← A – (HL+C)	×	×	×
		A, ES:[HL+C]	3	2	5	A,CY ← A – ((ES, HL)+C)	×	×	×

Notes 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

2. Number of CPU clocks (f_{CLK}) when the code flash area is accessed.

3. Except r = A

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

Table 40-5. Operation List (9/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	**Note 2**		Z	AC	CY
8-bit operation	OR	A, #byte	2	1	–	A ← A∨byte	×		
		saddr, #byte	3	2	–	(saddr) ← (saddr)∨byte	×		
		A, r Note 3	2	1	–	A ← A∨r	×		
		r, A	2	1	–	r ← r∨A	×		
		A, !addr16	3	1	4	A ← A∨(addr16)	×		
		A, ES:!addr16	4	2	5	A ← A∨(ES:addr16)	×		
		A, saddr	2	1	–	A ← A∨(saddr)	×		
		A, [HL]	1	1	4	A ← A∨(H)	×		
		A, ES:[HL]	2	2	5	A ← A∨(ES:HL)	×		
		A, [HL+byte]	2	1	4	A ← A∨(HL+byte)	×		
		A, ES:[HL+byte]	3	2	5	A ← A∨((ES:HL)+byte)	×		
		A, [HL+B]	2	1	4	A ← A∨(HL+B)	×		
		A, ES:[HL+B]	3	2	5	A ← A∨((ES:HL)+B)	×		
		A, [HL+C]	2	1	4	A ← A∨(HL+C)	×		
		A, ES:[HL+C]	3	2	5	A ← A∨((ES:HL)+C)	×		
	XOR	A, #byte	2	1	–	A ← A⊻byte	×		
		saddr, #byte	3	2	–	(saddr) ← (saddr)⊻byte	×		
		A, r Note 3	2	1	–	A ← A⊻r	×		
		r, A	2	1	–	r ← r⊻A	×		
		A, !addr16	3	1	4	A ← A⊻(addr16)	×		
		A, ES:!addr16	4	2	5	A ← A⊻(ES:addr16)	×		
		A, saddr	2	1	–	A ← A⊻(saddr)	×		
		A, [HL]	1	1	4	A ← A⊻(HL)	×		
		A, ES:[HL]	2	2	5	A ← A⊻(ES:HL)	×		
		A, [HL+byte]	2	1	4	A ← A⊻(HL+byte)	×		
		A, ES:[HL+byte]	3	2	5	A ← A⊻((ES:HL)+byte)	×		
		A, [HL+B]	2	1	4	A ← A⊻(HL+B)	×		
		A, ES:[HL+B]	3	2	5	A ← A⊻((ES:HL)+B)	×		
		A, [HL+C]	2	1	4	A ← A⊻(HL+C)	×		
		A, ES:[HL+C]	3	2	5	A ← A⊻((ES:HL)+C)	×		

Notes 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

2. Number of CPU clocks (f_{CLK}) when the code flash area is accessed.

3. Except r = A

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

(5) Communication at different potential (1.9 V, 2.5 V, 3 V) (UART mode) (1/2)

(T_A = –40 to +85°C, 1.9 V ≤ EV_{DD0} = EV_{DD1} ≤ $V_{DD}^{\text{Note 1}}$ ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LP (low-power main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Reception	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		$f_{MCK}/6^{\text{Note 1}}$		$f_{MCK}/6^{\text{Note 1}}$		$f_{MCK}/6^{\text{Note 1}}$		$f_{MCK}/6^{\text{Note 1}}$	bps
			Theoretical value of the maximum transfer rate f_{MCK} = $f_{CLK}^{\text{Note 4}}$		5.3		1.3		0.1		0.6	Mbps
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		$f_{MCK}/6^{\text{Note 1}}$		$f_{MCK}/6^{\text{Note 1}}$		$f_{MCK}/6^{\text{Note 1}}$		$f_{MCK}/6^{\text{Note 1}}$	bps
			Theoretical value of the maximum transfer rate f_{MCK} = $f_{CLK}^{\text{Note 4}}$		5.3		1.3		0.1		0.6	Mbps
			1.9 V ≤ EV_{DD} < 3.3 V, 1.8 V ≤ V_b ≤ 2.0 V		$f_{MCK}/6$ Notes 1 to 3		$f_{MCK}/6$ Notes 1, 2		$f_{MCK}/6$ Notes 1, 2		$f_{MCK}/6$ Notes 1, 2	bps
			Theoretical value of the maximum transfer rate f_{MCK} = $f_{CLK}^{\text{Note 4}}$		5.3		1.3		0.1		0.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. Use it with EV_{DD} ≥ V_b.

3. The following conditions are required for low voltage interface.

2.4 V ≤ EV_{DD} < 2.7 V: MAX. 2.6 Mbps

1.9 V ≤ EV_{DD} < 2.4 V: MAX. 1.3 Mbps

4. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

HS (high-speed main) mode:	32 MHz (2.8 V ≤ EV_{DD} ≤ 5.5 V), 24 MHz (2.7 V ≤ EV_{DD} ≤ 5.5 V), 16 MHz (2.5 V ≤ EV_{DD} ≤ 5.5 V), 12 MHz (2.4 V ≤ EV_{DD} ≤ 5.5 V), 6 MHz (2.1 V ≤ EV_{DD} ≤ 5.5 V),
LS (low-speed main) mode:	8 MHz (1.9 V ≤ EV_{DD} ≤ 5.5 V), 4 MHz (1.9 V ≤ EV_{DD} ≤ 5.5 V)
LP (low-power main) mode:	1 MHz (1.9 V ≤ EV_{DD} ≤ 5.5 V)
LV (low-voltage main) mode:	4 MHz (1.7 V ≤ EV_{DD} ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. V_b[V]: Communication line voltage

2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 5, 8)

3. f_{MCK}: Serial array unit operation clock frequency

(Operating clock that is set with the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))