Renesas Electronics America Inc - R5F10NLGDFB#50 Datasheet

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Applications of "Embedded - Microcontrollers"

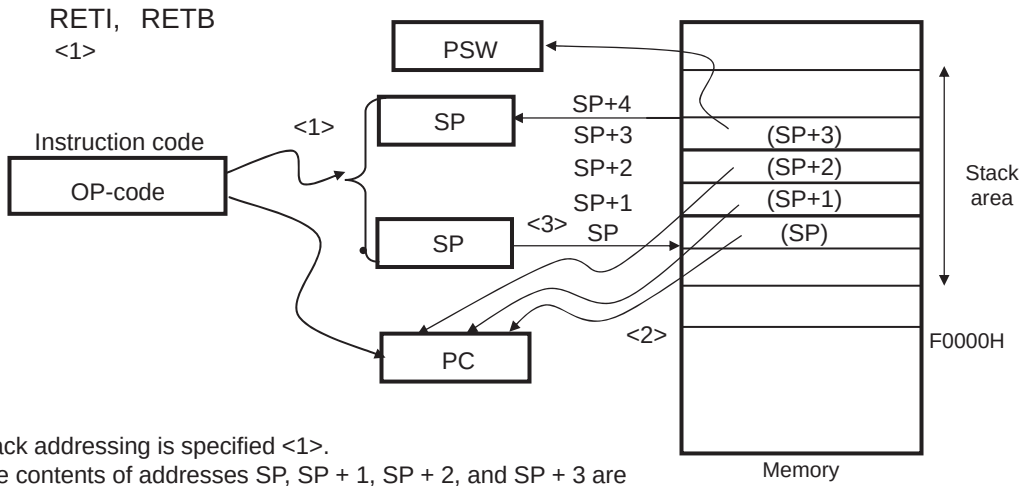
Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, IrDA, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 5.5V
Data Converters	A/D 4x10b, 4x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10nlgdfb-50

Table 3-6. Extended SFR (2nd SFR) List (11/11)

	Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
	F059CH	Year alarm register	RYRAR	R/W	–	–	√	Undefined
<R>	F059DH							
	F059CH	Binary counter 2 alarm enable register	BCNT2AER	R/W	–	–	√	Undefined
<R>	F059DH							
<R>	F059FH	Year alarm enable register	RYRAREN	R/W	–	√	–	Undefined
<R>	F059FH	Binary counter 3 alarm enable register	BCNT3AER	R/W	–	√	–	Undefined
<R>	F05A1H	RTC status register	RSR	R/W	–	√	–	Undefined
	F05A3H	RTC control register 1	RCR1	R/W	–	√	–	Undefined
	F05A5H	RTC control register 2	RCR2	R/W	–	√	–	Undefined
	F05A7H	RTC control register 3	RCR3	R/W	–	√	–	Undefined
	F05A9H	RTC control register 4	RCR4	R/W	–	√	–	Undefined
	F05AFH	Time error correction register	RADJ	R/W	–	√	–	Undefined
	F05B3H	RTC control register 5	RCR5	R/W	–	√	–	Undefined
	F05B9H	RCR5 guard register	RCR5GD	W	–	√	–	00H
	F05C1H	Time capture control register 0	RTCCR0	R/W	–	√	–	Undefined
	F05C3H	Time capture control register 1	RTCCR1	R/W	–	√	–	Undefined
	F05C5H	Time capture control register 2	RTCCR2	R/W	–	√	–	Undefined
	F05D3H	Second capture register 0	RSECCP0	R	–	√	–	Undefined
<R>	F05D3H	BCNT 0 capture register 0	BCNT0CP0	R	–	√	–	Undefined
	F05D5H	Minute capture register 0	RMINCP0	R	–	√	–	Undefined
<R>	F05D5H	BCNT 1 capture register 0	BCNT1CP0	R	–	√	–	Undefined
	F05D7H	Hour capture register 0	RHRCP0	R	–	√	–	Undefined
<R>	F05D7H	BCNT 2 capture register 0	BCNT2CP0	R	–	√	–	Undefined
	F05DBH	Day capture register 0	RDAYCP0	R	–	√	–	Undefined
<R>	F05DBH	BCNT 3 capture register 0	BCNT3CP0	R	–	√	–	Undefined
	F05DDH	Month capture register 0	RMONCP0	R	–	√	–	Undefined
	F05E3H	Second capture register 1	RSECCP1	R	–	√	–	Undefined
<R>	F05E3H	BCNT 0 capture register 1	BCNT0CP1	R	–	√	–	Undefined
	F05E5H	Minute capture register 1	RMINCP1	R	–	√	–	Undefined
<R>	F05E5H	BCNT 1 capture register 1	BCNT1CP1	R	–	√	–	Undefined
	F05E7H	Hour capture register 1	RHRCP1	R	–	√	–	Undefined
<R>	F05E7H	BCNT 2 capture register 1	BCNT2CP1	R	–	√	–	Undefined
	F05EBH	Day capture register 1	RDAYCP1	R	–	√	–	Undefined
<R>	F05EBH	BCNT 3 capture register 1	BCNT3CP1	R	–	√	–	Undefined
	F05EDH	Month capture register 1	RMONCP1	R	–	√	–	Undefined
	F05F3H	Second capture register 2	RSECCP2	R	–	√	–	Undefined
<R>	F05F3H	BCNT 0 capture register 2	BCNT0CP2	R	–	√	–	Undefined
	F05F5H	Minute capture register 2	RMINCP2	R	–	√	–	Undefined
<R>	F05F5H	BCNT 1 capture register 2	BCNT1CP2	R	–	√	–	Undefined
	F05F7H	Hour capture register 2	RHRCP2	R	–	√	–	Undefined
<R>	F05F7H	BCNT 2 capture register 2	BCNT2CP2	R	–	√	–	Undefined
	F05FBH	Day capture register 2	RDAYCP2	R	–	√	–	Undefined
<R>	F05FBH	BCNT 3 capture register 2	BCNT3CP2	R	–	√	–	Undefined
	F05FDH	Month capture register 2	RMONCP2	R	–	√	–	Undefined

Remark For SFRs in the SFR area, see **Table 3-5 SFR List**.

Figure 3-39. Example of RETI, RETB



- Stack addressing is specified <1>.
- The contents of addresses SP, SP + 1, SP + 2, and SP + 3 are stored in PC bits 7 to 0, 15 to 8, 19 to 16, and the PSW, respectively <2>.
- The value of SP <3> is increased by four.

6.3.12 Middle-speed on-chip oscillator frequency select register (MOCODIV)

The MOCODIV register is used to select the division ratio of the middle-speed on-chip oscillator.

The MOCODIV register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 6 - 15 Format of Middle-speed on-chip oscillator frequency select register (MOCODIV)

Address: F00F2H After reset: 00H R/W

Symbol	<7>	6	5	<4>	<3>	2	1	0
MOCODIV	0	0	0	0	0	0	MOCODIV1	MOCODIV0

MOCODIV1	MOCODIV0	Selection of middle-speed on-chip oscillator clock frequency
0	0	4 MHz
0	1	2 MHz
1	0	1 MHz
Other than above		Setting prohibited

Table 6 - 3 CPU Clock Transition and SFR Register Setting Examples (4/5)

(6) Changing the CPU to subsystem clock operation (E)
Target state transition: (B) → (E), (C) → (E), (D) → (E)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Clock After Change	PER2 Register	SCMC Register Note			
	VRTCEN	EXCLKS	OSCSELS	AMPHS1	AMPHS0
Changing to XT1 clock	1	0	1	0/1	0/1
Changing to external sub clock	1	1	1	×	×

Unnecessary if these registers are already set

→

SCSC Register	CMC Register	Waiting for Oscillation Stabilization	CSC Register	CKC Register	PER2 Register
XTSTOP	XT1SELEN		XT1SELDIS	CSS	VRTCEN
0	1	Necessary	0	1	0
×	1	Necessary	0	1	0

Unnecessary if the CPU is operating with the subsystem clock

Note After release from the reset state, the sub clock operation mode control register (SCMC) can be written only once by an 8-bit memory manipulation instruction.

Operation is possible after turning on the power supply to the VRTC pin and release from the RTC power-on reset.

(7) Changing to low-speed on-chip oscillator clock operation (F)
Target state transition: (B) → (F), (C) → (F), (D) → (F)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Clock After Change	CKSEL	Oscillation accuracy stabilization time	CKC Register
	SELLOSC		CSS
Changing to low-speed on-chip oscillator	1	210 μs	1

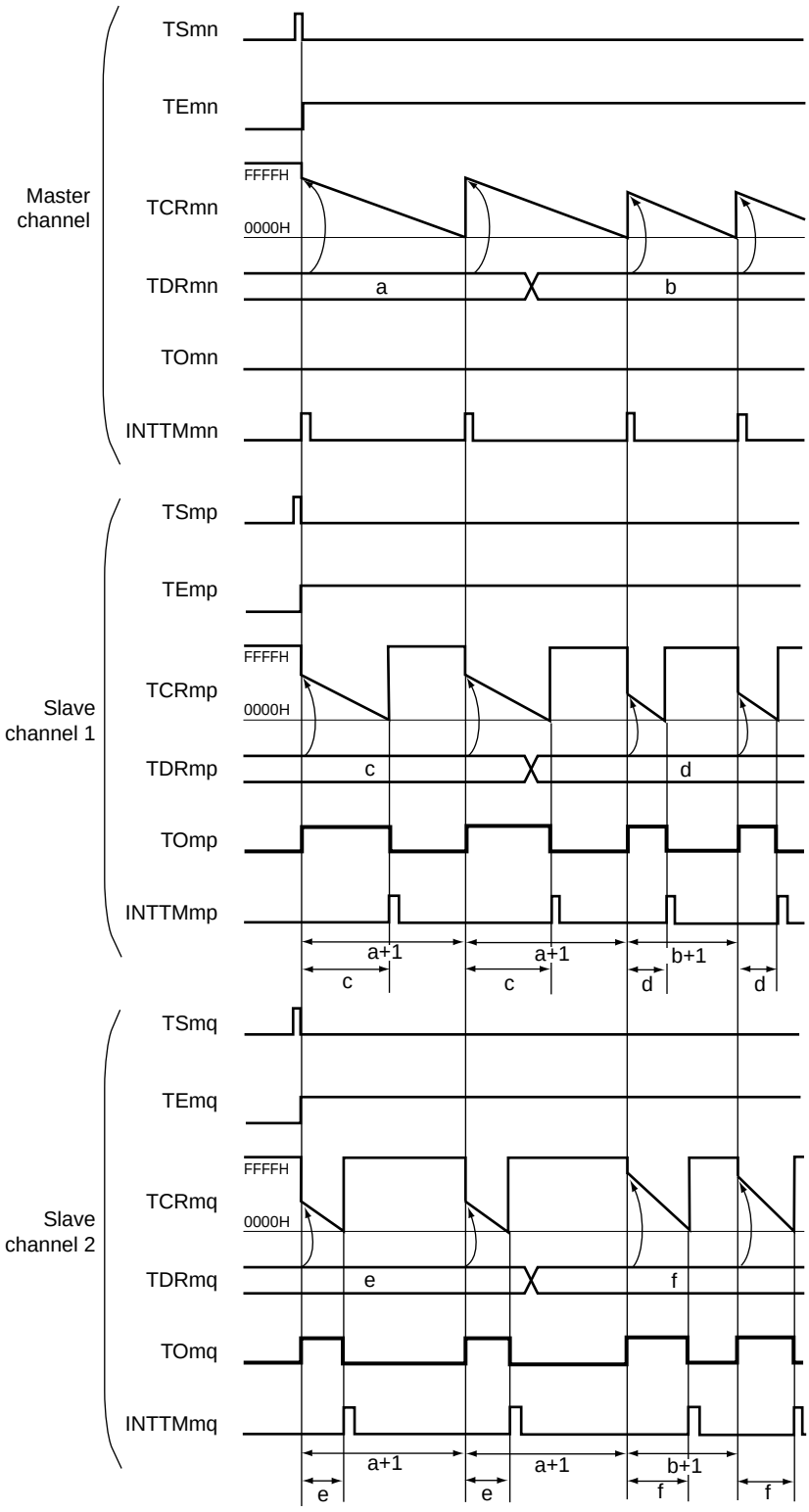
Unnecessary if the CPU is operating with the low-speed on-chip oscillator clock

Remark 1. ×: don't care
Remark 2. (A) to (R) in table 6 - 3 correspond to (A) to (R) in Figure 6 - 24.

Table 6 - 4 Changing CPU Clock (5/6)

CPU Clock		Condition Before Change	Processing After Change
Before Change	After Change		
<R> External subsystem clock	High-speed on-chip oscillator clock	Oscillation of high-speed on-chip oscillator and selection of high-speed on-chip oscillator clock as main system clock • HIOSTOP = 0, MCS = 0, MCS1 = 0	External subsystem clock input can be disabled (XTSTOP = 1) after checking that the CPU clock has been switched to the clock after transition.
	Middle-speed on-chip oscillator clock	Oscillation of middle-speed on-chip oscillator and selection of middle-speed on-chip oscillator clock • MIOEN = 1, MCS = 0, MCS1 = 1	
	PLL clock	Setting prohibited (switch to the high-speed on-chip oscillator clock first, and then switch to the PLL clock)	—
<R>	X1 clock	Stabilization of X1 oscillation and selection of high-speed system clock as main system clock • OSCSEL = 1, EXCLK = 0, MSTOP = 0 • After elapse of oscillation stabilization time • MCS = 1	External subsystem clock input can be disabled (XTSTOP = 1) after checking that the CPU clock has been switched to the clock after transition.
	External main system clock	Enabling input of external clock from the EXCLK pin and selection of high-speed system clock as main system clock • OSCSEL = 1, EXCLK = 1, MSTOP = 0 • MCS = 1	
	XT1 clock	Transition not possible	—
	External subsystem clock	Transition not possible	

Figure 8-76. Example of Basic Timing of Operation as Multiple PWM Output Function (Output Two Types of PWMs)



(**Remark** is listed on the next page.)

15.3.4 A/D converter mode register 1 (ADM1)

This register is used to specify the A/D conversion trigger, conversion mode, and hardware trigger signal.

The ADM1 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 15-7. Format of A/D Converter Mode Register 1 (ADM1)

Address: FFF32H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADM1	ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0

ADTMD1	ADTMD0	Selection of the A/D conversion trigger mode
0	×	Software trigger mode
1	0	Hardware trigger no-wait mode
1	1	Hardware trigger wait mode

ADSCM	Specification of the A/D conversion mode
0	Sequential conversion mode
1	One-shot conversion mode

ADTRS1	ADTRS0	Selection of the hardware trigger signal
0	0	End of timer channel 01 count or capture interrupt signal (INTTM01)
0	1	Event signal selected by ELC
1	0	Independent power supply RTC alarm interrupt signal (INTRTCALM), independent power supply RTC fixed-cycle interrupt signal (INTRTCPRD)
1	1	12-bit interval timer interrupt signal (INTIT)

<R>

Cautions 1. Rewrite the value of the ADM1 register while conversion is stopped (ADCS = 0, ADCE = 0).

2. To complete A/D conversion, specify at least the following time as the hardware trigger interval:
Hardware trigger no wait mode: 2 f_{CLK} clock + conversion start time + A/D conversion time
Hardware trigger wait mode: 2 f_{CLK} clock + conversion start time + A/D power supply stabilization wait time + A/D conversion time

<R>

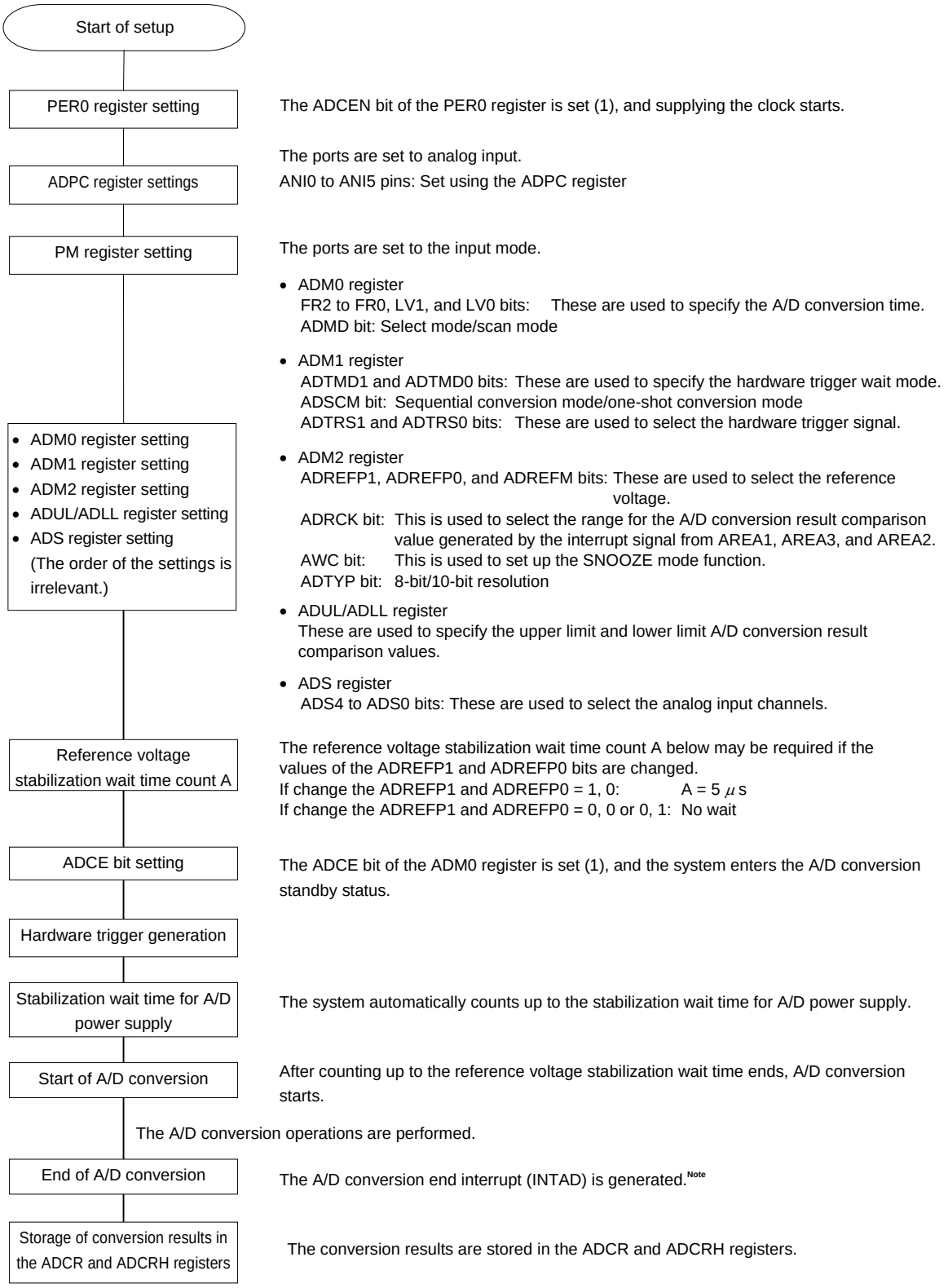
3. In modes other than SNOOZE mode, input of the next INTRTCALM/INTRTCPRD or INTIT will not be recognized as a valid hardware trigger for up to four f_{CLK} cycles after the first INTRTCALM/INTRTCPRD or INTIT is input.

Remarks 1. ×: don't care

2. f_{CLK}: CPU/peripheral hardware clock frequency

15.7.3 Setting up hardware trigger wait mode

Figure 15-32. Setting up Hardware Trigger Wait Mode



Note Depending on the settings of the ADRCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR, ADCRH registers.

17.2.4 ΔΣ A/D converter HPF control register (DSADHPFCR)

The DSADHPFCR register is used to select the cutoff frequency of the high pass filter and disable or enable the high-pass filter for each channel.

DSADHPFCR can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 17-6. Format of ΔΣ A/D Converter HPF Control Register (DSADHPFCR)

Address: F03C5H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
DSADHPFCR	DSADCOF1	DSADCOF0	0	0	DSADTHR3	DSADTHR2	DSADTHR1	DSADTHR0

DSADCOF1	DSADCOF0	Selection of cutoff frequency of high-pass filter
Bit 7	Bit 6	
0	0	0.607 Hz
0	1	1.214 Hz
1	0	2.429 Hz
1	1	4.857 Hz

DSADTHR3	High-pass filter disable of channel 3
0	High-pass filter used
1	High-pass filter not used

DSADTHR2	High-pass filter disable of channel 2
0	High-pass filter used
1	High-pass filter not used

DSADTHR1	High-pass filter disable of channel 1
0	High-pass filter used
1	High-pass filter not used

DSADTHR0	High-pass filter disable of channel 0
0	High-pass filter used
1	High-pass filter not used

Cautions 1. Be sure to clear bits 5 and 4 to "0".

2. Writing to the DSADTHRn bit shall be completed when any of the following conditions is satisfied:

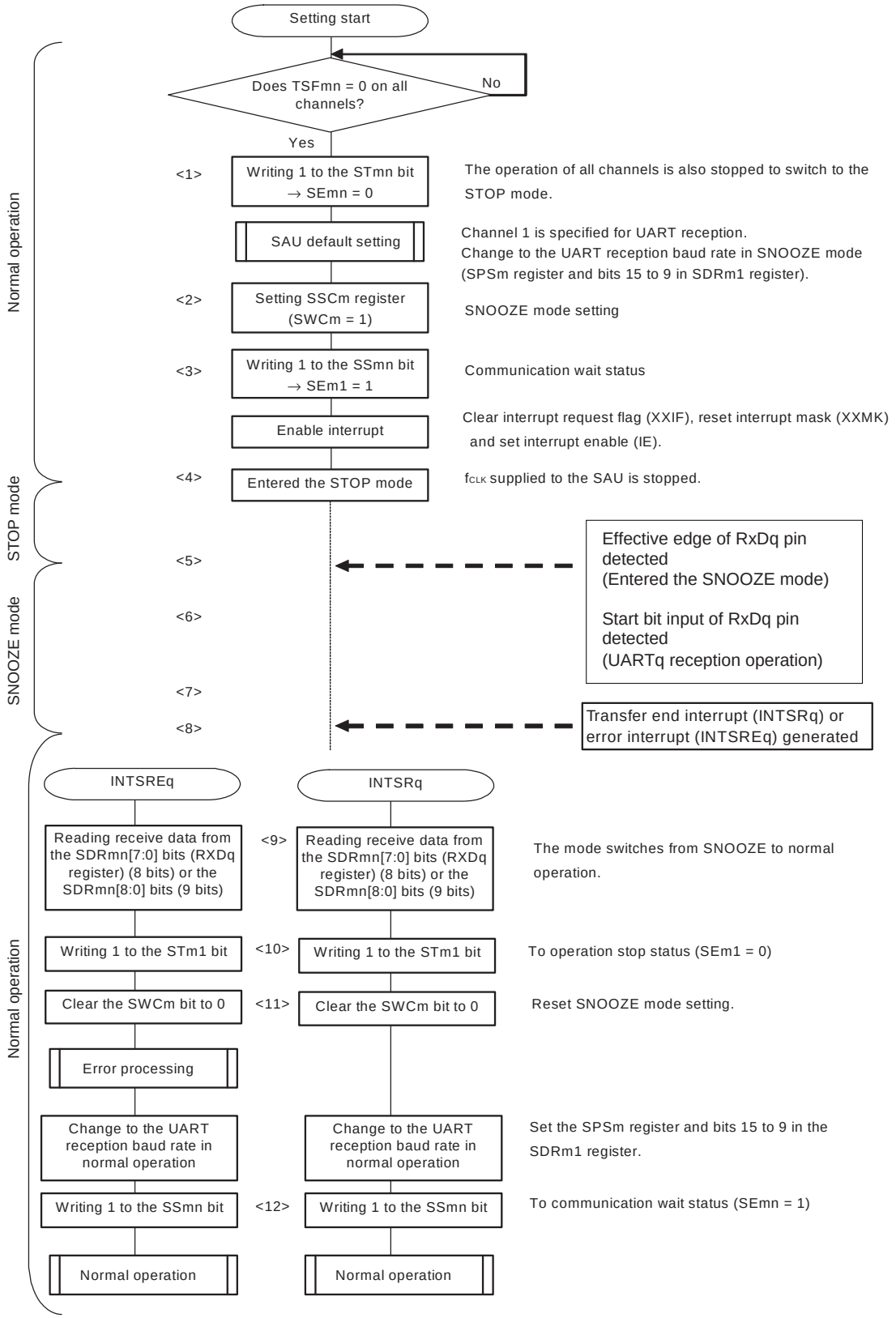
- **DSADCEn = 0 (Conversion is being stopped)**
- **Within 21 μs from the zero-cross detection interrupt**

Remark The high-pass filter convergence time can be changed by changing the high-pass filter cut-off frequency. The convergence time decreases as the cut-off frequency increases.

To initialize the high-pass filter, use the DSADRES bit of the peripheral reset control register (PRR1).

Figure 18-93. Flowchart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1 or EOCm1 = 1, SSECm = 0)

<R>

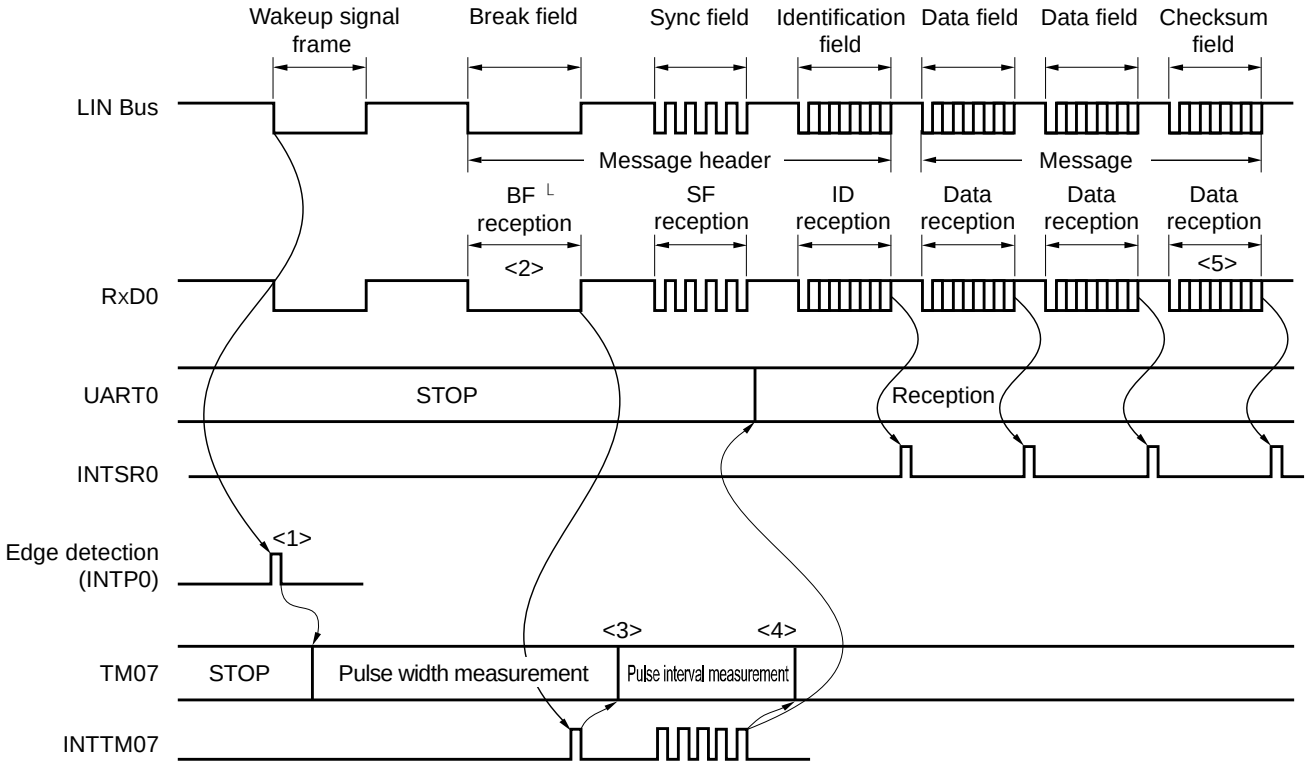


Remarks 1. <1> to <12> in the figure correspond to <1> to <12> in **Figure 18-91 Timing Chart of SNOOZE Mode Operation (EOCm1 = 0, SSECm = 0/1)** and **Figure 18-92 Timing Chart of SNOOZE Mode Operation (EOCm1 = 1, SSECm = 0)**.

2. m = 0; q = 0

<R>

Figure 18-101. Reception Operation of LIN



Here is the flow of signal processing.

<1> The wakeup signal is detected by detecting an interrupt edge (INTP0) on a pin. When the wakeup signal is detected, change TM07 to pulse width measurement upon detection of the wakeup signal to measure the low-level width of the BF signal. Then wait for BF signal reception.

<2> TM07 starts measuring the low-level width upon detection of the falling edge of the BF signal, and then captures the data upon detection of the rising edge of the BF signal. The captured data is used to judge whether it is the BF signal.

<3> When the BF signal has been received normally, change TM07 to pulse interval measurement and measure the interval between the falling edges of the RxD0 signal in the Sync field four times.

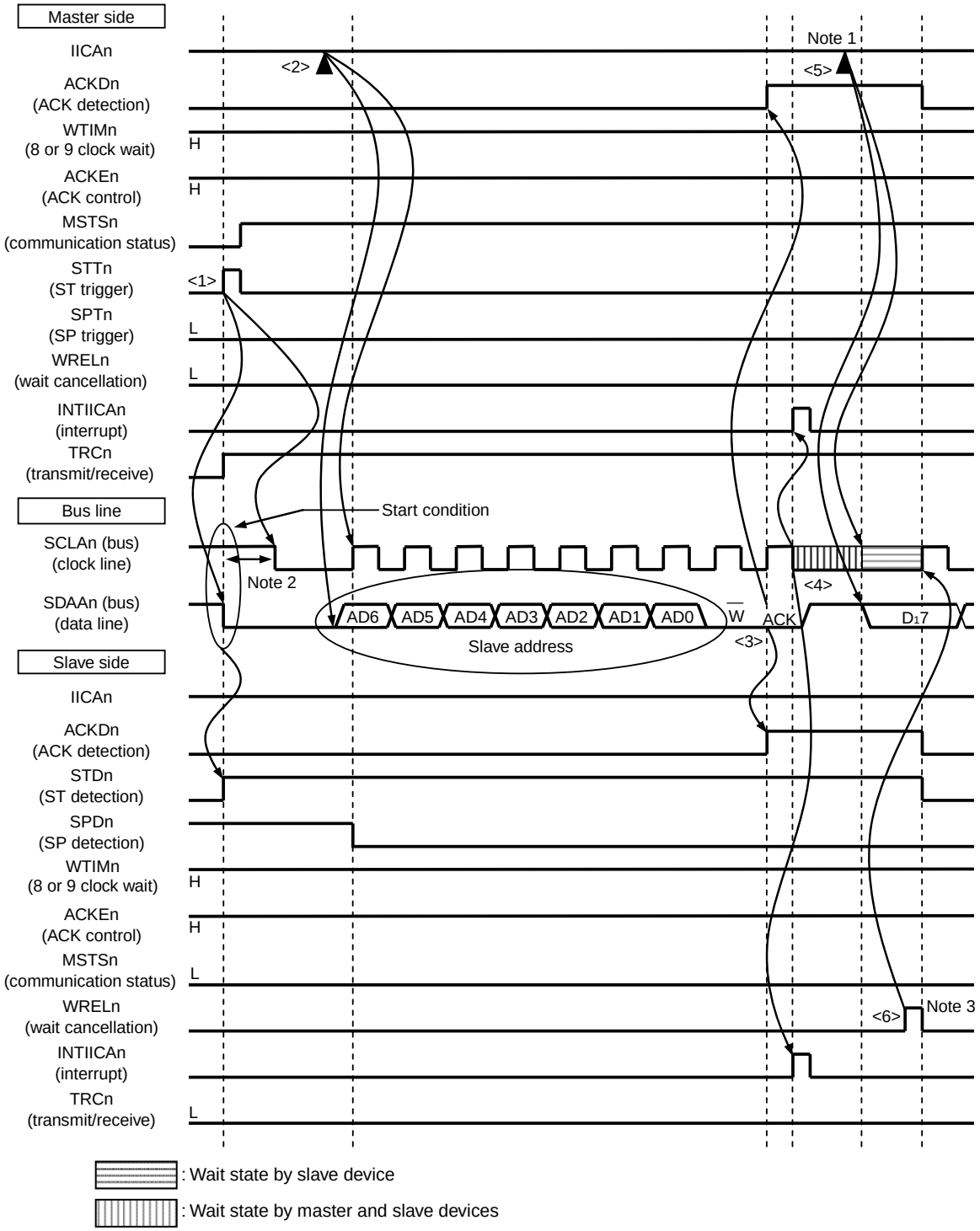
<4> When BF reception has been correctly completed, start channel 7 of the timer array unit and measure the bit interval (pulse width) of the sync field (see **8.8.3 Operation as input pulse interval measurement**).

<5> Calculate a baud rate error from the bit interval of sync field (SF). Stop UART0 once and adjust (re-set) the baud rate.

<6> The checksum field should be distinguished by software. In addition, processing to initialize UART0 after the checksum field is received and to wait for reception of BF should also be performed by software.

Figure 19-33. Example of Master to Slave Communication (9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (1/4)

(1) Start condition ~ address ~ data



Notes 1. Write data to IICAn, not setting the WRELn bit, in order to cancel a wait state during transmission by a master device.

2. Make sure that the time between the fall of the SDAAn pin signal and the fall of the SCLAn pin signal is at least 4.0 μs when specifying standard mode and at least 0.6 μs when specifying fast mode.

3. For releasing wait state during reception of a slave device, write “FFH” to IICAn or set the WRELn bit.

Remark n = 0

The following is a description of the Figure 19-33 (3) Data ~ data ~ stop condition <7> to <15>.

<7> After data transfer is completed, because of ACKEn = 1, the slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKDn = 1) at the rising edge of the 9th clock.

<8> The master device and slave device set a wait status (SCLAn = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICAn: end of transfer).

<9> The master device writes the data to transmit to the IICA shift register n (IICAn) and releases the wait status that it set by the master device.

<10> The slave device reads the received data and releases the wait status (WRELn = 1). The master device then starts transferring data to the slave device.

<11> When data transfer is complete, the slave device (ACKEn =1) sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKDn = 1) at the rising edge of the 9th clock.

<12> The master device and slave device set a wait status (SCLAn = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICAn: end of transfer).

<13> The slave device reads the received data and releases the wait status (WRELn = 1).

<14> By the master device setting a stop condition trigger (SPTn = 1), the bus data line is cleared (SDAAn = 0) and the bus clock line is set (SCLAn = 1). After the stop condition setup time has elapsed, by setting the bus data line (SDAAn = 1), the stop condition is then generated (i.e. SCLAn =1 changes SDAAn from 0 to 1).

<15> When a stop condition is generated, the slave device detects the stop condition and issues an interrupt (INTIICAn: stop condition).

Remarks 1. <1> to <15> in Figure 19-33 represent the entire procedure for communicating data using the I^2C bus.

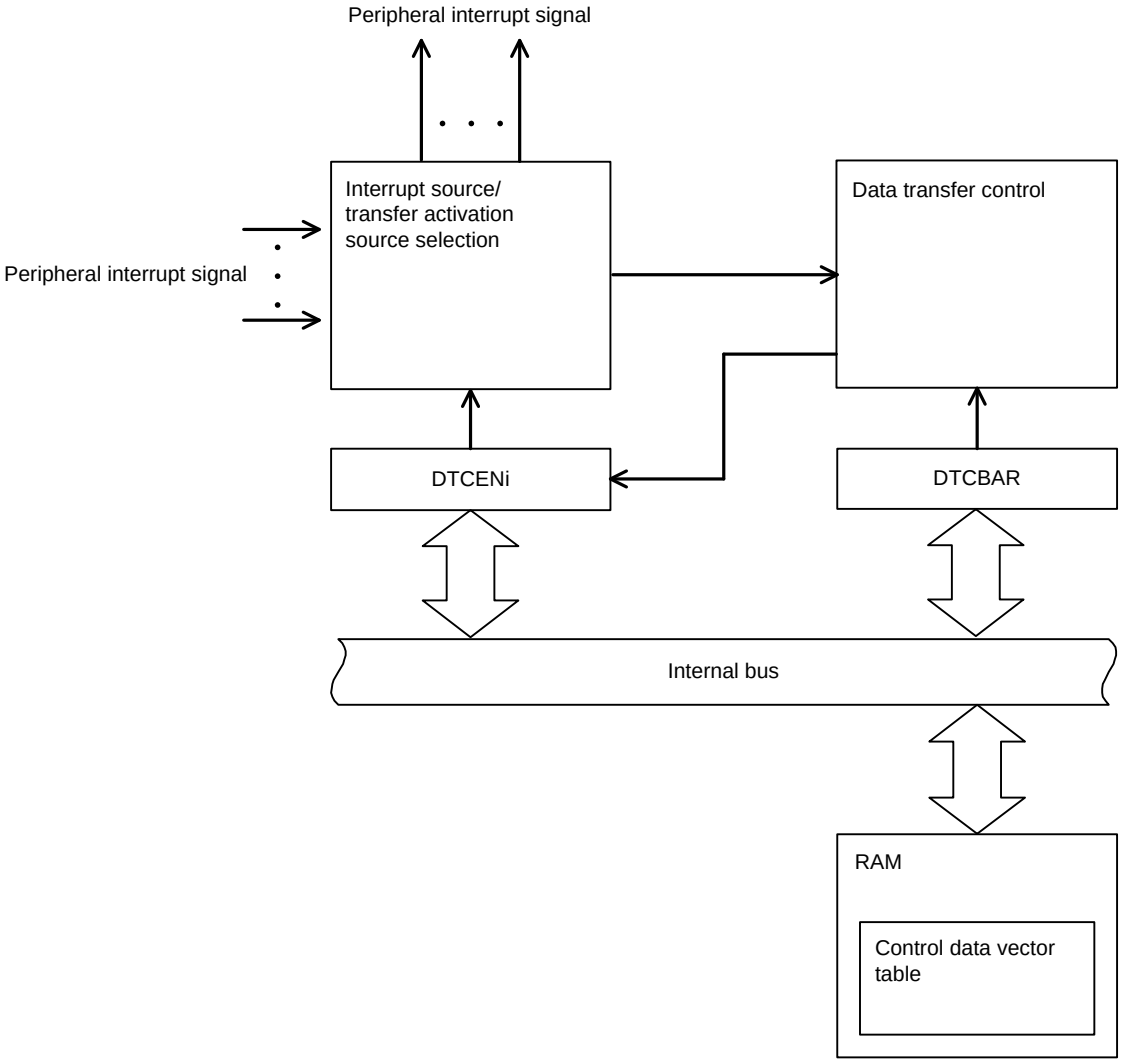
Figure 19-33 (1) Start condition ~ address ~ data shows the processing from <1> to <6>, Figure 19-33 (2) Address ~ data ~ data shows the processing from <3> to <10>, and Figure 19-33 (3) Data ~ data ~ stop condition shows the processing from <7> to <15>.

2. n = 0

22.2 Configuration of DTC

Figure 22-1 shows the DTC block diagram.

Figure 22-1. DTC Block Diagram



25.3.3 Key return flag register (KRF)

This register controls the key interrupt flags (KRF0 to KRF7).

The KRF register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 25 - 4 Format of Key return flag register (KRF)

Address: FFF35H After reset: 00H R/W Note

Symbol	7	6	5	4	3	2	1	0
KRF	KRF7	KRF6	KRF5	KRF4	KRF3	KRF2	KRF1	KRF0

KRFn	Key interrupt flag (n = 0 to 7)
0	No key interrupt signal has been detected.
1	A key interrupt signal has been detected.

Note Writing to 1 is invalid. To clear the KRFn bit, write 0 to the corresponding bit and 1 to the other bits using an 8-bit memory manipulation instruction.

27.3.2 Power-on-reset status register (PORSR)

The PORSR register is used to check the occurrence of a power-on reset.

Writing “1” to bit 0 (PORF) of the PORSR register is valid, and writing “0” is ignored.

Write 1 to the PORF bit in advance to enable checking of the occurrence of a power-on reset.

The PORSR register can be set by an 8-bit memory manipulation instruction.

Power-on reset signal generation clears this register to 00H.

Cautions 1. The PORSR register is reset only by a power-on reset; it retains the value when a reset caused by another factor occurs.

2. If the PORF bit is set to 1, it guarantees that no power-on reset has occurred, but it does not guarantee that the RAM value is retained.

Figure 27-6. Format of Power-on-Reset Status Register (PORSR)

Address: F00F9H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PORSR	0	0	0	0	0	0	0	PORF

PORF	Checking occurrence of power-on reset
0	A value 1 has not been written, or a power-on reset has occurred.
1	No power-on reset has occurred.

27.3.3 RTC power-on-reset status register (RTCPORSR)

<R> The RTCPORSR register is used to check the occurrence of an RTC Power-on reset.

Writing 1 to bit 0 (RTCPORF) of the RTCPORSR register enables this function. Writing 0 disables this function.

Write 1 to the RTCPORF bit in advance to enable checking of the occurrence of an RTC power-on reset.

The RTCPORSR register can be set by an 8-bit memory manipulation instruction.

Generation of the RTC power-on reset signal clears this register to 00H. This register is not reset by other reset sources (including the power-on reset of the internal V_{DD} power supply).

Caution The RTCPORSR register is reset only by an RTC power-on reset; it retains the value when a reset caused by another source occurs.

Figure 27-7. Format of RTC power-on-reset status register (RTCPORSR)

Address: F0380H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
RTCPORSR	0	0	0	0	0	0	0	RTCPORF

<R>

RTCPORF	Checking occurrence of RTC Power-on reset
0	A value 1 has not been written, or an RTC power-on reset has occurred.
1	No RTC power-on reset has occurred.

29.3.5 VRTC pin voltage detection control register (LVDVRTC)

This register is used to enable/disable VRTC pin voltage detection and select the detection voltage.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation input sets this register to 00H.

Figure 29 - 13 Format of Voltage detection control register for VRTC pin (LVDVRTC)

Address: F0334H After reset: 00H R/W Note 1

Symbol	<7>	<6>	5	4	3	2	1	0
LVDVRTC	LVDVRTCEN	LVDVRTCF	0	0	0	0	LVDVRTC1	LVDVRTC0

LVDVRTCEN	VRTC pin voltage detection enable/disable
0	Disables detection Note 3
1	Enables detection

LVDVRTCF Note 2	VRTC pin voltage detection flag
0	Supply voltage (VRTC) ≥ detection voltage ($V_{LVDVRTC}$), or detection is off
1	Supply voltage (VRTC) < detection voltage ($V_{LVDVRTC}$)

LVDVRTC1	LVDVRTC0	Detection voltage ($V_{LVDVRTC}$)	
		Rising edge	Falling edge
0	0	2.22 V	2.16 V
0	1	2.43 V	2.37 V
1	0	2.63 V	2.57 V
1	1	2.84 V	2.78 V

Note 1. Bit 6 is read only.

Note 2. When the LVDVRTCEN bit is set to 1 while voltage of VRTC pin < detection voltage ($V_{LVDVRTC}$), the LVDVRTCF bit is undefined until the stabilization time (300 μs) elapses.

Note 3. To disable INTLVDVRTC generation, do the followig steps.

Figure 29 - 14 Setting procedure to disable VRTC voltage detection function

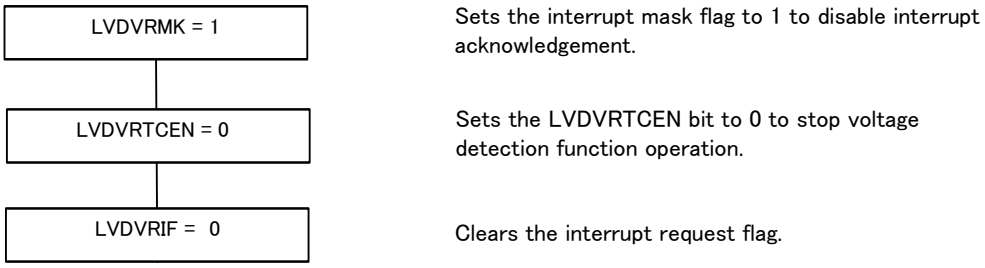


Figure 35-2. Format of User Option Byte (000C1H/010C1H) (2/2)

Address: 000C1H/010C1H[Note]

7	6	5	4	3	2	1	0
VPOC2	VPOC1	VPOC0	1	LVIS1	LVIS0	LVIMDS1	LVIMDS0

- LVD setting (interrupt mode)

Detection voltage		Option byte setting value						
V_{LVD}		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge						LVIMDS1	LVIMDS0
1.77 V	1.73 V	0	0	0	1	0	0	1
1.88 V	1.84 V		0	1	1	1		
1.98 V	1.94 V		0	1	1	0		
2.09 V	2.04 V		0	1	0	1		
2.50 V	2.45 V		1	0	1	1		
2.61 V	2.55 V		1	0	1	0		
2.71 V	2.65 V		1	0	0	1		
2.81 V	2.75 V		1	1	1	1		
2.92 V	2.86 V		1	1	1	0		
3.02 V	2.96 V		1	1	0	1		
3.13 V	3.06 V		0	1	0	0		
3.75 V	3.67 V		1	0	0	0		
4.06 V	3.98 V		1	1	0	0		
–		Setting of values other than above is prohibited.						

- LVD off setting (use of external reset input via $\overline{\text{RESET}}$ pin)

Detection voltage		Option byte setting value						
V_{LVD}		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge						LVIMDS1	LVIMDS0
–	–	1	×	×	×	×	×	1
–		Setting of values other than above is prohibited.						

Note Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

Cautions 1. Be sure to set bit 4 to "1".

2. After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in 41.4 AC Characteristics. This is done by utilizing the voltage detector or controlling the externally input reset signal. After the power supply is turned off, this LSI should be placed in the STOP mode, or placed in the reset state by utilizing the voltage detector or controlling the externally input reset signal, before the voltage falls below the operating range. The range of operating voltage varies with the setting of the user option byte (000C2H or 010C2H).

Remarks 1. ×: don't care

2. For LVD setting, see **29.1 Functions of Voltage Detector**.

3. The detection voltage is a typical value. For details, see **41.6.5 LVD circuit characteristics.**

41.6.4 POR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	When power supply rises[Note 1]	1.47	1.51	1.55	V
	V_{PDR}	When power supply falls[Note 2]	1.46	1.50	1.54	V

Notes 1. Be sure to maintain the reset state until the power supply voltage rises over the minimum V_{DD} value in the operating voltage range specified in **41.4 AC Characteristics**, by using the voltage detector or external reset pin.

2. If the power supply voltage falls while the voltage detector is off, be sure to either shift to STOP mode or execute a reset by using the voltage detector or external reset pin before the power supply voltage falls below the minimum operating voltage specified in **41.4 AC Characteristics**.

41.6.5 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = –40 to +85°C, $V_{PDR} \leq V_{DD}$[Note] ≤ 5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	When power supply rises	3.98	4.06	4.24	V
			When power supply falls	3.90	3.98	4.16	V
		V_{LVD1}	When power supply rises	3.68	3.75	3.92	V
			When power supply falls	3.60	3.67	3.84	V
		V_{LVD2}	When power supply rises	3.07	3.13	3.29	V
			When power supply falls	3.00	3.06	3.22	V
		V_{LVD3}	When power supply rises	2.96	3.02	3.18	V
			When power supply falls	2.90	2.96	3.12	V
		V_{LVD4}	When power supply rises	2.86	2.92	3.07	V
			When power supply falls	2.80	2.86	3.01	V
		V_{LVD5}	When power supply rises	2.76	2.81	2.97	V
			When power supply falls	2.70	2.75	2.91	V
		V_{LVD6}	When power supply rises	2.66	2.71	2.86	V
			When power supply falls	2.60	2.65	2.80	V
		V_{LVD7}	When power supply rises	2.56	2.61	2.76	V
			When power supply falls	2.50	2.55	2.70	V
		V_{LVD8}	When power supply rises	2.45	2.50	2.65	V
			When power supply falls	2.40	2.45	2.60	V
		V_{LVD9}	When power supply rises	2.05	2.09	2.23	V
			When power supply falls	2.00	2.04	2.18	V
		V_{LVD10}	When power supply rises	1.94	1.98	2.12	V
			When power supply falls	1.90	1.94	2.08	V
		V_{LVD11}	When power supply rises	1.84	1.88	2.01	V
			When power supply falls	1.80	1.84	1.97	V
		V_{LVD12}	When power supply rises	1.74	1.77	1.81	V
			When power supply falls	1.70	1.73	1.77	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

Note Either V_{DD} or VBAT is selected by the battery backup function.

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