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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, IrDA, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 5.5V
Data Converters	A/D 4x10b, 3x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10nmedfb-30

3.4.5 SFR addressing

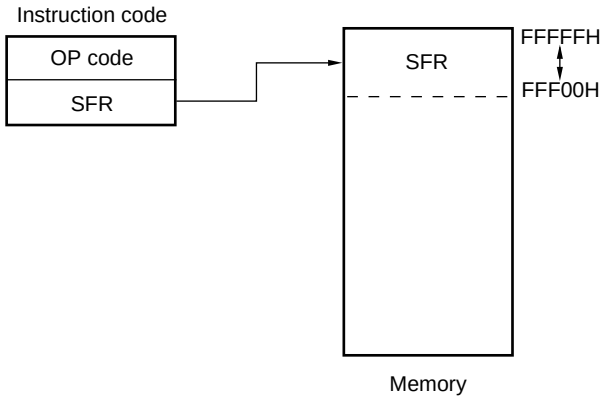
[Function]

SFR addressing directly specifies the target SFR addresses using 8-bit data in the instruction word. This type of addressing is applied only to the space from FFF00H to FFFFFH.

[Operand format]

Identifier	Description
SFR	SFR name
SFRP	16-bit-manipulatable SFR name (even address)

Figure 3-22. Outline of SFR Addressing



(2) Subsystem clock

<1> XT1 clock oscillator

This circuit oscillates a clock of f_{XT} = 32.768 kHz by connecting a 32.768 kHz resonator to XT1 pin and XT2 pin. Oscillation can be stopped by setting the XTSTOP bit (bit 6 of the clock operation status control register (CSC)).

An external subsystem clock (f_{EXS} = 32.768 kHz) can also be supplied from the EXCLKS/XT2/P124 pin. An external subsystem clock input can be disabled by the setting of the XTSTOP bit.

<2> Low-speed on-chip oscillator

This circuit oscillates a clock of f_{IL} = 15 kHz (TYP.).

The low-speed on-chip oscillator clock can be used as the CPU clock. The following peripheral hardware is driven by the low-speed on-chip oscillator clock.

- Watchdog timer
- 12-bit interval timer
- 8-bit interval timer
- Frequency measurement circuit
- Oscillation stop detection circuit
- LCD controller/driver

This clock operates when any bit among bit 4 (WDTON) of the option byte (000C0H), bit 4 (WUTMMCK0) of the subsystem clock supply option control register (OSMC), or bit 0 of the subsystem clock select register (CKSEL) is set to 1 (including multiple bits).
However, when WDTON = 1, WUTMMCK0 = 0, SELLOSC = 0, and bit 0 (WDSTBYON) of the option byte (000C0H) is 0, oscillation of the low-speed on-chip oscillator stops if the HALT or STOP instruction is executed.

Remark f_X: X1 clock oscillation frequency
f_{IH}: High-speed on-chip oscillator clock frequency (24 MHz max.)
f_{IM}: Middle-speed on-chip oscillator clock frequency
f_{EX}: External main system clock frequency
f_{XT}: XT1 clock oscillation frequency
f_{EXS}: External subsystem clock frequency
f_{IL}: Low-speed on-chip oscillator frequency
f_{PLL}: PLL clock frequency

6.6.3 Example of setting XT1 oscillation clock

After release from the reset state (except that following the RTC power-on reset), the high-speed on-chip oscillator clock is always the initial CPU/peripheral hardware clock (f_{CLK}).

After turning on the power supply to the VRTC pin and release from the RTC power-on reset, the XT1 oscillator and RTC circuit can operate.

To subsequently change the CPU/peripheral hardware clock (f_{CLK}) to the XT1 oscillation clock, set the oscillator and start oscillation by using the subsystem clock supply option control register (OSMC), sub clock operation mode control register (SCMC), clock operation mode control register (CMC), clock operation status control register (CSC), and sub clock operation status control register (SCSC), set the XT1 oscillation clock to f_{CLK} by using the system clock control register (CKC).

[Register settings] Set the register in the order of <1> to <10> below.

<1> Turn on the power supply to the VRTC pin, and release the RTC power-on reset.

<2> To operate the frequency measurement circuit, 12-bit interval timer, 8-bit interval timer, clock output/buzzer output, oscillation stop detection circuit, and LCD controller/driver wit the sub-system clock (ultra-low current consumption) in STOP mode or in HALT mode while CPU is operating with the sub-system clock, set the RTCLPC bit to 1.

	7	6	5	4	3	2	1	0
OSMC	RTCLPC 0/1	0	0	WUTMMCK0 0	0	0	0	0

<3> Set (1) the VRTCEN bit in the PER2 register to permit access to the SFRs in the VRTC power-supply domain.

<4> Set the EXCLKS, OSCSELS, AMPHS1, and AMPHS0 bits in the SCMC register, and set the XT1 oscillation mode and the gain for the XT1 oscillator.

.

	7	6	5	4	3	2	1	0
SCMC	0	0	EXCLKS 0	OSCSELS 1	0	AMPHS1 0/1	AMPHS0 0/1	0

AMPHS0 and AMPHS1 bits: These bits are used to specify the oscillation mode of the XT1 oscillator.

<5> Clear (0) the XTSTOP bit of the SCSC register to start oscillation of the XT1 oscillator.

	7	6	5	4	3	2	1	0
SCSC	0	XTSTOP 0	0	0	0	0	0	0

<6> Set (1) the XT1SELEN bit in the CMC register to permit selection of the XT1 clock as the CPU clock.

<7> Use the timer function or another function to wait for oscillation of the XT1 oscillation clock to stabilize by using software.

8.3.3 Timer clock select register m (TPSm)

The TPSm register is a 16-bit register that is used to select two types or four types of operation clocks (CKm0, CKm1, CKm2, CKm3) that are commonly supplied to each channel. CKm0 is selected by using bits 3 to 0 of the TPSm register, and CKm1 is selected by using bits 7 to 4 of the TPSm register. In addition, only for channels 1 and 3, CKm2 and CKm3 can be also selected. CKm2 is selected by using bits 9 and 8 of the TPSm register, and CKm3 is selected by using bits 13 and 12 of the TPSm register.

Rewriting of the TPSm register during timer operation is possible only in the following cases.

If the PRSm00 to PRSm03 bits can be rewritten (n = 0 to 7):
All channels for which CKm0 is selected as the operation clock (CKSmn1, CKSmn0 = 0, 0) are stopped (TEmn = 0).

If the PRSm10 to PRSm13 bits can be rewritten (n = 0 to 7):
All channels for which CKm2 is selected as the operation clock (CKSmn1, CKSmn0 = 0, 1) are stopped (TEmn = 0).

If the PRSm20 and PRSm21 bits can be rewritten (n = 1, 3):
All channels for which CKm1 is selected as the operation clock (CKSmn1, CKSmn0 = 1, 0) are stopped (TEmn = 0).

If the PRSm30 and PRSm31 bits can be rewritten (n = 1, 3):
All channels for which CKm3 is selected as the operation clock (CKSmn1, CKSmn0 = 1, 1) are stopped (TEmn = 0).

The TPSm register can be set by a 16-bit memory manipulation instruction.

Reset signal generation clears this register to 0000H.

Figure 8-15. Format of Timer Mode Register mn (TMRmn) (1/4)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 2, 4, 6)	CKS mn1	CKS mn0	0	CCS mn	MAST ERmn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 1, 3)	CKS mn1	CKS mn0	0	CCS mn	SPLIT mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 0, 5, 7)	CKS mn1	CKS mn0	0	CCS mn	0[Note]	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

CKS mn1	CKS mn0	Selection of operation clock (f_{MCK}) of channel n
0	0	Operation clock CKm0 set by timer clock select register m (TPSm)
0	1	Operation clock CKm2 set by timer clock select register m (TPSm)
1	0	Operation clock CKm1 set by timer clock select register m (TPSm)
1	1	Operation clock CKm3 set by timer clock select register m (TPSm)

Operation clock (f_{MCK}) is used by the edge detector. A count clock (f_{TCLK}) and a sampling clock are generated depending on the setting of the CCSmn bit.
The operation clocks CKm2 and CKm3 can only be selected for channels 1 and 3.

CCS mn	Selection of count clock (f_{TCLK}) of channel n
0	Operation clock (f_{MCK}) specified by the CKSmn0 and CKSmn1 bits
1	Valid edge of input signal input from the TImn pin In channels 0, 1, 5, 6, and 7, valid edge of input signal selected by TIS0

Count clock (f_{TCLK}) is used for the counter, output controller, and interrupt controller.

<R>

Note Bit 11 is fixed at 0 of read only, write is ignored.

Cautions 1. Be sure to clear bits 13, 5, and 4 to "0".

2. The timer array unit must be stopped (TTm = 00FFH) if the clock selected for f_{CLK} is changed (by changing the value of the system clock control register (CKC)), even if the operating clock specified by using the CKSmn0 and CKSmn1 bits (f_{MCK}) or the valid edge of the signal input from the TImn pin is selected as the count clock (f_{TCLK}).

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

8.3.12 Timer output level register m (TOLm)

The TOLm register is a register that controls the timer output level of each channel.

The setting of the inverted output of channel n by this register is reflected at the timing of set or reset of the timer output signal while the timer output is enabled (TOEmn = 1) in the Slave channel output mode (TOMmn = 1). In the master channel output mode (TOMmn = 0), this register setting is invalid.

The TOLm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TOLm register can be set with an 8-bit memory manipulation instruction with TOLmL.

Reset signal generation clears this register to 0000H.

Figure 8-23. Format of Timer Output Level register m (TOLm)

Address: F01BCH, F01BDH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOLm	0	0	0	0	0	0	0	0	TOLm7	TOLm6	TOLm5	TOLm4	TOLm3	TOLm2	TOLm1	0

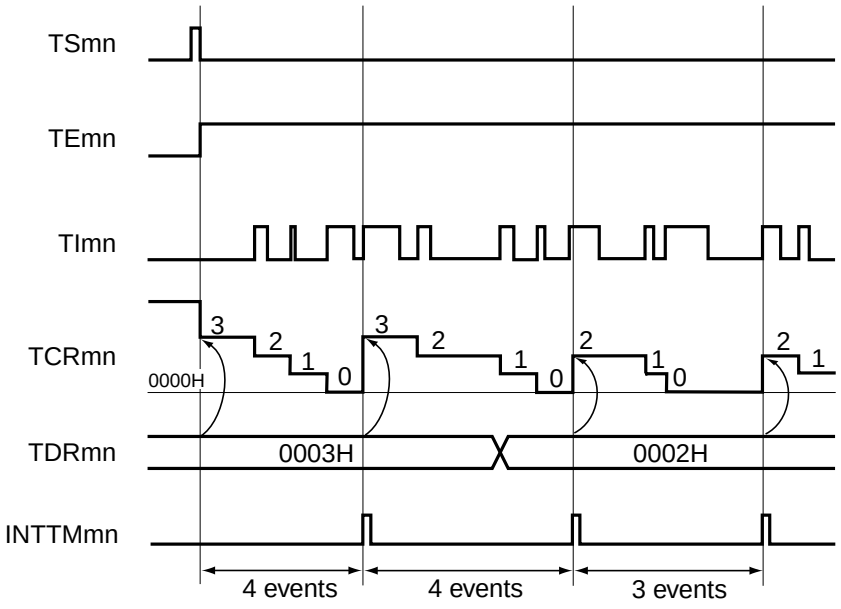
TOLmn	Control of timer output level of channel n
0	Positive logic output (active-high)
1	Negative logic output (active-low)

Caution Be sure to clear bits 15 to 8, and 0 to "0".

Remarks 1. If the value of this register is rewritten during timer operation, the timer output logic is inverted when the timer output signal changes next, instead of immediately after the register value is rewritten.

2. m: Unit number (m = 0), n: Channel number (n = 0 to 7)

Figure 8-50. Example of Basic Timing of Operation as External Event Counter



Remarks 1. m: Unit number (m = 0), n: Channel number (n = 0 to 7)

2. TSmn: Bit n of timer channel start register m (TSm)
TEmn: Bit n of timer channel enable status register m (TEm)
TImn: TImn pin input signal
TCRmn: Timer count register mn (TCRmn)
TDRmn: Timer data register mn (TDRmn)

8.9.3 Operation as multiple PWM output function

By extending the PWM function and using multiple slave channels, many PWM waveforms with different duty values can be output.

For example, when using two slave channels, the period and duty factor of an output pulse can be calculated by the following expressions.

Pulse period = {Set value of TDRmn (master) + 1} × Count clock period
Duty factor 1 [%] = {Set value of TDRmp (slave 1)}/{Set value of TDRmn (master) + 1} × 100
Duty factor 2 [%] = {Set value of TDRmq (slave 2)}/{Set value of TDRmn (master) + 1} × 100

Remark Although the duty factor exceeds 100% if the set value of TDRmp (slave 1) > {set value of TDRmn (master) + 1} or if the {set value of TDRmq (slave 2)} > {set value of TDRmn (master) + 1}, it is summarized into 100% output.

Timer count register mn (TCRmn) of the master channel operates in the interval timer mode and counts the periods.

The TCRmp register of the slave channel 1 operates in one-count mode, counts the duty factor, and outputs a PWM waveform from the TOmp pin. The TCRmp register loads the value of timer data register mp (TDRmp), using INTTMmn of the master channel as a start trigger, and starts counting down. When TCRmp = 0000H, TCRmp outputs INTTMmp and stops counting until the next start trigger (INTTMmn of the master channel) has been input. The output level of TOmp becomes active one count clock after generation of INTTMmn from the master channel, and inactive when TCRmp = 0000H.

In the same way as the TCRmp register of the slave channel 1, the TCRmq register of the slave channel 2 operates in one-count mode, counts the duty factor, and outputs a PWM waveform from the TOmq pin. The TCRmq register loads the value of the TDRmq register, using INTTMmn of the master channel as a start trigger, and starts counting down. When TCRmq = 0000H, the TCRmq register outputs INTTMmq and stops counting until the next start trigger (INTTMmn of the master channel) has been input. The output level of TOmq becomes active one count clock after generation of INTTMmn from the master channel, and inactive when TCRmq = 0000H.

When channel 0 is used as the master channel as above, up to seven types of PWM signals can be output at the same time.

Caution To rewrite both timer data register mn (TDRmn) of the master channel and the TDRmp register of the slave channel 1, write access is necessary at least twice. Since the values of the TDRmn and TDRmp registers are loaded to the TCRmn and TCRmp registers after INTTMmn is generated from the master channel, if rewriting is performed separately before and after generation of INTTMmn from the master channel, the TOmp pin cannot output the expected waveform. To rewrite both the TDRmn register of the master and the TDRmp register of the slave, be sure to rewrite both the registers immediately after INTTMmn is generated from the master channel (This applies also to the TDRmq register of the slave channel 2).

Remark m: Unit number (m = 0), n: Channel number (n = 0, 2, 4)
p: Slave channel number, q: Slave channel number
$n < p < q \leq 7$ (Where p and q are integers greater than n)

9.2.5 Hour counter (RHRCNT)/binary counter 2 (BCNT2)

(1) In calendar count mode:

The RHRCNT counter is used for setting and counting the BCD-coded hour value. It counts carries generated once per hour in the minute counter.
The specifiable time differs according to the setting in the hours mode bit (RCR2.HR24).
When the RCR2.HR24 bit is 0: From 00 to 11 (in BCD)
When the RCR2.HR24 bit is 1: From 00 to 23 (in BCD)
If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, be sure to stop the count operation through the setting of the START bit in RCR2.
The PM bit is only enabled when the RCR2.HR24 bit is 0. Otherwise, the setting in the PM bit has no effect.
To read this counter, follow the procedure in section 9.3.6, Reading 64-Hz counter and time.

Figure 9 - 8 Format of Hour Counter (RHRCNT)

Address: F0587H After reset: Undefined R/W

Symbol	7	6	5	4	3	2	1	0
RHRCNT	0	PM	HR10		HR1			

PM	PM
0	a.m.
1	p.m.
Time Counter Setting for a.m./p.m.	

HR10	10-Hour Count
Counts from 0 to 2 once per carry from the ones place.	

HR1	1-Hour Count
Counts from 0 to 9 once per hour. When a carry is generated, 1 is added to the tens place.	

(2) In binary count mode:

The BCNT2 counter is a readable/writable 32-bit binary counter b23 to b16.
The 32-bit binary counter performs count operation by a carry generating for each second of the 64-Hz counter.
Before writing to this register, be sure to stop the count operation through the setting of the START bit in RCR2.
To read this counter, follow the procedure in section 9.3.6, Reading 64-Hz counter and time.

Figure 9 - 9 Format of Binary Counter 2 (BCNT2)

Address: F0587H After reset: Undefined

Symbol	7	6	5	4	3	2	1	0
BCNT2	BCNT[23:16]							

9.2.6 Day-of-week counter (RWKCNT)/binary counter 3 (BCNT3)

(1) In calendar count mode:

The RWKCNT counter is used for setting and counting in the coded day-of-week value. It counts carries generated once per day in the hour counter.
A value from 0 through 6 can be specified; if a value outside of this range is specified, the RTC does not operate correctly.
Before writing to this register, be sure to stop the count operation through the setting of the START bit in RCR2.
To read this counter, follow the procedure in section 9.3.6, Reading 64-Hz counter and time.

Figure 9 - 10 Format of Day-of-Week Counter (RWKCNT)

Address: F0589H After reset: Undefined R/W

Symbol	7	6	5	4	3	2	1	0
RWKCNT	0	0	0	0	0	DAYW		

DAYW2	DAYW1	DAYW0	Day-of-Week Counting
0	0	0	Sunday
0	0	1	Monday
0	1	0	Tuesday
0	1	1	Wednesday
1	0	0	Thursday
1	0	1	Friday
1	1	0	Saturday
1	1	1	Setting Prohibited

(2) In binary count mode:

The BCNT3 counter is a readable/writable 32-bit binary counter b31 to b24.
The 32-bit binary counter performs count operation by a carry generating for each second of the 64-Hz counter.
Before writing to this register, be sure to stop the count operation through the setting of the START bit in RCR2.
To read this counter, follow the procedure in section 9.3.6, Reading 64-Hz counter and time.

Figure 9 - 11 Format of Binary Counter 3 (BCNT3)

Address: F0589H After reset: Undefined

Symbol	7	6	5	4	3	2	1	0
BCNT3	BCNT[31:24]							

12.4.3.2 When count source ($f_{SX}/2^m$) is selected

After 1 is written to the TSTARTni (n = 0, 1, i = 0, 1) bit in the TRTCRn register, the count is started with the next sub clock (f_{SX}), and then the counter is incremented from 00H to 01H by the next count source ($f_{SX}/2^m$). Likewise, after 0 is written to the TSTARTni bit, the count is stopped with the sub clock (f_{SX}).

However, the first period to count 00H when the timer starts counting is shorter than one cycle of the count source as below, depending on the timing for writing to the TSTARTni bit and the timing of the next count source.

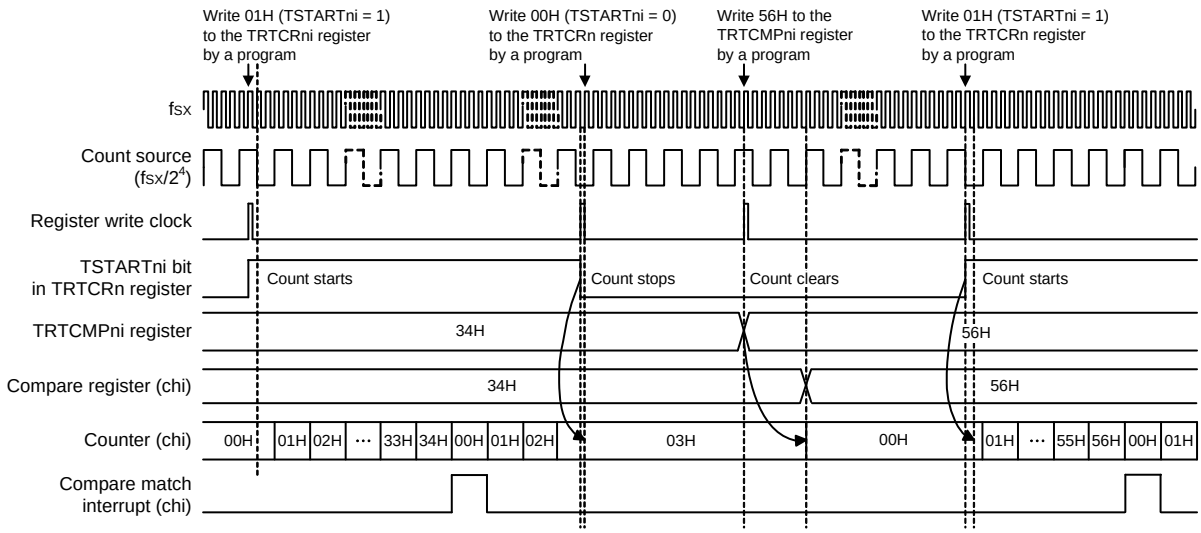
Minimum: One cycle of the sub clock (f_{SX})

Maximum: One cycle of the count source

Figure 12 - 11 shows the timing for starting/stopping count operation, and Figure 12- 12 shows the timing of count stop → compare setting (count clearing) → count start. Figure 12 - 11 and Figure 12 - 12 show the update timing in

8-bit counter mode, but operation is performed at the same timing even in 16-bit counter mode.

Figure 12 - 11 Example of Count Start/Stop Operation ($f_{SX}/2^m$ Selected)

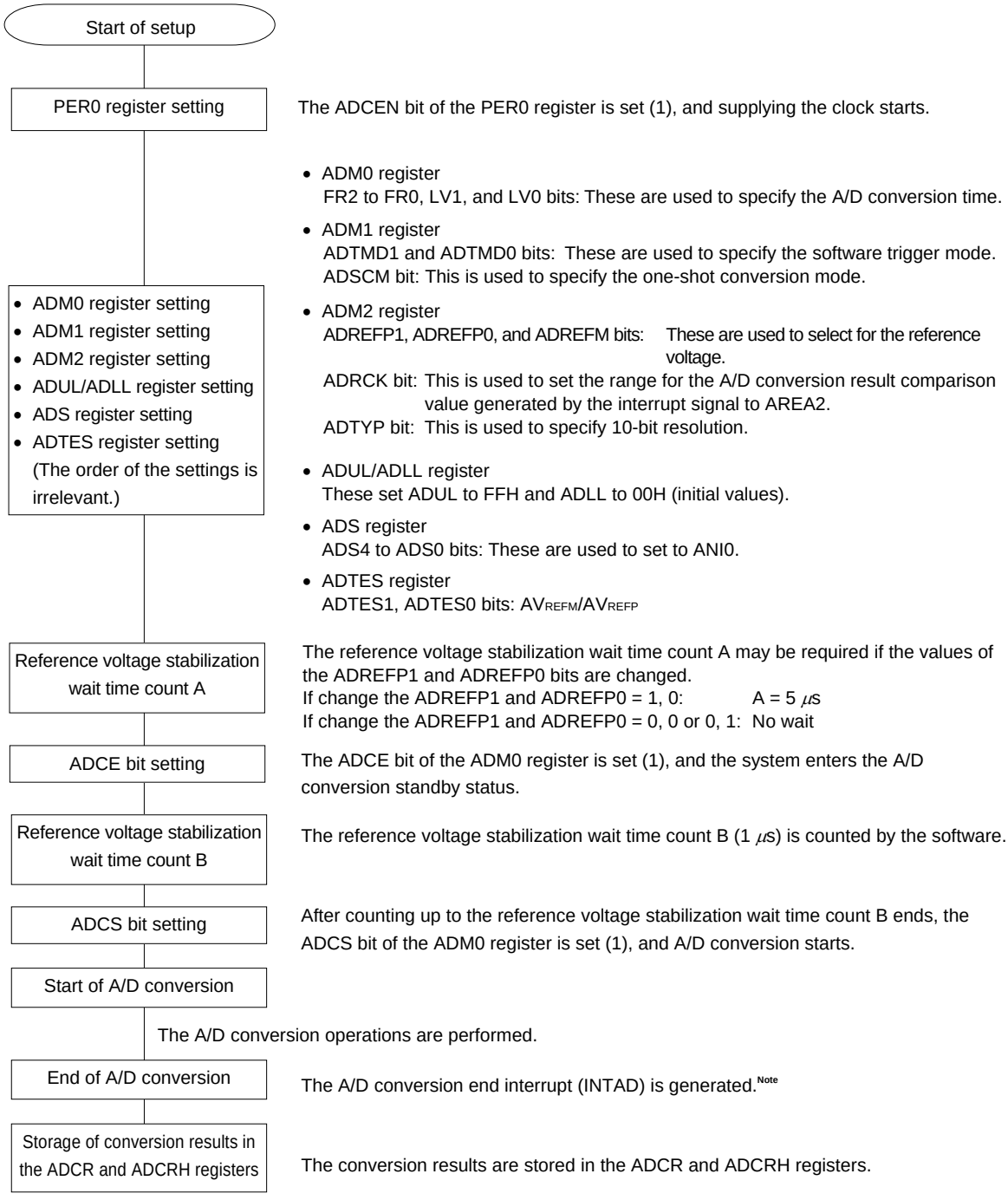


The TCSMDn bit in the TRTCRn register is set to 0 (8-bit counter operation)

Remark n = 0, 1 i = 0, 1

15.7.5 Setting up test mode

Figure 15-34. Setting up Test Mode



Note Depending on the settings of the ADRCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR, ADCRH registers.

Caution For the procedure for testing the A/D converter, see 32.3.8 A/D test function.

Figure 18-50. Example of Contents of Registers for Slave Transmission of 3-Wire Serial I/O (CSI00, CSI10, CSI30) (2/2)

(e) Serial output enable register m (SOEm) … Sets only the bits of the target channel to 1.

<R>

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm														SOEm2		SOEm0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0	0/1

(f) Serial channel start register m (SSm) … Sets only the bits of the target channel to 1.

<R>

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm													SSm3	SSm2	SSm1	SSm0
	0	0	0	0	0	0	0	0	0	0	0	0	×	0/1	×	0/1

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: CSI number (p = 00, 10, 30), mn = 00, 02, 12

2. ☐: Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

(d) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop

(i) When WTIMn = 0 (after restart, does not match address (= not extension code))

▲1: IICSn = 0001×110B
▲2: IICSn = 0001×000B
▲3: IICSn = 00000×10B
△4: IICSn = 00000001B

Remark ▲: Always generated
△: Generated only when SPIEn = 1
×: Don't care

(ii) When WTIMn = 1 (after restart, does not match address (= not extension code))

▲1: IICSn = 0001×110B
▲2: IICSn = 0001××00B
▲3: IICSn = 00000×10B
△4: IICSn = 00000001B

Remark ▲: Always generated
△: Generated only when SPIEn = 1
×: Don't care

Remark n = 0

22.4.2 Normal mode

One to 256 bytes of data are transferred by one activation during 8-bit transfer and 2 to 512 bytes during 16-bit transfer. The number of transfers can be 1 to 256 times. When the data transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 is performed, the DTC generates an interrupt request corresponding to the activation source to the interrupt controller during DTC operation, and sets the corresponding bit among bits DTCENi0 to DTCENi7 (i = 0 to 4) in the DTCENi register to 0 (activation disabled).

Table 22-7 shows register functions in normal mode. Figure 22-15 shows data transfers in normal mode.

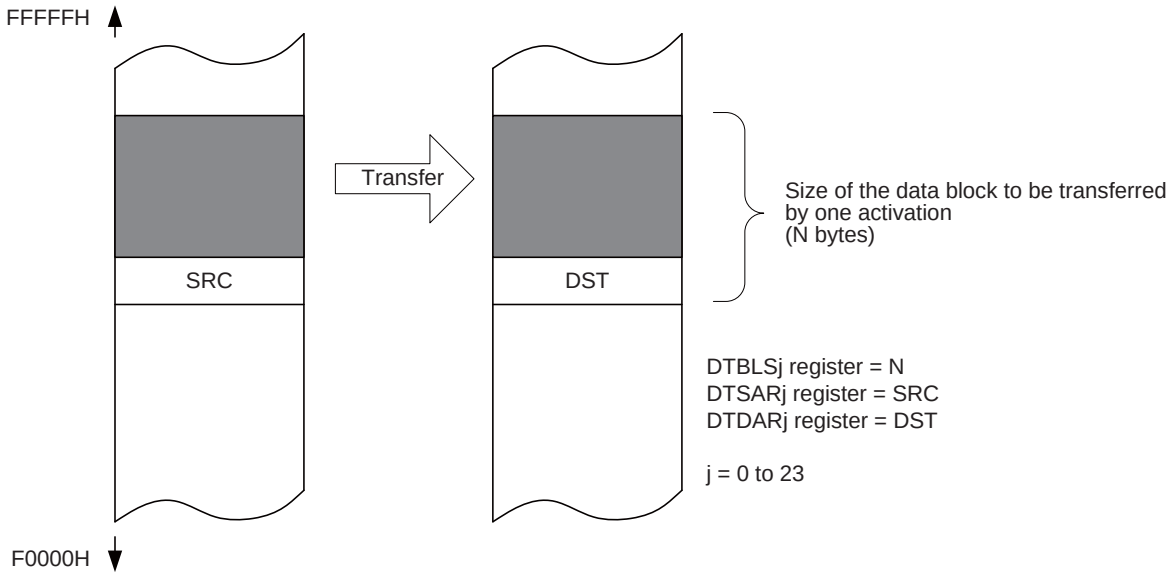
Table 22-7. Register Functions in Normal Mode

Register Name	Symbol	Function
DTC block size register j	DTBLSj	Size of the data block to be transferred by one activation
DTC transfer count register j	DTCCTj	Number of data transfers
DTC transfer count reload register j	DTRLDj	Not used[Note]
DTC source address register j	DTSARj	Data transfer source address
DTC destination address register j	DTDARj	Data transfer destination address

Note Initialize this register to 00H when parity error resets are enabled (RPERDIS = 0) using the RAM parity error detection function.

Remark j = 0 to 23

Figure 22-15. Data Transfers in Normal Mode



DTCCR Register Setting				Source Address Control	Destination Address Control	Source Address After Transfer	Destination Address After Transfer
DAMOD	SAMOD	RPTSEL	MODE				
0	0	X	0	Fixed	Fixed	SRC	DST
0	1	X	0	Incremented	Fixed	SRC + N	DST
1	0	X	0	Fixed	Incremented	SRC	DST + N
1	1	X	0	Incremented	Incremented	SRC + N	DST + N

X: 0 or 1

Table 24-1. Interrupt Source List (3/4)

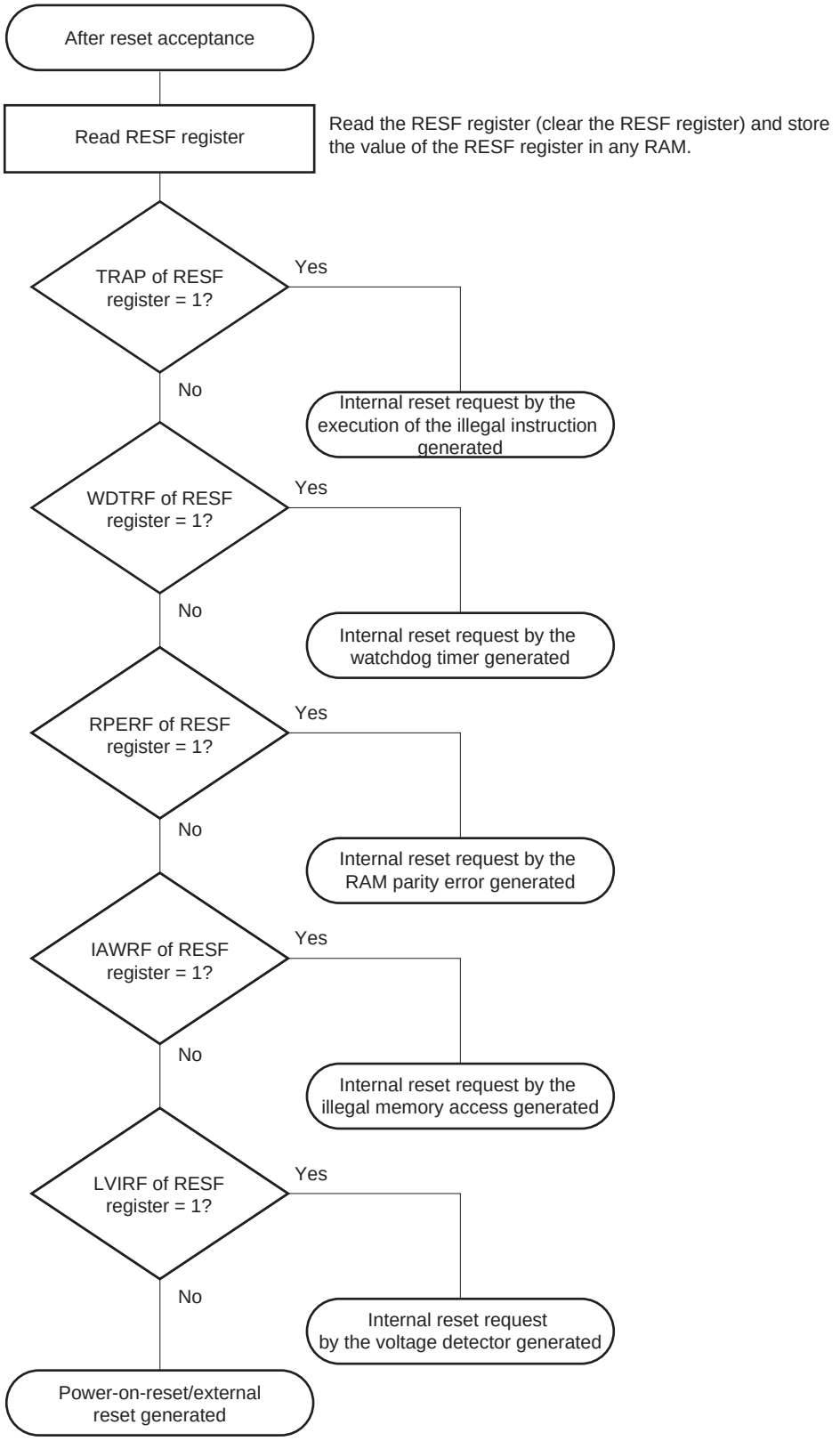
Interrupt Type Maskable	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2	100-pin	80-pin	64-pin
		Name	Trigger						
Maskable	44	INTSRE3	UART3 reception communication error occurrence	Internal	005CH	(A)	√	-	-
	45	INTMACLOF	Multiply-accumulation overflow/underflow interrupt		005EH		√	√	√
	46	INTOSDC	Oscillation stop detection		0060H		√	√	√
	47	INTFL	Reserved Note 3		0062H		√	√	√
	48	INTDSADZC 0	Zero-cross detection 0 of 24-bit ΔΣ-type A/D converter		0064H		√	√	√
	49	INTDSADZC 1	Zero-cross detection 1 of 24-bit ΔΣ-type A/D converter		0066H		√	√	√
	50	INTIT10	8-bit interval timer channel 10/channel 1 (when cascade) compare match detection		0068H		√	√	√
	51	INTIT11	8-bit interval timer channel 11 compare match detection		006AH		√	√	√
	52	INTLVDVDD	Voltage detection of V_{DD} pin		006CH		√	√	√
	53	INTLVDVBA T	Voltage detection of VBAT pin		006EH		√	√	√
	54	INTLVDVRT C	Voltage detection of VRTC pin		0070H		√	√	√
	55	INTLVDEXL VD	Voltage detection of EXLVD pin		0072H		√	√	√

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 42 indicates the lowest priority.

2. Basic configuration types (A) to (C) correspond to (A) to (C) in Figure 24-1.

3. Be used at the flash self-programming library or the data flash library.

Figure 27-5. Example of Procedure for Checking Reset Source



30.2 Registers

Table 30-3 lists the registers used for battery backup.

Table 30-3. Registers

Register Name	Symbol
Battery backup power switching control register 0	BUPCTL0
Battery backup power switching control register 1	BUPCTL1
Global digital input disable register	GDIDIS

30.2.1 Battery backup power switching control register 0 (BUPCTL0)

<R> The BUPCTL0 register is used to select the power supply pin.

The BUPCTL0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

VBATEN (bit 7) and VBATSEL (bit 0) are cleared to 0 only when a power-on reset is generated. Other bits are cleared to 0 when a reset signal is generated.

Figure 30-2. Format of Battery Backup Power Switching Control Register 0 (BUPCTL0) (1/2)

Address: F0330H After reset: 00H[Note 1] R/W

<R>

Symbol	<7>	6	5	4	<3>	2	1	<0>
BUPCTL0	VBATEN	0	0	0	VBATCMPM	0	0	VBATSEL

<R>

VBATEN[Notes 2, 4]	Battery backup function control
0	Battery backup function stops[Note 3]
1	Battery backup function operates

Notes 1. VBATEN (bit 7) and VBATSEL (bit 0) are cleared to 0 only when a power-on reset is generated.

2. To set the VBATEN bit to 1, write 0 and then write 1 to this bit. If a value is written to an SFR other than BUPCTL0 after 0 has been written, the VBATEN bit cannot be set to 1.
To set the VBATEN bit to 0, write 1 and then write 0 to this bit. If a value is written to an SFR other than BUPCTL0 after 1 has been written, the VBATEN bit cannot be set to 0.

3. By setting the battery backup function stop (VBATEN is cleared) when the internal power supply is set to the VBAT supply, the power supply can be switched from the V_{DD} pin.
To forcibly shut down the power supply from the VBAT pin when the V_{DD} voltage is not supplied, clear the VBATEN bit to 0. The power is not supplied (power-on-reset status) since the power supply from V_{DD} pin is forcibly switched. After that, this status is recovered by the V_{DD} power supply.

<R> **4.** The minimum operating voltage of this product varies according to the VBATEN setting value.
When VBATEN = 0, the minimum operating voltage is 1.7 V.
When VBATEN = 1, the minimum operating voltage is 1.9 V.

41.2.2 On-chip oscillator characteristics

(T_A = –40 to +85°C, 1.7 V ≤ V_{DD}[Note 3] ≤ 5.5 V, V_{SS} = 0 V)

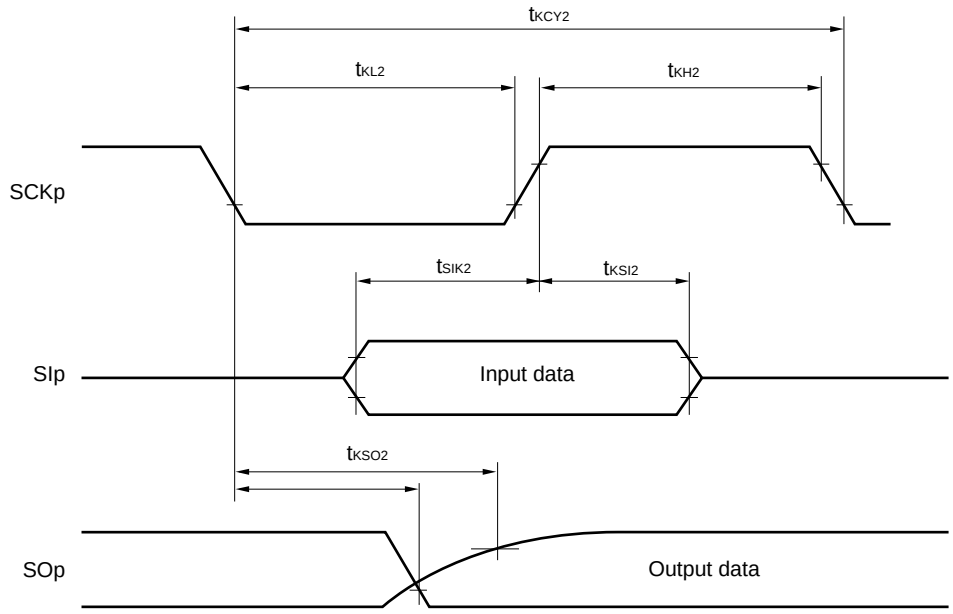
Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency[Notes 1, 2]	f_{IH}			1.5		24	MHz
High-speed on-chip oscillator clock frequency accuracy		–20 to +85°C	1.9 V ≤ V_{DD}[Note 3] ≤ 5.5 V	–1.0		+1.0	%
			1.7 V ≤ V_{DD}[Note 3] ≤ 1.9 V	–5.0		+5.0	%
		–40 to –20°C	1.9 V ≤ V_{DD}[Note 3] ≤ 5.5 V	–1.5		+1.5	%
			1.7 V ≤ V_{DD}[Note 3] ≤ 1.9 V	–5.5		+5.5	%
<R> Middle-speed on-chip oscillator clock frequency[Note 2]	f_{IM}			1		4	MHz
<R> Middle-speed on-chip oscillator clock frequency accuracy		1.9 V ≤ V_{DD}[Note 3] ≤ 5.5 V		–12		+12	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				–15		+15	%

Notes 1. The high-speed on-chip oscillator frequency is selected by using bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of the HOCODIV register.

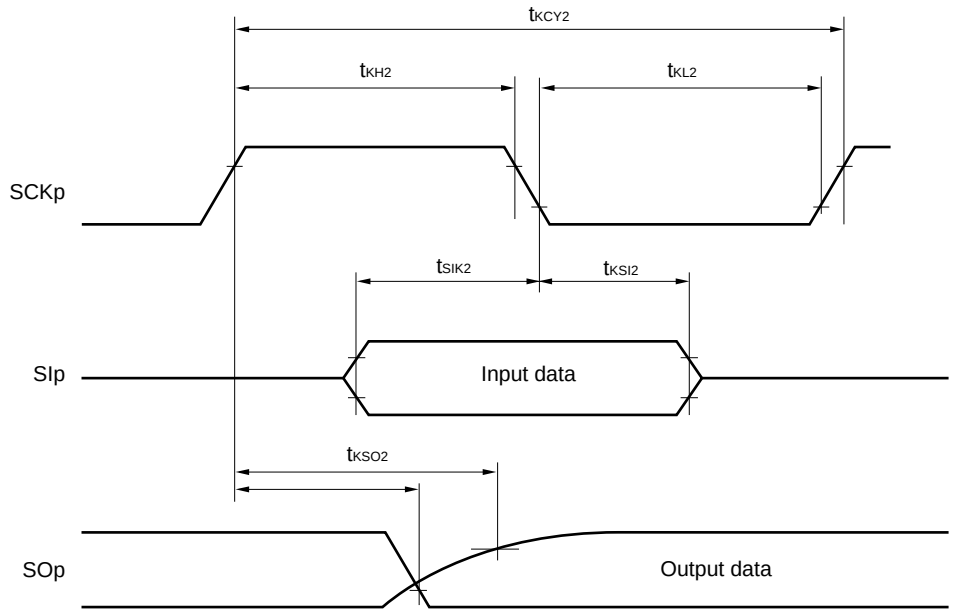
2. This indicates the oscillator characteristics only. See **41.4 AC Characteristics** for the instruction execution time.

3. Either V_{DD} or VBAT is selected by the battery backup function.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remark p: CSI number (p = 00, 10, 30), m: Unit number, n: Channel number (mn = 00, 02, 12),
g: PIM and POM number (g = 0, 1, 8)