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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, IrDA, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 5.5V
Data Converters	A/D 4x10b, 3x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10nmgdfb-30

Set in each port I/O, buffer, pull-up resistor is also valid for alternate functions.

2.1.1 64-pin products

(1/2)

Function Name	Pin Type	I/O	After Reset Released	Alternate Function	Function
P05	8-5-10	I/O	Input port	SCK00/SCL00/TI04/ TO04/INTP3	Port 0. 3-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software setting at input port. Input of P05 and P06 can be set to TTL input buffer. Output of P05 to P07 can be set to N-ch open-drain output (V_{DD} tolerance).
P06				SI00/RxD0/TI03/TO03/ SDA00/INTP4/TOOLRxD	
P07	7-5-10			SO00/TxD0/TI02/TO02/ INTP2/TOOLTxD	
P10	7-5-4	I/O	Digital input invalid[Note 1]	SEG4	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software setting at input port. Input of P12, P13, P15, and P16 can be set to TTL input buffer. Output of P12 to P17 can be set to N-ch open-drain output (V_{DD} tolerance). Can be set to LCD output[Note 2].
P11				SEG5	
P12	8-5-10			SEG6/SCK10/SCL10	
P13				SEG7/INTP6/SI10/RxD1/ SDA10/	
P14	7-5-10			SEG8/SO10/TxD1	
P15	8-5-10			SEG9/(SCK00)/(SCL00)	
P16				SEG10/INTP7/(SI00)/ (RxD0)/(SDA00)	
P17	7-5-10			SEG11/(SO00)/(TxD0)	
P20	4-3-3	I/O	Analog input port	AV_{REFP}/ANI0	Port 2. 4-bit I/O port. Input/output can be specified in 1-bit units. Can be set to analog input[Note 3].
P21				AV_{REFM}/ANI1	
P22	4-17-1			ANI2/EXLVD	
P23	4-3-3			ANI3	
P30	8-5-10	I/O	Digital input invalid[Note 1]	SEG24/INTP5/TI07/ TO07/RxD2/IrRxD	Port3. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software setting at input port. Can be set to LCD output[Note 2]. Input of P30 can be set to TTL input buffer. Output of P31 can be set to N-ch open drain output (V_{DD} tolerance).
P31	7-5-10			SEG25/TI06/TO06/TxD2/ IrTxD	

Notes 1. "Digital input invalid" refers to the state in which all the digital outputs, digital inputs, and LCD outputs are disabled.

2. Digital or LCD for each pin can be selected with the port mode register x (PMx) and the LCD port function register x (PFSEGx) (can be set in 1-bit unit).

3. Setting digital or analog to each pin can be done in A/D port configuration register (ADPC).

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR0). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR0)**.

5.3 Initial Setting of Flash Operation Modes

The option byte (000C2H) is used to set the initial state of flash operation mode and the high-speed on-chip oscillator after a reset is released.

Set an appropriate flash operation mode according to the V_{DD} voltage and the high-speed on-chip oscillator frequency at a reset release.

<R> When a reset is released, the value of CMODE1 and CMODE0 is updated in MODE1 and MODE0 in the flash operation mode select register (FLMODE) and the value of FRQSEL2 to FRQSEL0 is updated in the high-speed on-chip oscillator frequency select register (HOCODIV).

Figure 5 - 5 Format of User option byte (000C2H)

Address: 000C2H

Symbol	7	6	5	4	3	2	1	0
	CMODE1	CMODE0	1	0	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0

CMODE1	CMODE0	Selection of flash operation mode after reset release
0	0	LV (low-voltage main) mode
1	0	LS (low-speed main) mode
1	1	HS (high-speed main) mode
Other than above		Setting prohibited

FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0	High-speed on-chip oscillator frequency
0	0	0	0	24 MHz
1	0	0	1	16 MHz
0	0	0	1	12 MHz
1	0	1	0	8 MHz
0	0	1	0	6 MHz
1	0	1	1	4 MHz
0	0	1	1	3 MHz
1	1	0	0	2 MHz
0	1	0	0	1.5 MHz
1	1	0	1	1 MHz
Other than above				Setting prohibited

9.3.9.1 Automatic adjustment

Enable automatic adjustment by setting the RCR2.AADJE bit to 1.
Automatic adjustment is the addition or subtraction of the value counted by the prescaler to or from the value in the RADJ register every time the adjustment period selected by the RCR2.AADJE bit elapses.
Examples are shown below.

[Example 1] Sub-clock running at 32.769 kHz
Adjustment procedure:
When the sub-clock is running at 32.769 kHz, 1 second elapses every 32,769 clock cycles. The RTC is meant to run at 32,768 clock cycles, so the clock runs fast by one clock cycle every second. The time on the clock is fast by 60 clock cycles per minute, so adjustment can take the form of setting the clock back by 60 cycles every minute.

Register settings: (when RCR2.CNTMD = 0)

- RCR2.AADJP = 0 (adjustment every minute)
- RADJ.PMADJ[1:0] = 10b (adjustment is performed by the subtraction from the prescaler.)
- RADJ.ADJ[5:0] = 60 (3Ch)

[Example 2] Sub-clock running at 32.766 kHz
Adjustment procedure:
When the sub-clock is running at 32.766 kHz, 1 second elapses every 32,766 clock cycles. The RTC is meant to run at 32,768 clock cycles, so the clock runs slow by two clock cycles every second. The time on the clock is slow by 20 clock cycles every 10 seconds, so adjustment can take the form of setting the clock forward by 20 cycles every 10 seconds.

Register settings: (when RCR2.CNTMD = 0)

- RCR2.AADJP = 1 (adjustment every 10 seconds)
- RADJ.PMADJ[1:0] = 01b (adjustment is performed by the addition to the prescaler.)
- RADJ.ADJ[5:0] = 20 (14h)

[Example 3] Sub-clock running at 32.764 kHz
Adjustment procedure:
At 32.764 kHz, 1 second elapses on 32,764 clock cycles. Since the RTC operates for 32,768 clock cycles as 1 second, the clock is delayed for four clock cycles per second. In 8 seconds, the delay is 32 clock cycles, so correction can be made by proceeding the clock for 32 clock cycles every 8 seconds.

Register settings when the RCR2.CNTMD bit is 1

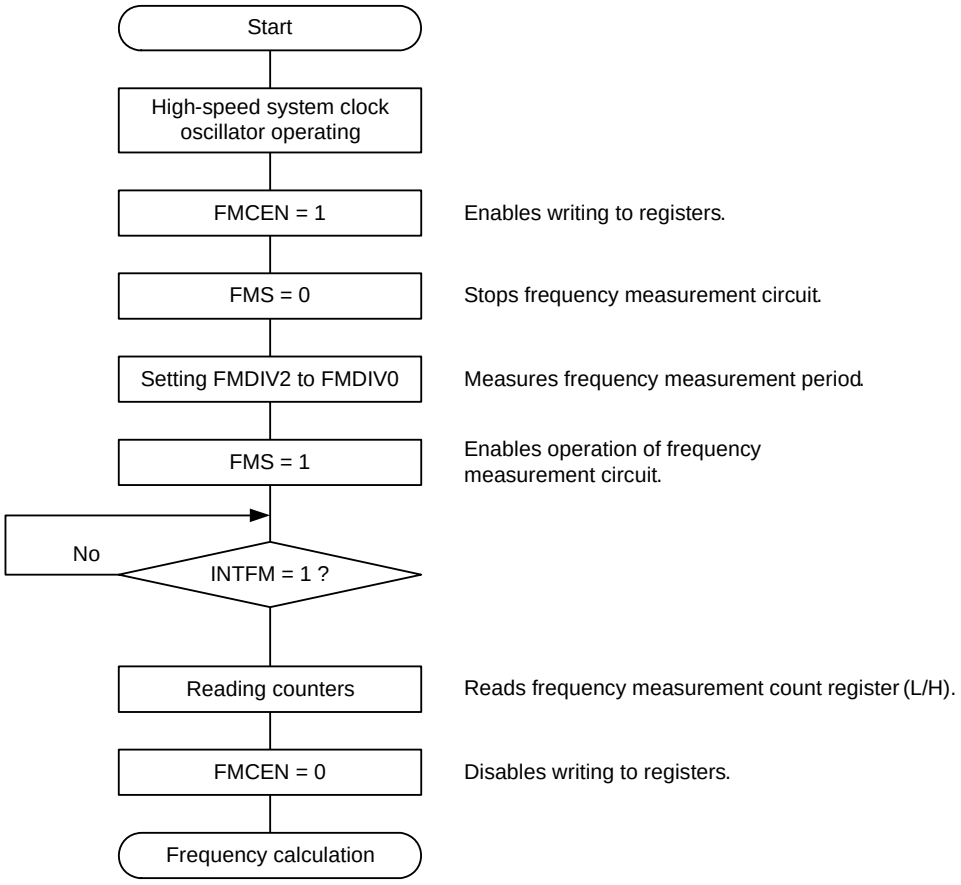
- RCR2.AADJP = 1 (adjustment every 8 seconds)
- RADJ.PMADJ[1:0] = 01b (adjustment is performed by the addition to the prescaler.)
- RADJ.ADJ[5:0] = 32 (20h)

10.4 Frequency Measurement Circuit Operation

10.4.1 Setting frequency measurement circuit

Set frequency measurement circuit after setting 0 to FMS first.

Figure 10 - 9 Procedure for Setting Frequency Measurement Circuit Using Reference Clock



Caution After the frequency measurement count register (L/H) is read, be sure to set FMCEN to 0.

The f_{SX} or f_{IL} oscillation frequency is calculated by using the following expression.

$$f_{SX} \text{ or } f_{IL} \text{ oscillation frequency} = \frac{\text{Reference clock frequency [Hz]} \times \text{operation trigger division ratio}}{\text{Frequency measurement count register value (FMCR)}} \text{ [Hz]}$$

For example, when the frequency is measured under the following conditions

- Count clock frequency: f_{MX} = 10 MHz
- Frequency measurement period setting register: FMDIV2 to FMDIV0 = 111B (operation trigger division ratio: 2^{15})

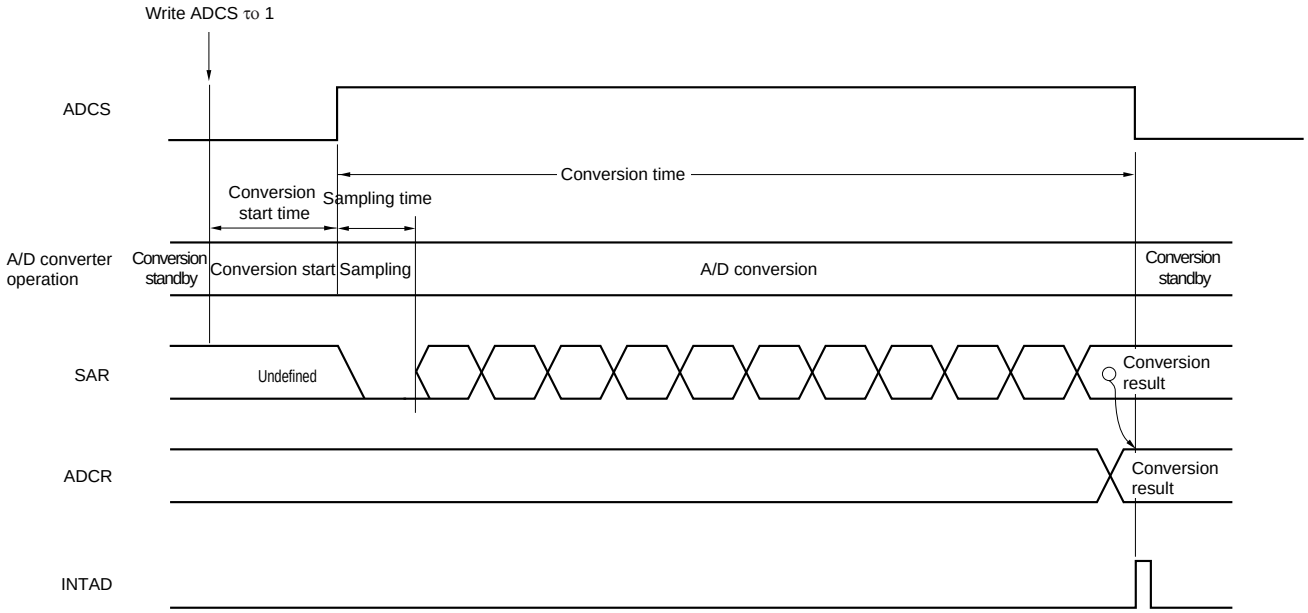
and the measurement result is as follows,

- Frequency measurement count register: FMCR = 10000160D

the f_{SX} or f_{IL} oscillation frequency is obtained as below.

$$f_{SX} \text{ or } f_{IL} \text{ oscillation frequency} = \frac{(10 \times 10^6) \times 2^{15}}{10000160} = 32767.47572 \text{ [Hz]}$$

Figure 15-16. Conversion Operation of A/D Converter (Software Trigger Mode)



In one-shot conversion mode, the ADCS bit is automatically cleared to 0 after completion of A/D conversion.

In sequential conversion mode, A/D conversion operations proceed continuously until the software clears bit 7 (ADCS) of the A/D converter mode register 0 (ADM0) to 0.

When the value of the analog input channel specification register (ADS) is rewritten or overwritten during conversion, the current A/D conversion is interrupted, and A/D conversion is performed on the analog input newly specified in the ADS register. The partially converted data is discarded.

Reset signal generation clears the A/D conversion result register (ADCR, ADCRH) to 0000H or 00H.

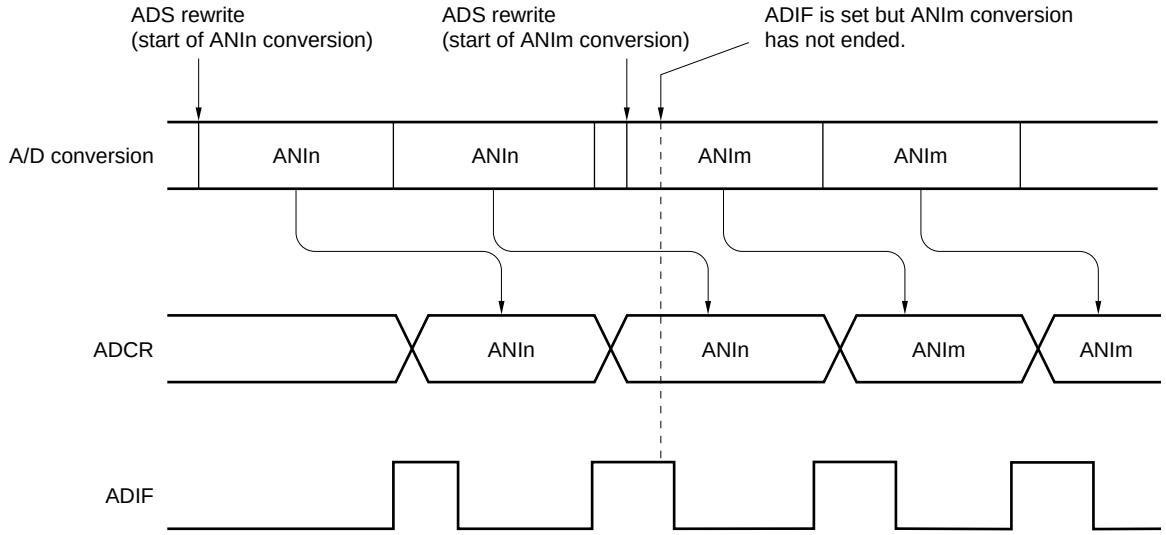
(7) Interrupt request flag (ADIF)

The interrupt request flag (ADIF) is not cleared even if the analog input channel specification register (ADS) is changed.

Therefore, if an analog input pin is changed during A/D conversion, the A/D conversion result and ADIF flag for the pre-change analog input may be set just before the ADS register rewrite. Caution is therefore required since, at this time, when ADIF flag is read immediately after the ADS register rewrite, ADIF flag is set despite the fact A/D conversion for the post-change analog input has not ended.

When A/D conversion is stopped and then resumed, clear ADIF flag before the A/D conversion operation is resumed.

Figure 15-46. Timing of A/D Conversion End Interrupt Request Generation



(8) Conversion results just after A/D conversion start

While in the software trigger mode or hardware trigger no-wait mode, the first A/D conversion value immediately after A/D conversion starts may not fall within the rating range if the ADCS bit is set to 1 within 1 μs after the ADCE bit was set to 1. Take measures such as polling the A/D conversion end interrupt request (INTAD) and removing the first conversion result.

(9) A/D conversion result register (ADCR, ADCRH) read operation

When a write operation is performed to A/D converter mode register 0 (ADM0), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of the ADCR and ADCRH registers may become undefined. Read the conversion result following conversion completion before writing to the ADM0, ADS, or ADPC register. Using a timing other than the above may cause an incorrect conversion result to be read.

18.3.3 Serial mode register mn (SMRmn)

The SMRmn register is a register that sets an operation mode of channel n. It is also used to select an operation clock (f_{MCK}), specify whether the serial clock (f_{SCK}) may be input or not, set a start trigger, an operation mode (CSI, UART, or simplified I^2C), and an interrupt source. This register is also used to invert the level of the receive data only in the UART mode.

Rewriting the SMRmn register is prohibited when the register is in operation (when SEmn = 1). However, the MDmn0 bit can be rewritten during operation.

The SMRmn register can be set by a 16-bit memory manipulation instruction.

Reset signal generation sets the SMRmn register to 0020H.

Figure 18-7. Format of Serial Mode Register mn (SMRmn) (1/2)

Address: F0110H, F0111H (SMR00) to F0116H, F0117H (SMR03), F0150H, F0151H (SMR10) to F0156H, F0157H (SMR13) After reset: 0020H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKSmn	CCSmn	0	0	0	0	0	STSmn[Note]	0	SISmn0[Note]	1	0	0	MDmn2	MDmn1	MDmn0

CKSmn	Selection of operation clock (f_{MCK}) of channel n
0	Operation clock CKm0 set by the SPSm register
1	Operation clock CKm1 set by the SPSm register
Operation clock (f_{MCK}) is used by the edge detector. In addition, depending on the setting of the CCSmn bit and the higher 7 bits of the SDRmn register, a transfer clock (f_{TCLK}) is generated.	

CCSmn	Selection of transfer clock (f_{TCLK}) of channel n
0	Divided operation clock f_{MCK} specified by the CKSmn bit
1	Clock input f_{SCK} from the SCKp pin (slave transfer in CSI mode)
Transfer clock f_{TCLK} is used for the shift register, communication controller, output controller, interrupt controller, and error controller. When CCSmn = 0, the division ratio of operation clock (f_{MCK}) is set by the higher 7 bits of the SDRmn register.	

STSmn	Selection of start trigger source
0	Only software trigger is valid (selected for CSI, UART transmission, and simplified I^2C).
1	Valid edge of the RxDq pin (selected for UART reception)
Transfer is started when the above source is satisfied after 1 is set to the SSm register.	

Note The SMR01, SMR03, SMR11, and SMR13 registers only.

Caution Be sure to clear bits 13 to 9, 7, 4, and 3 (or bits 13 to 6, 4, and 3 for the SMR00, SMR02, SMR10, or SMR12 register) to "0". Be sure to set bit 5 to "1".

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 10, 30), q: UART number (q = 0 to 3), r: IIC number (r = 00, 10, 30), mn = 00 to 03, 10 to 13

(2) When communication reservation function is disabled (bit 0 (IICRSVn) of IICA flag register n (IICFn) = 1)

When bit 1 (STTn) of IICA control register n0 (IICCTLn0) is set to 1 when the bus is not used in a communication during bus communication, this request is rejected and a start condition is not generated. The following two statuses are included in the status where bus is not used.

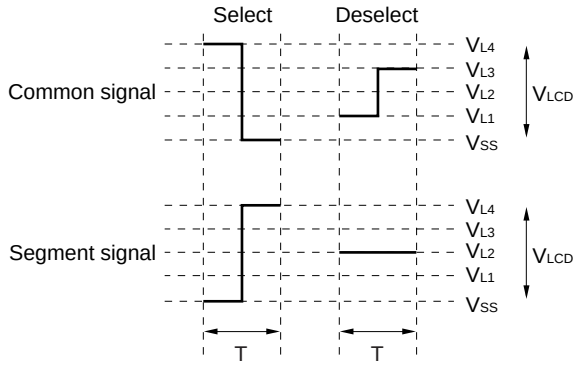
- When arbitration results in neither master nor slave operation
- When an extension code is received and slave operation is disabled (ACK is not returned and the bus was released by setting bit 6 (LRELn) of the IICCTLn0 register to 1 and saving communication)

To confirm whether the start condition was generated or request was rejected, check STCFn (bit 7 of the IICFn register). It takes up to 5 clocks of f_{MCK} until the STCFn bit is set to 1 after setting STTn = 1. Therefore, secure the time by software.

Remark n = 0

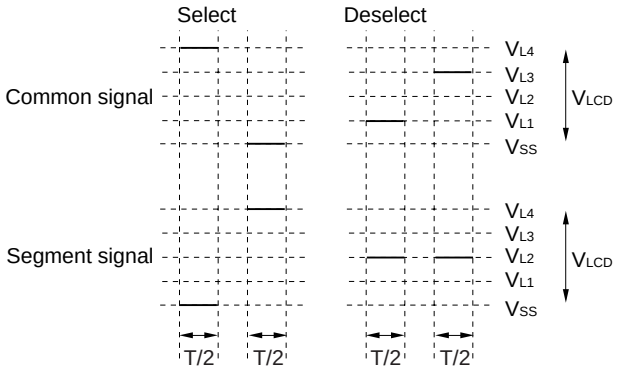
Figure 21-24. Voltages and Phases of Common and Segment Signals (3/3)

(e) 1/4 bias method (waveform A)



T: One LCD clock period

(f) 1/4 bias method (waveform B)



T: One LCD clock period

21.10.3 Three-time-slice display example

Figure 21-32 shows how the 8-digit LCD panel having the display pattern shown in Figure 21-31 is connected to the segment signals (SEG0 to SEG23) and the common signals (COM0 to COM2). This example displays data “123456.78” in the LCD panel. The contents of the display data register (addresses F0400H to F0417H) correspond to this display.

The following description focuses on numeral “6.” (6.) displayed in the third digit. To display “6.” in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG6 to SEG8 pins according to Table 21-16 at the timing of the common signals COM0 to COM2; see Figure 21-31 for the relationship between the segment signals and LCD segments.

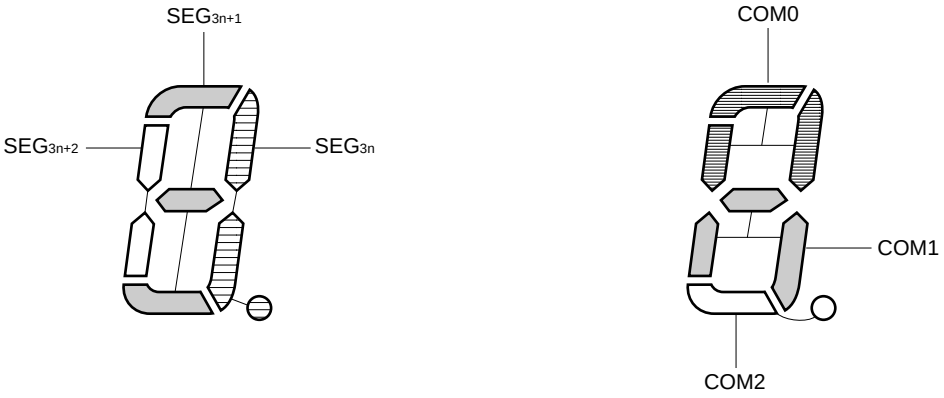
Table 21-16. Select and Deselect Voltages (COM0 to COM2)

Segment / Common	SEG6	SEG7	SEG8
COM0	Deselect	Select	Select
COM1	Select	Select	Select
COM2	Select	Select	–

According to Table 21-16, it is determined that the display data register location (F0406H) that corresponds to SEG6 must contain x110.

Figures 21-33 and 21-34 show examples of LCD drive waveforms between the SEG6 signal and each common signal in the 1/2 and 1/3 bias methods, respectively. When the select voltage is applied to SEG6 at the timing of COM1 or COM2, an alternate rectangle waveform, $+V_{LCD}/-V_{LCD}$, is generated to turn on the corresponding LCD segment.

Figure 21-31. Three-Time-Slice LCD Display Pattern and Electrode Connections



Remark 100-pin products: n = 0 to 13

22.4.2 Normal mode

One to 256 bytes of data are transferred by one activation during 8-bit transfer and 2 to 512 bytes during 16-bit transfer. The number of transfers can be 1 to 256 times. When the data transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 is performed, the DTC generates an interrupt request corresponding to the activation source to the interrupt controller during DTC operation, and sets the corresponding bit among bits DTCENi0 to DTCENi7 (i = 0 to 4) in the DTCENi register to 0 (activation disabled).

Table 22-7 shows register functions in normal mode. Figure 22-15 shows data transfers in normal mode.

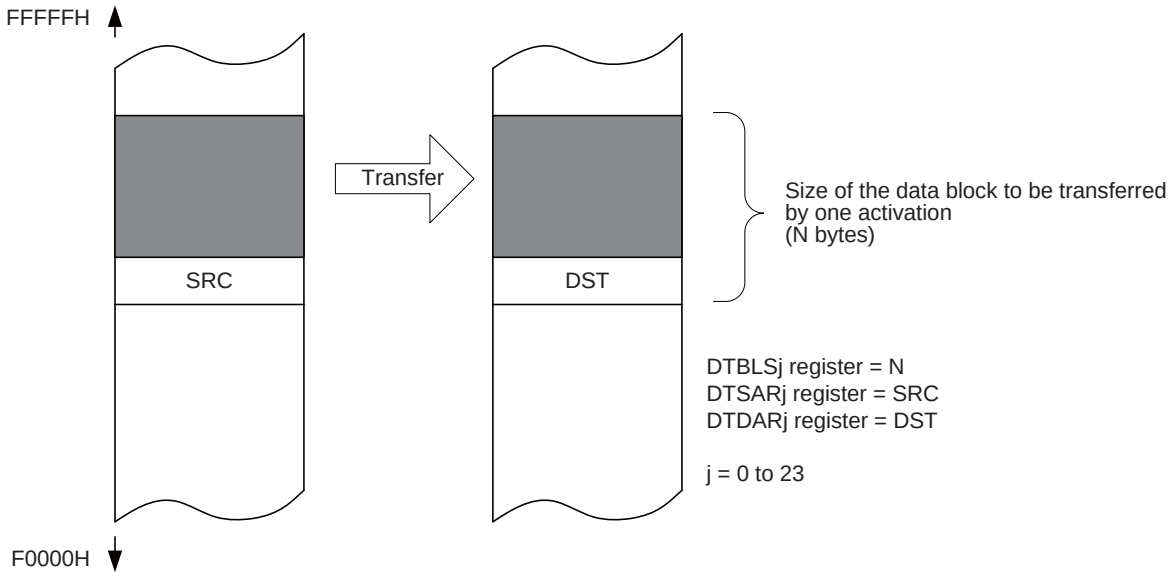
Table 22-7. Register Functions in Normal Mode

Register Name	Symbol	Function
DTC block size register j	DTBLSj	Size of the data block to be transferred by one activation
DTC transfer count register j	DTCCTj	Number of data transfers
DTC transfer count reload register j	DTRLDj	Not used[Note]
DTC source address register j	DTSARj	Data transfer source address
DTC destination address register j	DTDARj	Data transfer destination address

Note Initialize this register to 00H when parity error resets are enabled (RPERDIS = 0) using the RAM parity error detection function.

Remark j = 0 to 23

Figure 22-15. Data Transfers in Normal Mode



DTCCR Register Setting				Source Address Control	Destination Address Control	Source Address After Transfer	Destination Address After Transfer
DAMOD	SAMOD	RPTSEL	MODE				
0	0	X	0	Fixed	Fixed	SRC	DST
0	1	X	0	Incremented	Fixed	SRC + N	DST
1	0	X	0	Fixed	Incremented	SRC	DST + N
1	1	X	0	Incremented	Incremented	SRC + N	DST + N

X: 0 or 1

CHAPTER 23 EVENT LINK CONTROLLER (ELC)

23.1 Functions of ELC

The event link controller (ELC) mutually connects (links) events output from each peripheral function. By linking events, it becomes possible to coordinate operation between peripheral functions directly without going through the CPU.

The ELC has the following functions.

- Capable of directly linking event signals from 22 types of peripheral functions to specified peripheral functions
- Event signals can be used as activation sources for operating any one of five types of peripheral functions

23.2 Configuration of ELC

Figure 23 - 1 shows the ELC Block Diagram.

Figure 23 - 1 ELC Block Diagram

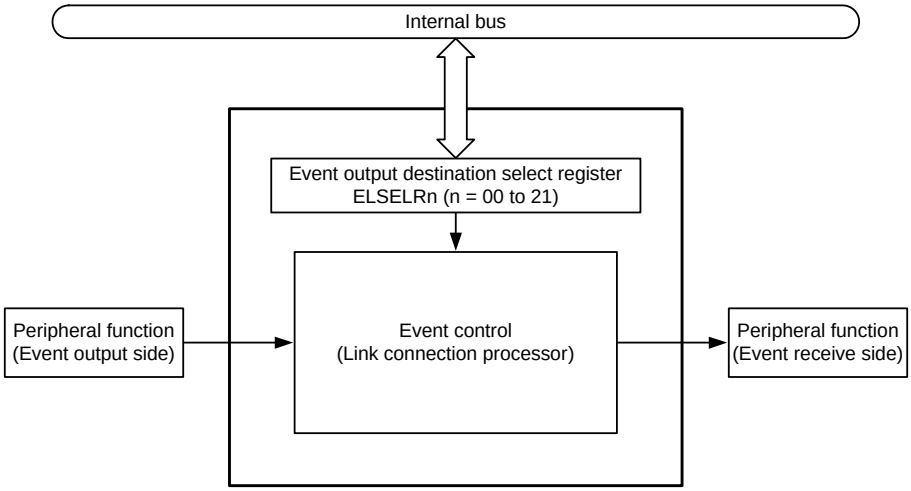


Table 24-1. Interrupt Source List (2/4)

	Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2	100-pin	80-pin	64-pin
			Name	Trigger						
<R>	Maskable	20	INTTM00	End of timer channel 00 count or capture	Internal	002CH	(A)	√	√	√
		22	INTFM	End of frequency measurement		0030H		√	√	√
		23	INTTM01	End of timer channel 01 count or capture (at 16-bit/lower 8-bit timer operation)		0032H		√	√	√
		24	INTTM02	End of timer channel 02 count or capture		0034H		√	√	√
		25	INTTM03	End of timer channel 03 count or capture (at 16-bit/lower 8-bit timer operation)		0036H		√	√	√
		26	INTAD	End of A/D conversion		0038H		√	√	√
		27	INTRTCALM	Alarm match detection of real-time clock		003AH		√	√	√
			INTRTCPRD	Fixed-cycle signal of real-time clock				√	√	√
<R>		28	INTIT	Interval signal of 12-bit interval timer detection		003CH		√	√	√
		29	INTKR	Key return signal detection	External	003EH	(B)	√	√	√
		30	INTST3/ INTCSI30/ INTIIC30	UART3 transmission transfer end or buffer empty interrupt/CSI30 transfer end or buffer empty interrupt/IIC30 transfer end	Internal	0040H	(A)	√	-	-
		31	INTSR3	UART3 reception transfer end		0042H		√	-	-
		32	INTDSAD	End of ΔΣ A/D conversion		0044H		√	√	√
		33	INTTM04	End of timer channel 04 count or capture		0046H		√	√	√
		34	INTTM05	End of timer channel 05 count or capture		0048H		√	√	√
		35	INTP6	Pin input edge detection	External	004AH	(B)	√	√	√
		36	INTP7			004CH		√	√	√
<R>		37	INTRTCIC0 Note 3	Tamper detection of RTCIC0 pin		004EH		√	√	-
<R>		38	INTRTCIC1 Note 3	Tamper detection of RTCIC1 pin		0050H		√	√	-
<R>		39	INTRTCIC2 Note 3	Tamper detection of RTCIC2 pin		0052H		√	√	-
		40	INTTM06	End of timer channel 06 count or capture	Internal	0054H	(A)	√	√	√
		41	INTTM07	End of timer channel 07 count or capture		0056H		√	√	√
		42	INTIT00	8-bit interval timer channel 00/channel 0 (when cascade) compare match detection		0058H		√	√	√
		43	INTIT01	8-bit interval timer channel 01 compare match detection		005AH		√	√	√

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 42 indicates the lowest priority.

2. Basic configuration types (A) to (C) correspond to (A) to (C) in Figure 24-1.

3. The input buffer power supply of the INTRTCIC0, INTRTCIC1, and INTRTCIC2 pins is connected to internal V_{DD}. Interrupts can be accepted even when a battery backup function is used and power is supplied from the VBAT pin.

Table 24-2. Flags Corresponding to Interrupt Request Sources (3/3)

Interrupt Source	Interrupt Request Flag	Register	Interrupt Mask Flag	Register	Priority Specification Flag	Register
INTTM06	TMIF06	IF2H	TMMK06	MK2H	TMPR006, TMPR106	PR02H, PR12H
INTTM07	TMIF07		TMMK07		TMPR007, TMPR107	
INTIT00	ITIF00		ITMK00		ITPR000, ITPR100	
INTIT01	ITIF01		ITMK01		ITPR001, ITPR101	
INTSRE3	SREIF3		SREMK3		SREPR03, SREPR13	
INTMACLOF	MACIF		MACMK		MACPR0, MACPR1	
INTOSDC	OSDIF		OSDMK		OSDPR0, OSDPR1	
INTFL	FLIF		FLMK		FLPR0, FLPR1	
INTDSADZC0	DSAZIF0	IF3L	DSAZMK0	MK3L	DSAZPR00, DSAZPR10	PR03L, PR13L
INTDSADZC1	DSAZIF1		DSAZMK1		DSAZPR01, DSAZPR11	
INTIT10	ITIF10		ITMK10		ITPR010, ITPR110	
INTIT11	ITIF11		ITMK11		ITPR011, ITPR111	
INTLVDVDD	LVDVDIF		LVDVDMK		LVDVDPR0, LVDVDPR1	
INTLVDVBAT	LVDVBIF		LVDVBMK		LVDVBPR0, LVDVBPR1	
INTLVDVRTC	LVDVRIF		LVDVRMK		LVDVRPR0, LVDVRPR1	
INTLVDEXLVD	LVDEXIF		LVDEXMK		LVDEXPR0, LVDEXPR1	

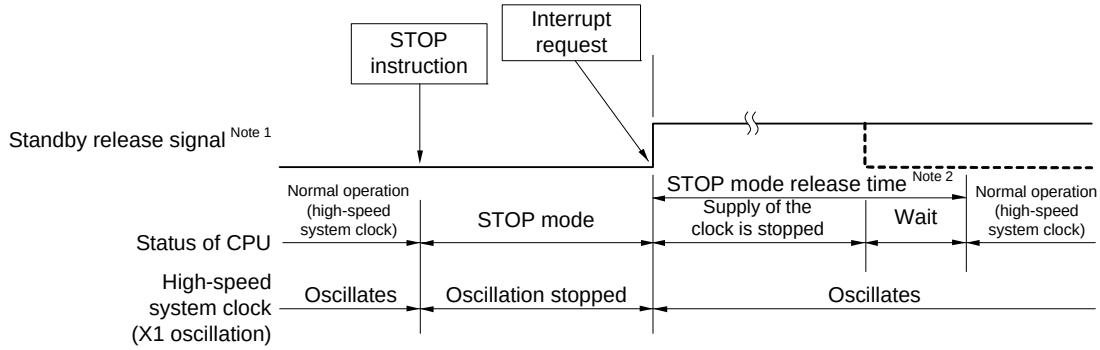
Table 26 - 1 Operating Statuses in HALT Mode (4/4)

Item \ HALT Mode Setting		When HALT Instruction is Executed While CPU is Operating on Subsystem Clock		
		When CPU is Operating on XT1 Clock (f_{XT})	When CPU is Operating on External Subsystem Clock (f_{EXS})	When CPU is Operating on Low-speed on-chip oscillator clock (f_{IL})
AES circuit		Operable		
Power-on-reset function				
RTC power-on-reset function				
Voltage detection function	Internal power supply voltage (internal V_{DD})			
	V_{DD}, V_{BAT}, V_{RTC}, EXLVD pin supply voltage			
External interrupt	INTP0 to INTP7			
	RTCIC0 to RTCIC2			
Key interrupt function				
CRC operation function	High-speed CRC	Operation disabled		
	General-purpose CRC	In the calculation of the RAM area, operable when DTC is executed only		
Illegal-memory access detection function		Operable when DTC is executed only		
RAM parity error detection function				
RAM guard function				
SFR guard function				

Remark Operation stopped: Operation is automatically stopped before switching to the HALT mode.
Operation disabled: Operation is stopped before switching to the HALT mode.
f_{IH}: High-speed on-chip oscillator clock
f_{IL}: Low-speed on-chip oscillator clock
f_{IM}: Middle-speed on-chip oscillator clock
f_X: X1 clock
f_{EX}: External main system clock
f_{XT}: XT1 clock
f_{EXS}: External subsystem clock
f_{PLL}: PLL clock frequency

Figure 26 - 4 STOP Mode Release by Interrupt Request Generation (2/2)

(2) When high-speed system clock (X1 oscillation) is used as CPU clock



Note 1. For details of the standby release signal, see **Figure 24 - 1 Basic Configuration of Interrupt Function**.

Note 2. STOP mode release time

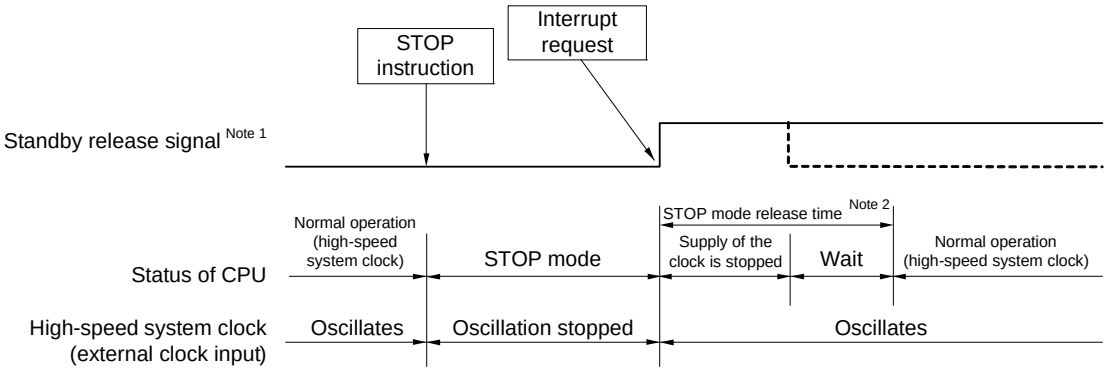
Supply of the clock is stopped:

18 μs to "whichever is longer 65 μs or the oscillation stabilization time (set by OSTS)"

Wait:

- When vectored interrupt servicing is carried out: 10 to 11 clocks
- When vectored interrupt servicing is not carried out: 4 to 5 clocks

(3) When high-speed system clock (external clock input) is used as CPU clock



Note 1. For details of the standby release signal, see **Figure 24 - 1 Basic Configuration of Interrupt Function**.

Note 2. STOP mode release time

Supply of the clock is stopped:

18 μs to 65 μs

Wait:

- When vectored interrupt servicing is carried out: 7 clocks
- When vectored interrupt servicing is not carried out: 1 clock

Caution To reduce the oscillation stabilization time after release from the STOP mode while CPU operates based on the high-speed system clock (X1 oscillation), switch the clock to the high-speed on-chip oscillator clock temporarily before executing the STOP instruction.

Remark 1. The clock supply stop time varies depending on the temperature conditions and STOP mode period.

Remark 2. The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

Bit 0 (LVIRF) of the reset control flag register (RESF) is set to 1 if reset occurs. For details of the RESF register, see **CHAPTER 27 RESET FUNCTION**.

The RL78/I1C products have voltage detection function for each power supply pin.

While voltage detection function is operating, whether the supply voltage of each pin is more than the detection level can be checked by interruption or reading the voltage detection flag.

- The LVD circuit compares the V_{DD} pin voltage (V_{DD}) with the detection voltage (V_{LVDVDD}), and generates a one-shot interrupt request signal (INTLVDVDD) by detecting $V_{DD} > V_{LVDVDD}$ or $V_{DD} < V_{LVDVDD}$.

- The LVD circuit compares the VBAT pin voltage (VBAT) with the detection voltage ($V_{LVDVBAT}$), and generates a one-shot interrupt request signal (INTLVDVBAT) by detecting VBAT > $V_{LVDVBAT}$ or VBAT < $V_{LVDVBAT}$.

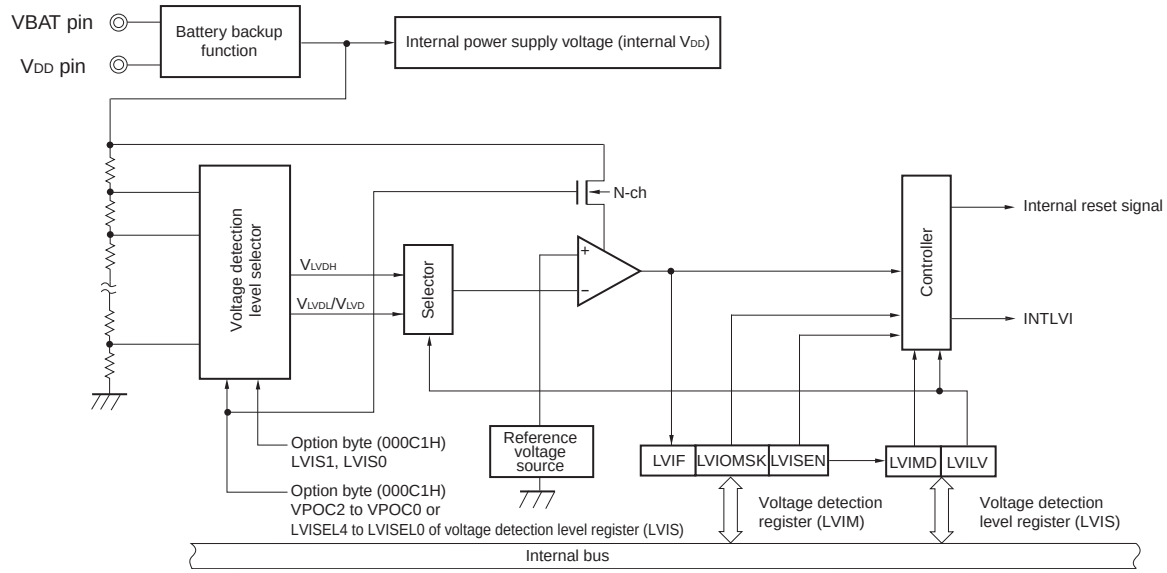
- The LVD circuit compares the VRTC pin voltage (VRTC) with the detection voltage ($V_{LVDVRTC}$), and generates a one-shot interrupt request signal (INTLVDVRTC) by detecting VRTC > $V_{LVDVRTC}$ or VRTC < $V_{LVDVRTC}$.

- The LVD circuit compares the EXLVD pin voltage (EXLVD) with the detection voltage ($V_{LVDEXLVD}$), and generates a one-shot interrupt request signal (INTLVDEXLVD) by detecting EXLVD > $V_{LVDEXLVD}$ or EXLVD < $V_{LVDEXLVD}$.

29.2 Configuration of Voltage Detector

The block diagrams of the voltage detector (LVD) are shown in Figure 29 - 1 to Figure 29 - 5.

Figure 29 - 1 Block Diagram of Voltage Detector (LVD)



29.5 Changing of LVD Detection Voltage Setting

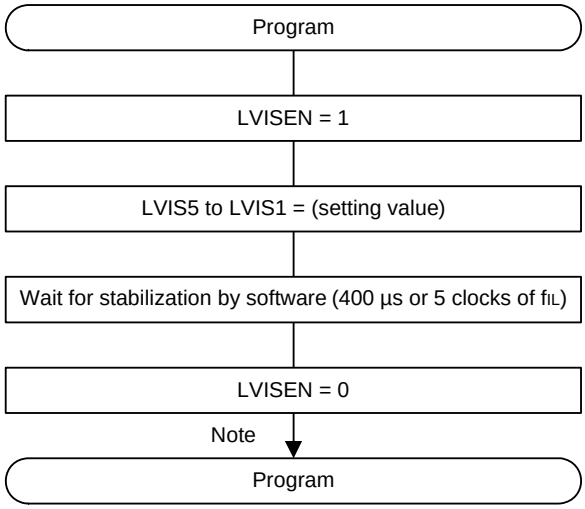
To change the LVD detection voltage by software, use the following procedure.

The LVD detection voltage can be changed in interrupt mode and reset mode.

In interrupt & reset mode, the value of the LVD detection voltage cannot be changed. Keep the initial value (set value in the option byte) unchanged.

To use two or more LVD detection voltages by changing LVISEL4 to LVISEL0 in the LVIS register by software, the highest voltage value of the used LVD detection voltages must be specified in the VPOC2 to VPOC0, LVIS1, and LVIS0 bits in the option byte (000C1H).

Figure 29 - 25 Changing of LVD Detection Voltage Setting



Note After LVISEN is set to 0, LVD is detected if $V_{LVD} > V_{DD}$, and a reset/interrupt is generated.

Figure 30-12. Power Supply Switching Operation with Hardware (VBATSEL = 0)

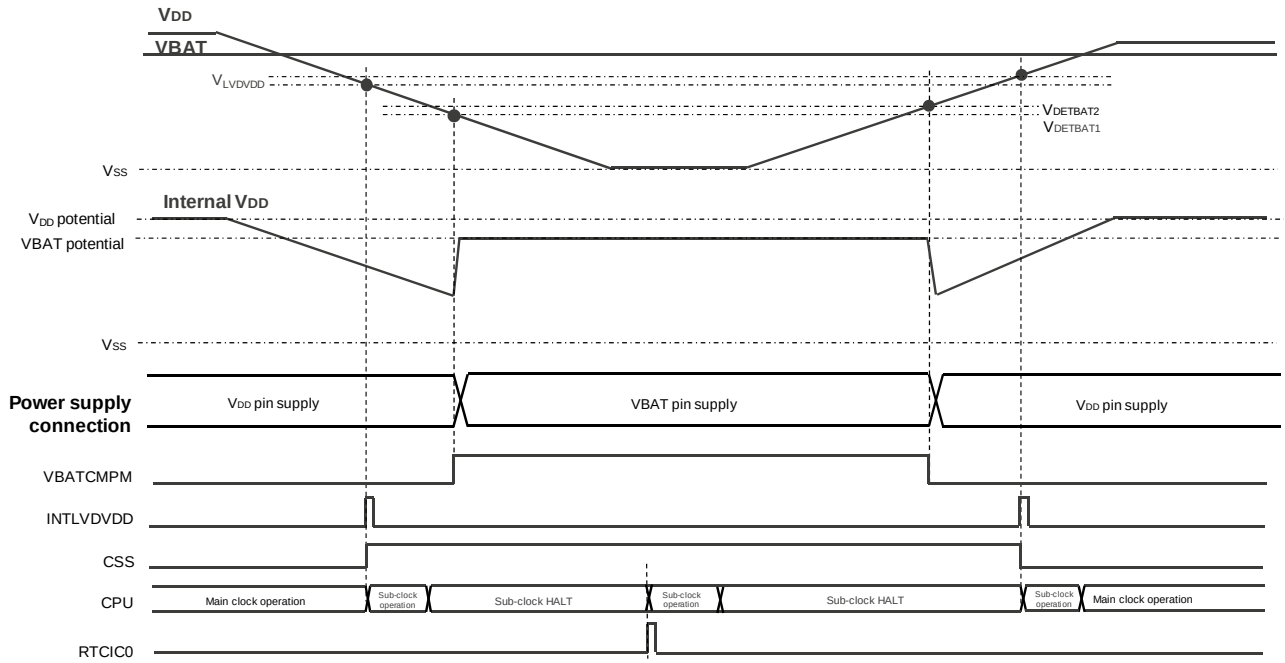
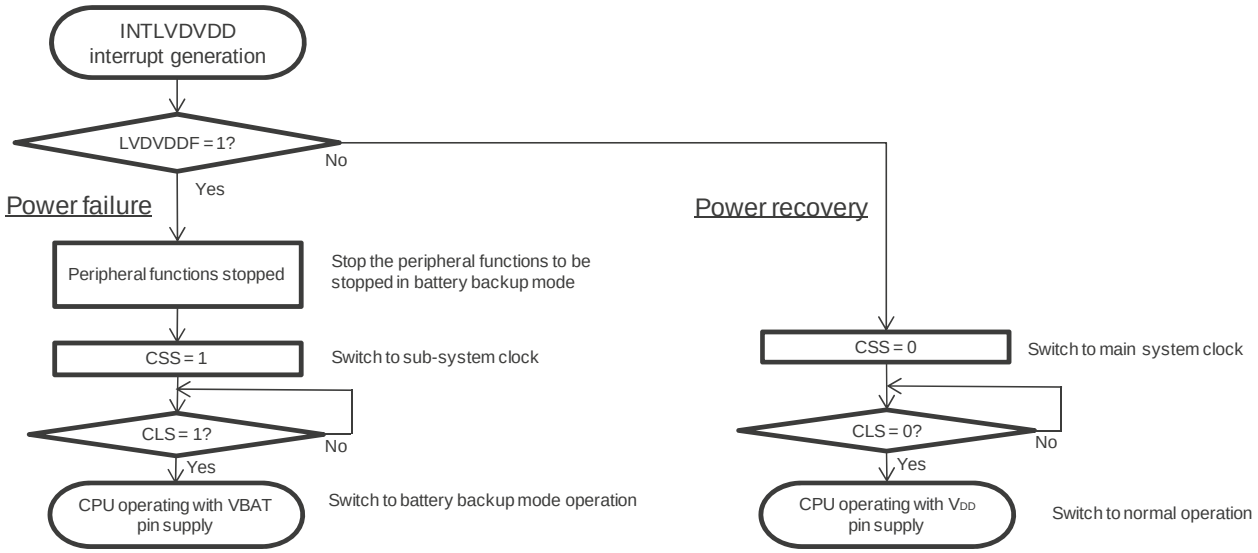


Figure 30-13. Setting Procedure for Power Supply Switching with Hardware



36.4.3 Selecting communication mode

Communication mode of the RL78 microcontroller as follows.

Table 36 - 6 Communication Modes

Communication Mode	Standard Setting Note 1				Pins Used
	Port	Speed Note 2	Frequency	Multiply Rate	
1-line mode (when flash memory programmer is used, or when external device is used)	UART	115200 bps, 250000 bps, 500000 bps, 1 Mbps	—	—	TOOL0
Dedicated UART (when external device is used)	UART	115200 bps, 250000 bps, 500000 bps, 1 Mbps	—	—	TOOLTxD, TOOLRxD

Note 1. Selection items for Standard settings on GUI of the flash memory programmer.

Note 2. Because factors other than the baud rate error, such as the signal waveform slew, also affect UART communication, thoroughly evaluate the slew as well as the baud rate error.