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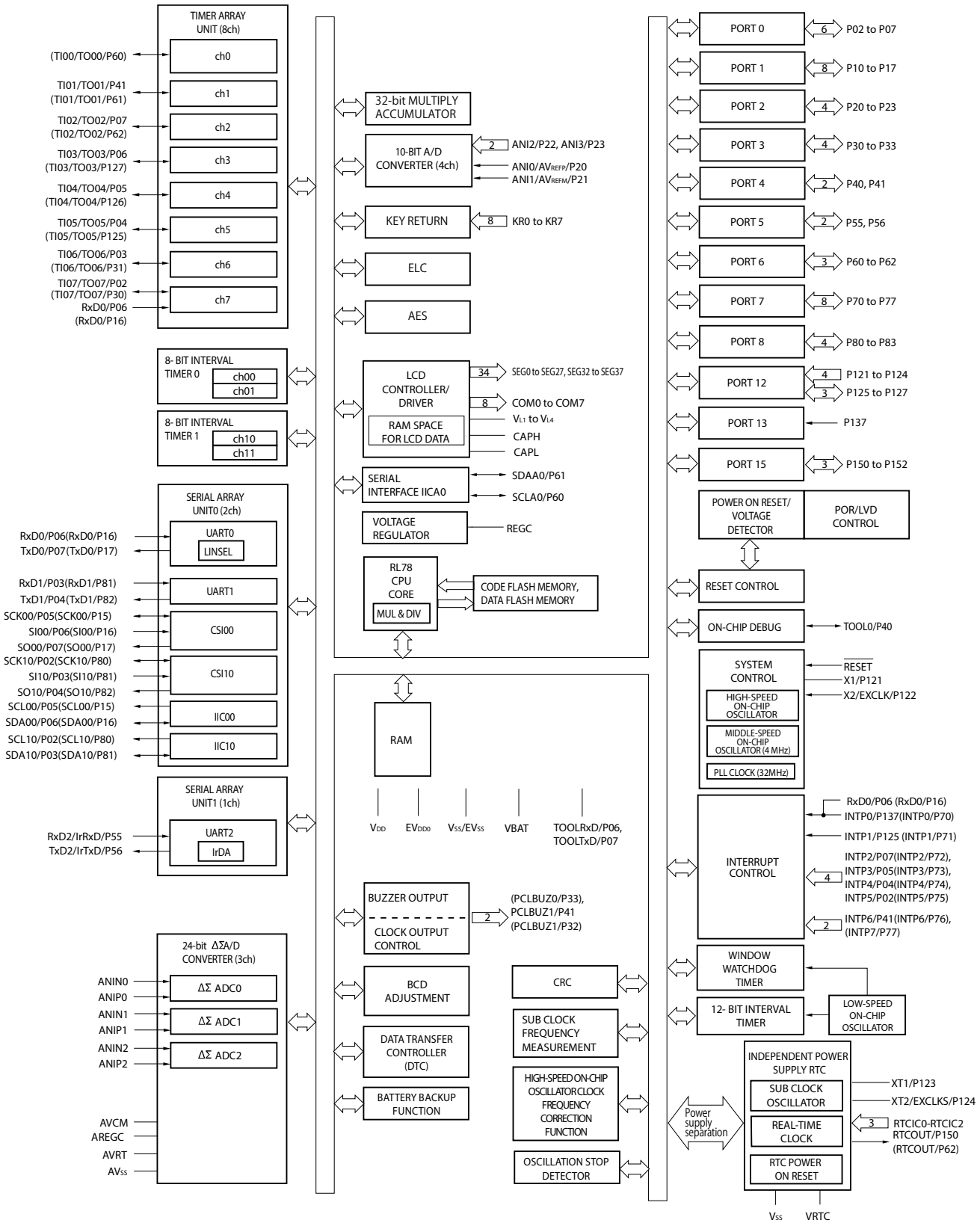
Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, IrDA, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 5.5V
Data Converters	A/D 4x10b, 3x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10nmgdfb-50

1.5.2 80-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR0). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR0)**.

1.6 Outline of Functions

(1/3)

	Item		64-pin		80-pin			100-pin	
<R>			R5F10NLEDFB	R5F10NLGDFB	R5F10NMEDFB	R5F10NMGDFB	R5F10NMJDFB	R5F10NPGDFB	R5F10NPJDFB
	Code flash memory (KB)		64 KB	128 KB	64 KB	128 KB	256 KB	128 KB	256 KB
	Data flash memory (KB)		2 KB						
	RAM (KB)		6 KB	8 KB[Note 1]	6 KB	8 KB[Note 1]	16 KB[Note 2]	8 KB[Note 1]	16 KB[Note 2]
	Address space		1 MB						
<R>	Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.5 to 5.5 V), HS (High-speed main) mode: 1 to 12 MHz (V_{DD} = 2.4 to 5.5 V), HS (High-speed main) mode: 1 to 6 MHz (V_{DD} = 2.1 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.9 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.7 to 5.5 V), LP (Low-power main) mode: 1 MHz (V_{DD} = 1.9 to 5.5 V)						
		High -speed on-chip oscillator clock (f_{IH}) MAX.: 24 MHz Middle -speed on-chip oscillator clock (f_{IM}) MAX.: 4 MHz	HS (High-speed main) mode: 1 to 24 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.5 to 5.5 V), HS (High-speed main) mode: 1 to 12 MHz (V_{DD} = 2.4 to 5.5 V), HS (High-speed main) mode: 1 to 6 MHz (V_{DD} = 2.1 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.9 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.7 to 5.5 V), LP (Low-power main) mode: 1 MHz (V_{DD} = 1.9 to 5.5 V)						
		PLL clock (f_{PLL})	-				HS (High-speed main) mode: 32 MHz (V_{DD} = 2.8 to 5.5 V)		
	Subsystem clock	Subsystem clock oscillator clock (f_{SX})	XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz (TYP.): V_{DD} = 1.7 to 5.5 V						
		Low-speed on-chip oscillator clock (f_{IL})	15 kHz (TYP.): V_{DD} = 1.7 to 5.5V						
	High-speed on-chip oscillator clock frequency correction function		Correct the frequency of the high-speed on-chip oscillator clock by the subsystem clock.						
	General-purpose register		8 bits × 8 registers × 4 banks						
	Minimum instruction execution time		0.03125 μs (PLL clock: f_{PLL} = 32 MHz selection)						
			0.04167 μs (High-speed on-chip oscillator: f_{IH} = 24 MHz operation)						
			30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)						
			66.6 μs (Low-speed on-chip oscillator: f_{IL} = 15 kHz operation)						
	Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (16 bits × 16 bits), division (32 bits ÷ 32 bits) • Multiplication and accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (set, reset, test, and boolean operation), etc.						
	I/O port	Total	35		52			68	
		CMOS I/O	27		44			60	
		CMOS input	5		5			5	
		CMOS output	-		-			-	
		N-ch O.D I/O (6 V tolerance)	3		3			3	

Notes 1. In the case of the 8 KB, this is about 7 KB when the self-programming function is used.

2. In the case of the 16 KB, this is about 15 KB when the self-programming function is used.

4.3.3 Pull-up resistor option registers (PUxx)

These registers specify whether the on-chip pull-up resistors are to be used or not. On-chip pull-up resistors can be used in 1-bit units only for the bits set to normal output mode (POMmn = 0) and input mode (PMmn = 1) for the pins to which the use of an on-chip pull-up resistor has been specified in these registers. On-chip pull-up resistors cannot be connected to bits set to output mode and bits used as alternate-function output pins and analog setting (ADPC = 1), regardless of the settings of these registers.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H (PU4 is set to 01H, PU15 is set to 07H).

Caution When a port with the PIMn register is input from different potential device to TTL buffer, pull up to the power supply of the different potential device via an external pull-up resistor by setting PUmn = 0.

Figure 4-3. Format of Pull-up Resistor Option Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU0	PU07	PU06	PU05	PU04	PU03	PU02	0	0	F0030H	00H	R/W
PU1	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10	F0031H	00H	R/W
PU3	PU37	PU36	PU35	PU34	PU33	PU32	PU31	PU30	F0033H	00H	R/W
PU4	0	0	0	0	PU43	PU42	PU41	PU40	F0034H	01H	R/W
PU5	PU57	PU56	PU55	PU54	PU53	PU52	PU51	PU50	F0035H	00H	R/W
PU7	PU77	PU76	PU75	PU74	PU73	PU72	PU71	PU70	F0037H	00H	R/W
PU8	0	0	PU85	PU84	PU83	PU82	PU81	PU80	F0038H	00H	R/W
PU12	PU127	PU126	PU125	0	0	0	0	0	F003CH	00H	R/W
PU15	0	0	0	0	0	PU152	PU151	PU150	F003FH	07H	R/W

PUmn	Pmn pin on-chip pull-up resistor selection (m = 0, 1, 3 to 5, 7, 8, 12, 15 ; n = 0 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Caution Be sure to set bits that are not mounted to their initial values.

Table 4-6. Setting Examples of Registers and Output Latches When Using Alternate Function (5/10)

Pin Name	Used Function		PIOR0×	POM××	PM××	P××	PFSEG×× (ISCVL3, ISCCAP)[Note]	Alternate Function Output		64-pin	80-pin	100-pin
	Function Name	I/O						SAU Output Function	Other than SAU			
P30	P30	Input	–	–	1	×	0	–	–	√	√	√
		Output	×	–	0	0/1	0	–	(TO07) = 0			
	SEG24	Output	×	–	0	0	1	–	–			
	(TI07)	Input	PIOR00 = 1	–	1	×	0	–	–	–	√	√
	TI07	Input	PIOR00 = 0	–	1	×	0	–	–	√	–	–
	(TO07)	Output	PIOR00 = 1	–	0	0	0	–	–	–	√	√
	TO07	Output	PIOR00 = 0	–	0	0	0	–	–	√	–	–
	RxD2	Input	×	–	1	×	0	–	–	√	–	–
	IrRxD	Input	×	–	1	×	0	–	–			
	INTP5	Input	PIOR04 = 0	–	1	×	0	–	–			
P31	P31	Input	–	–	1	×	0	–	–	√	√	√
		Output	×	–	0	0/1	0	TxD2/IrTxD = 1	(TO06) = 0			
		N-ch open drain output	×	1	0	0/1	0		–	√	–	–
	SEG25	Output	×	–	0	0	1	–	–	√	√	√
	(TI06)	Input	PIOR00 = 1	–	1	×	0	–	–	–	√	√
	TI06	Input	PIOR00 = 0	–	1	×	0	–	–	√	–	–
	(TO06)	Output	PIOR00 = 1	–	0	0	0	–	–	–	√	√
	TO06	Output	PIOR00 = 0	–	0	0	0	–	–	√	–	–
	TxD2	Output	×	0/1	0	1	0	–	–	√	–	–
	IrTxD	Output	×	0/1	0	1	0	–	–			
P32	P32	Input	–	–	1	×	0	–	–	–	√	√
		Output	×	–	0	0/1	0	–	(PCLBUZ1) = 0			
	SEG26	Output	×	–	0	0	1	–	–			
	(PCLBUZ1)	Output	PIOR03 = 1	–	0	0	0	–	–			
P33	P33	Input	–	–	1	×	0	–	–	–	√	√
		Output	×	–	0	0/1	0	–	(PCLBUZ0) = 0			
	SEG27	Output	×	–	0	0	1	–	–			
	(PCLBUZ0)	Output	PIOR03 = 1	–	0	0	0	–	–			
P34	P34	Input	–	–	1	×	0	–	–	–	–	√
		Output	–	–	0	0/1	0	–	–			
	SEG28	Output	–	–	0	0	1	–	–			
P35	P35	Input	–	–	1	×	0	–	–	–	–	√
		Output	–	–	0	0/1	0	–	–			
	SEG29	Output	–	–	0	0	1	–	–			
P36	P36	Input	–	–	1	×	0	–	–	–	–	√
		Output	–	–	0	0/1	0	–	–			
	SEG30	Output	–	–	0	0	1	–	–			
P37	P37	Input	–	–	1	×	0	–	–	–	–	√
		Output	–	–	0	0/1	0	–	–			
	SEG31	Output	–	–	0	0	1	–	–			
P40	P40	Input	–	–	1	×	–	–	–	√	√	√
		Output	–	–	0	0/1	–	–	–			
	TOOL0	I/O	–	–	×	×	–	–	–			
P41	P41	Input	–	–	1	×	–	–	–	–	√	√
		Output	×	–	0	0/1	–	–	TO01 = 0 PCLBUZ1 = 0			
	TI01	Input	PIOR00 = 0	–	1	×	–	–	–	√	√	√
	TO01	Output	PIOR00 = 0	–	0	0	–	–	PCLBUZ1 = 0			
	PCLBUZ1	Output	PIOR03 = 0	–	0	0	–	–	TO01 = 0	–	√	√
	INTP6	Input	PIOR04 = 0	–	1	×	–	–	–			

Note ISCVL3 and ISCCAP are registers that correspond to P125, and P126 and P127, respectively.

Table 4-6. Setting Examples of Registers and Output Latches When Using Alternate Function (9/10)

Pin Name	Used Function		CMC Register (EXCLK, OSCSEL)	SCMC Register (EXCLKS, OSCSELS)	P××	64-pin	80-pin	100-pin
	Function Name	I/O						
P121	P121	Input	00/10/11	–	×	√	√	√
	X1	–	01		–			
P122	P122	Input	00/10		×	√	√	√
	X2	–	01		–			
	EXCLK	Input	11		–			
P123	P123	Input	–	00/10/11	×	√	√	√
	XT1	–		01	–			
P124	P124	Input		00/10	×	√	√	√
	XT2	–		01	–			
	EXCLKS	Input		11	–			

Table 4-6. Setting Examples of Registers and Output Latches When Using Alternate Function (10/10)

Pin Name	Used Function		PIOR0×	POM××	PM××	P××	PFSEG×× (ISCVL3, ISCCAP)[Note]	Alternate Function Output		64-pin	80-pin	100-pin
	Function Name	I/O						SAU Output Function	Other than SAU			
P125	P125	Input	–	–	1	×	1	–	–	√	√	√
		Output	×	–	0	0/1	1	–	(TO05) = 0 PCLBUZ1 = 0			
	V_{L3}	–	×	–	1	×	0	–	–			
	INTP1	Input	PIOR04 = 0	–	1	×	1	–	–			
	(TI05)	Input	PIOR00 = 1	–	1	×	1	–	–	–	√	√
	TI05	Input	PIOR00 = 0	–	1	×	1	–	–	√	–	–
	(TO05)	Output	PIOR00 = 1	–	0	0	1	–	PCLBUZ1 = 0	–	√	√
	TO05	Output	PIOR00 = 0	–	0	0	1	–	PCLBUZ1 = 0	√	–	–
	PCLBUZ1	Output	PIOR03 = 0	–	0	0	1	–	TO05 = 0			
P126	P126	Input	–	–	1	×	1	–	–	√	√	√
		Output	×	–	0	0/1	1	–	(TO04) = 0			
	CAPL	–	×	–	1	×	0	–	–			
	(TI04)	Input	PIOR00 = 1	–	1	×	1	–	–			
	(TO04)	Output	PIOR00 = 1	–	0	0	1	–	–			
P127	P127	Input	–	–	1	×	1	–	–	√	√	√
		Output	×	–	0	0/1	1	–	(TO03) = 0			
	CAPH	–	×	–	1	×	0	–	–			
	(TI03)	Input	PIOR00 = 1	–	1	×	1	–	–			
	(TO03)	Output	PIOR00 = 1	–	0	0	1	–	–			
P137	P137	Input	–	–	–	×	–	–	–	√	√	√
	INTP0	Input	PIOR04 = 0	–	–	×	–	–	–			
P150	P150	Input	–	×	1	×	–	–	–	–	√	√
		Output	×	–	0	0/1	–	–	–			
	RTCOUT	Output	PIOR03 = 0	–	0	0	–	–	–			
	RTCIC0	Input	×	–	1	×	–	–	–			
P151	P151	Input	–	×	1	×	–	–	–	–	√	√
		Output	–	–	0	0/1	–	–	–			
	RTCIC1	Input	–	–	1	×	–	–	–			
P152	P152	Input	–	–	1	×	–	–	–	–	√	√
		Output	–	–	0	0/1	–	–	–			
	RTCIC2	Input	–	–	1	×	–	–	–			

Note ISCVL3 and ISCCAP are registers that correspond to P125, and P126 and P127, respectively.

power consumption oscillation (AMPHS1, AMPHS0 = 1, 0) is selected.

• Configure the circuit of the circuit board, using material with little parasitic capacitance and wiring resistance.

• Place a ground pattern that has the same potential as Vss as much as possible near the XT1 oscillator.

• Be sure that the signal lines between the XT1 and XT2 pins, and the resonators do not cross with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.

• The impedance between the XT1 and XT2 pins may drop and oscillation may be disturbed due to moisture absorption of the circuit board in a high-humidity environment or dew condensation on the board. When using the circuit board in such an environment, take measures to damp-proof the circuit board, such as by coating.

• When coating the circuit board, use material that does not cause capacitance or leakage between the XT1 and XT2 pins.

Caution 7. Be sure to clear bits 7, 6, 3, and 0 to 0.

15.6.5 Hardware trigger no-wait mode (select mode, sequential conversion mode)

<1> In the stop status, the ADCE bit of A/D converter mode register 0 (ADM0) is set to 1, and the system enters the A/D conversion standby status.

<2> After the software counts up to the stabilization wait time (1 μs), the ADCS bit of the ADM0 register is set to 1 to place the system in the hardware trigger standby status (and conversion does not start at this stage). Note that, while in this status, A/D conversion does not start even if ADCS is set to 1.

<3> If a hardware trigger is input while ADCS = 1, A/D conversion is performed on the analog input specified by the analog input channel specification register (ADS).

<4> When A/D conversion ends, the conversion result is stored in the A/D conversion result register (ADCR, ADCRH), and the A/D conversion end interrupt request signal (INTAD) is generated. After A/D conversion ends, the next A/D conversion immediately starts.

<5> If a hardware trigger is input during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.

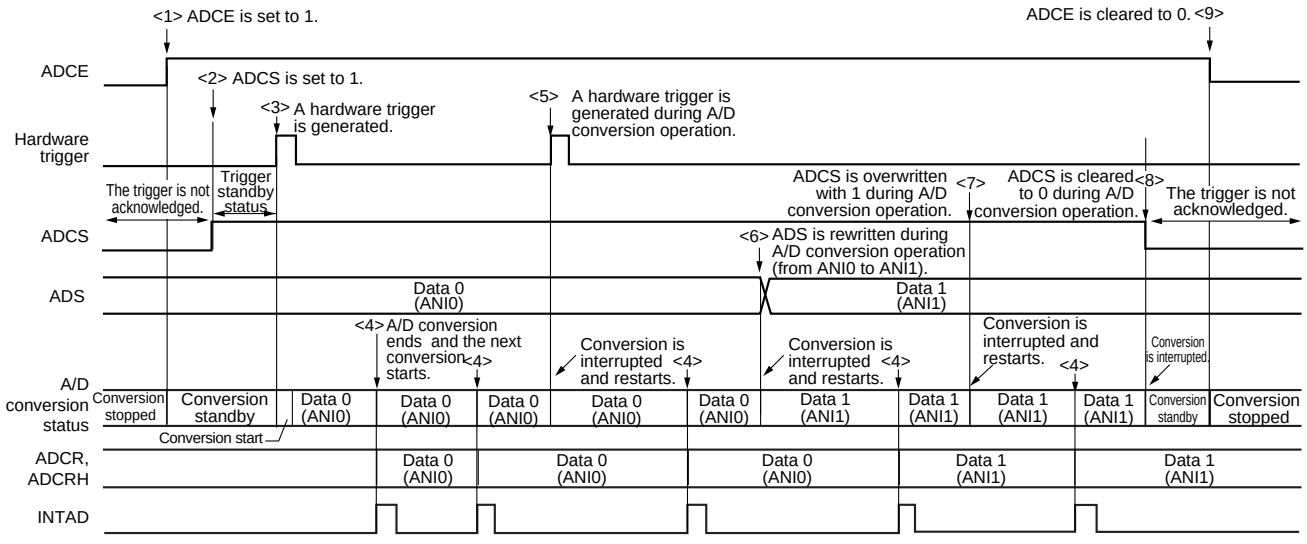
<6> When the value of the ADS register is rewritten or overwritten during conversion operation, the current A/D conversion is interrupted, and A/D conversion is performed on the analog input respecified by the ADS register. The partially converted data is discarded.

<7> When ADCS is overwritten with 1 during conversion operation, the current A/D conversion is interrupted, and conversion restarts. The partially converted data is discarded.

<8> When ADCS is cleared to 0 during conversion operation, the current A/D conversion is interrupted, and the system enters the A/D conversion standby status. However, the A/D converter does not stop in this status.

<9> When ADCE is cleared to 0 while in the A/D conversion standby status, the A/D converter enters the stop status. When ADCS = 0, inputting a hardware trigger is ignored and A/D conversion does not start.

Figure 15-22. Example of Hardware Trigger No-wait Mode (Select Mode, Sequential Conversion Mode) Operation Timing



17.2.13 Peripheral clock control register (PCKC)

The PCKC register is used to control peripheral clocks. Set bit 0 to select a clock for the 24-bit ΔΣ A/D converter.

The PCKC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 17-20. Format of Peripheral Clock Control Register (PCKC)

Address: F0098H After reset: 00H R/W

Symbol	7	6	5	4	3	2	<1>	<0>
PCKC	0	0	0	0	0	0	PLLCK	DSADCK

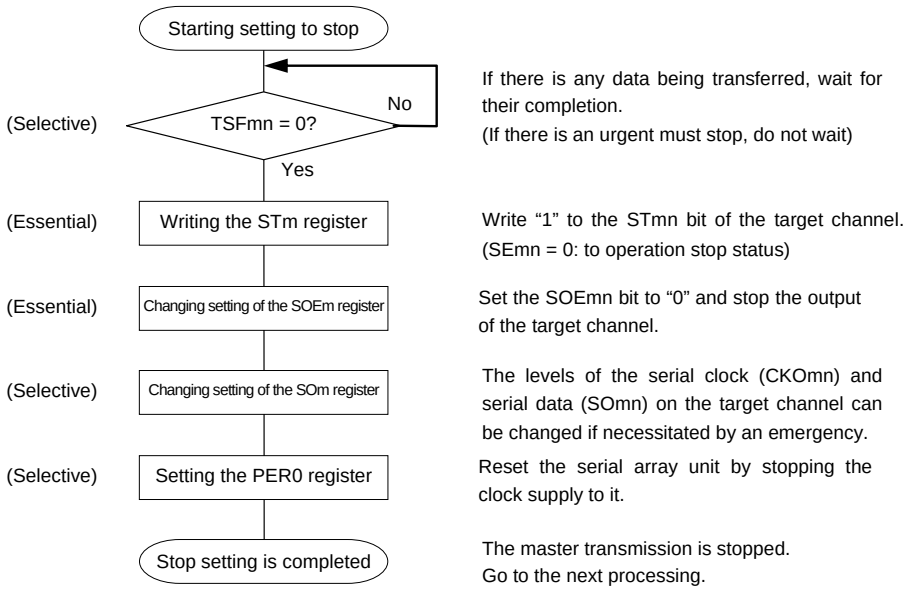
DSADCK	Selection of operation clock for 24-bit ΔΣ A/D converter
0	Supply high-speed on-chip oscillator clock (f_{IH}). (Stop f_{MX} supply)Note 1
1	Supply high-speed system clock (f_{MX})Note 2

Notes 1. When selecting the high-speed on-chip oscillator clock, be sure to run the high-speed on-chip oscillator clock frequency correction function.

2. Only a 12 MHz crystal oscillator can be used as the high-speed system clock frequency (f_{MX}).

Caution Be sure to clear bits 7 to 2 to "0".

Figure 18-44. Procedure for Stopping Master Transmission/Reception



CHAPTER 19 SERIAL INTERFACE IICA

19.1 Functions of Serial Interface IICA

Serial interface IICA has the following three modes.

(1) Operation stop mode

This mode is used when serial transfers are not performed. It can therefore be used to reduce power consumption.

(2) I^2C bus mode (multimaster supported)

This mode is used for 8-bit data transfers with several devices via two lines: a serial clock (SCLAn) line and a serial data bus (SDAAn) line.

This mode complies with the I^2C bus format and the master device can generated “start condition”, “address”, “transfer direction specification”, “data”, and “stop condition” data to the slave device, via the serial data bus. The slave device automatically detects these received status and data by hardware. This function can simplify the part of application program that controls the I^2C bus.

Since the SCLAn and SDAAn pins are used for open drain outputs, serial interface IICA requires pull-up resistors for the serial clock line and the serial data bus line.

(3) Wakeup mode

The STOP mode can be released by generating an interrupt request signal (INTIICAn) when an extension code from the master device or a local address has been received while in STOP mode. This can be set by using the WUPn bit of IICA control register n1 (IICCTLn1).

Figure 19-1 shows a block diagram of serial interface IICA.

Remark n = 0

19.2 Configuration of Serial Interface IICA

Serial interface IICA includes the following hardware.

Table 19-1. Configuration of Serial Interface IICA

Item	Configuration
Registers	IICA shift register n (IICAn) Slave address register n (SVAn)
Control registers	Peripheral enable register 0 (PER0) Peripheral Reset Control Register 0 (PRR0) IICA control register n0 (IICCTLn0) IICA status register n (IICSn) IICA flag register n (IICFn) IICA control register n1 (IICCTLn1) IICA low-level width setting register n (IICWLn) IICA high-level width setting register n (IICWHn) Port mode register 6 (PM6) Port register 6 (P6)

Remark n = 0

(1) IICA shift register n (IICAn)

The IICAn register is used to convert 8-bit serial data to 8-bit parallel data and vice versa in synchronization with the serial clock. The IICAn register can be used for both transmission and reception.

The actual transmit and receive operations can be controlled by writing and reading operations to the IICAn register.

Cancel the wait state and start data transfer by writing data to the IICAn register during the wait period.

The IICAn register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears IICAn to 00H.

Figure 19-3. Format of IICA Shift Register n (IICAn)

Address: FFF50H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
IICAn								

Cautions 1. Do not write data to the IICAn register during data transfer.

2. Write or read the IICAn register only during the wait period. Accessing the IICAn register in a communication state other than during the wait period is prohibited. When the device serves as the master, however, the IICAn register can be written only once after the communication trigger bit (STTn) is set to 1.

3. When communication is reserved, write data to the IICAn register after the interrupt triggered by a stop condition is detected.

Remark n = 0

(2) When communication reservation function is disabled (bit 0 (IICRSVn) of IICA flag register n (IICFn) = 1)

When bit 1 (STTn) of IICA control register n0 (IICCTLn0) is set to 1 when the bus is not used in a communication during bus communication, this request is rejected and a start condition is not generated. The following two statuses are included in the status where bus is not used.

- When arbitration results in neither master nor slave operation
- When an extension code is received and slave operation is disabled (ACK is not returned and the bus was released by setting bit 6 (LRELn) of the IICCTLn0 register to 1 and saving communication)

To confirm whether the start condition was generated or request was rejected, check STCFn (bit 7 of the IICFn register). It takes up to 5 clocks of f_{MCK} until the STCFn bit is set to 1 after setting STTn = 1. Therefore, secure the time by software.

Remark n = 0

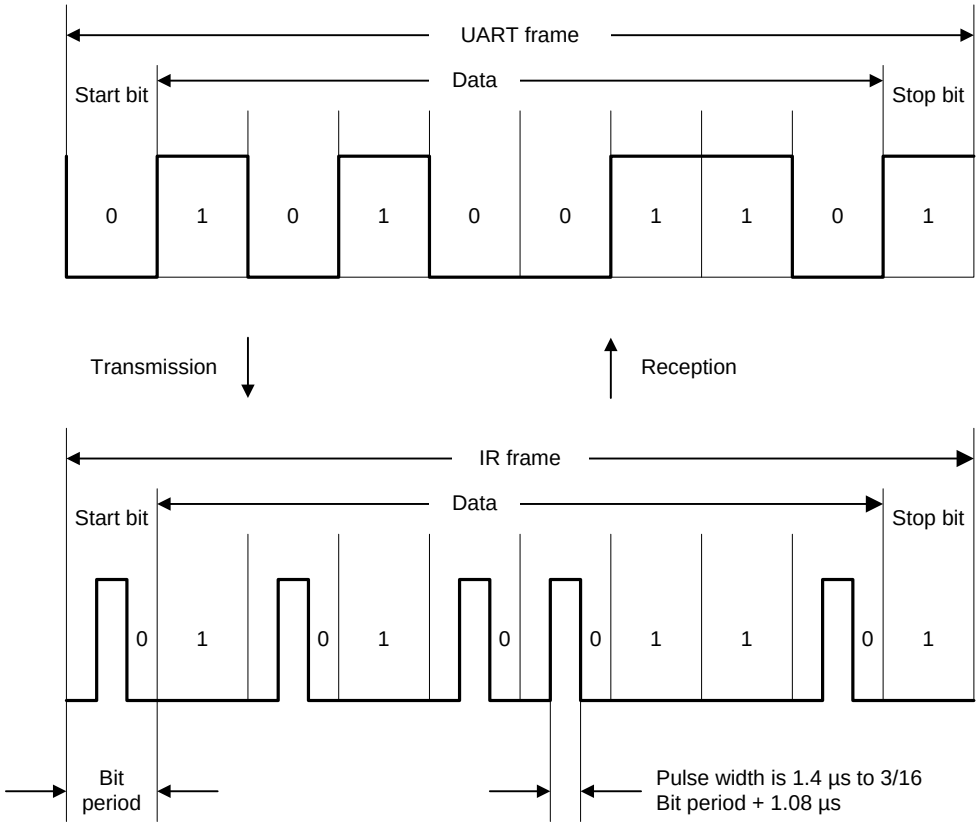
20.3.2 Transmission

In transmission, the signals output from the SAU (UART frames) are converted to the IR frame data through the IrDA (see **Figure 20-5**). When IRTXINV bit is 0 and serial data is 0, high-level pulses with the width of 3/16 the bit rate (1-bit width period) are output (initial setting). The high-level pulse width can be changed by using the IRCKS2 to IRCKS0 bits. The standard prescribes that the minimum high-level pulse width should be 1.41 μs and the maximum high-level pulse width be (3/16 + 2.5%) $\times$ bit rate or (3/16 $\times$ bit rate) + 1.08 μs.

When the CPU/peripheral hardware clock (f_{CLK}) is 20 MHz, the high-level pulse width can be 1.41 μs to 1.6 μs.

When serial data is 1, no pulses are output.

Figure 20-5. IrDA Transmission/Reception



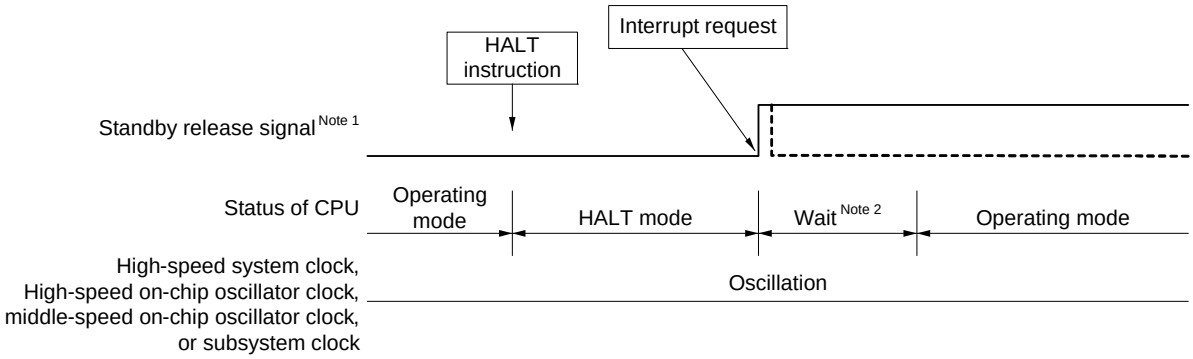
(2) HALT mode release

The HALT mode can be released by the following two sources.

(a) Release by unmasked interrupt request

When an unmasked interrupt request is generated, the HALT mode is released. If interrupt acknowledgment is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgment is disabled, the next address instruction is executed.

Figure 26 - 1 HALT Mode Release by Interrupt Request Generation



Note 1. For details of the standby release signal, see **Figure 24 - 1 Basic Configuration of Interrupt Function**.

Note 2. Wait time for HALT mode release

- When vectored interrupt servicing is carried out
  - Main system clock: 15 to 16 clocks
  - Subsystem clock (RTCLPC = 0): 10 to 11 clocks
  - Subsystem clock (RTCLPC = 1): 11 to 12 clocks
- When vectored interrupt servicing is not carried out
  - Main system clock: 9 to 10 clocks
  - Subsystem clock (RTCLPC = 0): 4 to 5 clocks
  - Subsystem clock (RTCLPC = 1): 5 to 6 clocks

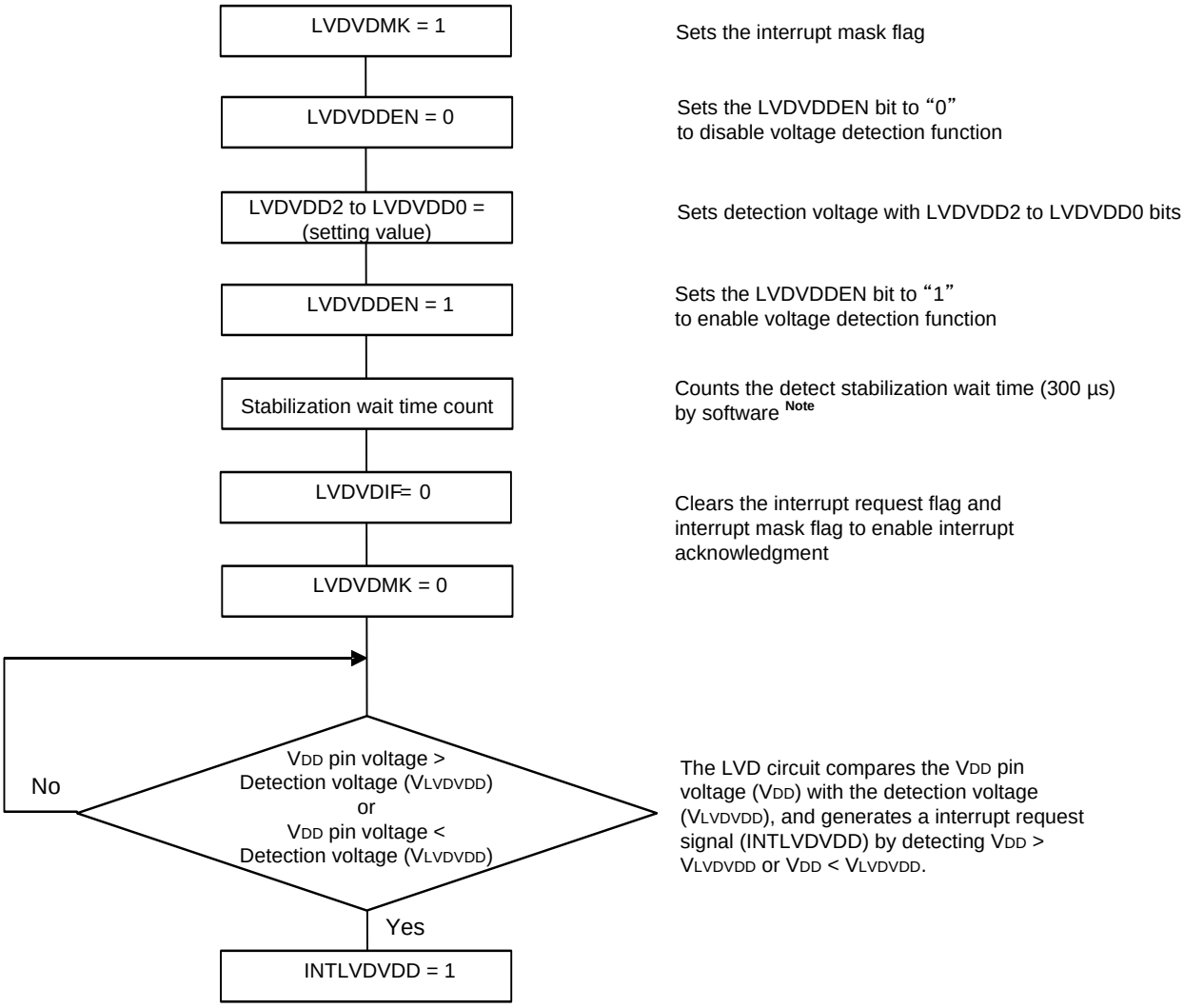
Remark The broken lines indicate the case when the interrupt request which has released the standby mode is acknowledged.

29.4.4 Each power supply pin voltage detection setting procedure

(1) V_{DD}

The setting procedure of V_{DD} pin voltage detection is shown below.

Figure 29 - 21 Setting Procedure of V_{DD} Pin Voltage Detection



Note Be sure to set the detection voltage level when pin voltage < detection voltage.

Caution If other process operating secures the stabilization wait time after setting the LVDVDDEN bit to 1 to enable the voltage detect function operation, the count process isn't required.

Table 36 - 12 Relationship Between Enabling Security Function and Command

(1) During serial programming

Valid Security	Executed Command	
	Block Erase	Write
Prohibition of block erase	Blocks cannot be erased.	Can be performed. Note
Prohibition of writing	Blocks can be erased.	Cannot be performed.
Prohibition of rewriting boot cluster 0	Boot cluster 0 cannot be erased.	Boot cluster 0 cannot be written.

Note Confirm that no data has been written to the write area. Because data cannot be erased after block erase is prohibited, do not write data if the data has not been erased.

(2) During self-programming

Valid Security	Executed Command	
	Block Erase	Write
Prohibition of block erase	Blocks can be erased.	Can be performed.
Prohibition of writing		
Prohibition of rewriting boot cluster 0	Boot cluster 0 cannot be erased.	Boot cluster 0 cannot be written.

Remark To prohibit writing and erasing during self-programming, use the flash shield window function (see **36.6.3** for detail).

Table 36 - 13 Setting Security in Each Programming Mode

(1) During serial programming

Security	Security Setting	How to Disable Security Setting
Prohibition of block erase	Set via GUI of dedicated flash memory programmer, etc.	Cannot be disabled after set.
Prohibition of writing		Set via GUI of dedicated flash memory programmer, etc.
Prohibition of rewriting boot cluster 0		Cannot be disabled after set.

Caution Releasing the setting of prohibition of writing is enabled only when the security is not set as the block erase prohibition and the boot cluster 0 rewrite prohibition with code flash memory area and data flash memory area being blanks.

(2) During self-programming

Security	Security Setting	How to Disable Security Setting
Prohibition of block erase	Set by using flash self-programming library.	Cannot be disabled after set.
Prohibition of writing		Cannot be disabled during self-programming (set via GUI of dedicated flash memory programmer, etc. during serial programming).
Prohibition of rewriting boot cluster 0		Cannot be disabled after set.

Table 40-5. Operation List (4/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag
				Note 1	Note 2		Z AC CY
8-bit data transfer	XCH	A, [HL+B]	2	2	–	A ←→ (HL+B)	
		A, ES:[HL+B]	3	3	–	A ←→ ((ES, HL)+B)	
		A, [HL+C]	2	2	–	A ←→ (HL+C)	
		A, ES:[HL+C]	3	3	–	A ←→ ((ES, HL)+C)	
	ONEB	A	1	1	–	A ← 01H	
		X	1	1	–	X ← 01H	
		B	1	1	–	B ← 01H	
		C	1	1	–	C ← 01H	
		!addr16	3	1	–	(addr16) ← 01H	
		ES:!addr16	4	2	–	(ES, addr16) ← 01H	
		saddr	2	1	–	(saddr) ← 01H	
	CLRB	A	1	1	–	A ← 00H	
		X	1	1	–	X ← 00H	
		B	1	1	–	B ← 00H	
		C	1	1	–	C ← 00H	
		!addr16	3	1	–	(addr16) ← 00H	
		ES:!addr16	4	2	–	(ES,addr16) ← 00H	
		saddr	2	1	–	(saddr) ← 00H	
	MOVS	[HL+byte], X	3	1	–	(HL+byte) ← X	× ×
		ES:[HL+byte], X	4	2	–	(ES, HL+byte) ← X	× ×
16-bit data transfer	MOVW	rp, #word	3	1	–	rp ← word	
		saddrp, #word	4	1	–	(saddrp) ← word	
		sfrp, #word	4	1	–	sfrp ← word	
		AX, rp Note 3	1	1	–	AX ← rp	
		rp, AX Note 3	1	1	–	rp ← AX	
		AX, !addr16	3	1	4	AX ← (addr16)	
		!addr16, AX	3	1	–	(addr16) ← AX	
		AX, ES:!addr16	4	2	5	AX ← (ES, addr16)	
		ES:!addr16, AX	4	2	–	(ES, addr16) ← AX	
		AX, saddrp	2	1	–	AX ← (saddrp)	
		saddrp, AX	2	1	–	(saddrp) ← AX	
		AX, sfrp	2	1	–	AX ← sfrp	
		sfrp, AX	2	1	–	sfrp ← AX	

Notes 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

2. Number of CPU clocks (f_{CLK}) when the code flash area is accessed.

3. Except rp = AX

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.

41.6.2 24-bit ΔΣ A/D converter characteristics

(1) Reference voltage

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD}[Note] ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Internal reference voltage	V_{AVRTO}			0.8		V
<R> Temperature coefficient for internal reference voltage	dREF/dt	0.47 μF capacitor connected to AREGC, AVRT, and AVCM pins		10		ppm/°C

Note Either V_{DD} or VBAT is selected by the battery backup function.

(2) Analog input

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD}[Note] ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage range (differential voltage)	V_{AIN}	x1 gain	–500		500	mV
		x2 gain	–250		250	
		x4 gain	–125		125	
		x8 gain	–62.5		62.5	
		x16 gain	–31.25		31.25	
		x32 gain (for current channels)	–15.625		15.625	
Input gain	ainGAIN	x1 gain		1		dB
		x2 gain		2		
		x4 gain		4		
		x8 gain		8		
		x16 gain		16		
		x32 gain (for current channels)		32		
Input impedance	ainRIN	Differential voltage	150	360		kΩ
		Single-ended voltage	100	240		

Note Either V_{DD} or VBAT is selected by the battery backup function.

41.8 LCD Characteristics

41.8.1 Resistance division method

(1) Static display mode

(T_A = –40 to +85°C, V_{L4} (MIN.) ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD}[Note] ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.0		V_{DD}[Note]	V

Note Either V_{DD} or VBAT is selected by the battery backup function.

(2) 1/2 bias method, 1/4 bias method

(T_A = –40 to +85°C, V_{L4} (MIN.) ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD}[Note] ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.7		V_{DD}[Note]	V

Note Either V_{DD} or VBAT is selected by the battery backup function.

(3) 1/3 bias method

(T_A = –40 to +85°C, V_{L4} (MIN.) ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD}[Note] ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.5		V_{DD}[Note]	V

Note Either V_{DD} or VBAT is selected by the battery backup function.