Welcome to E-XFL.COM

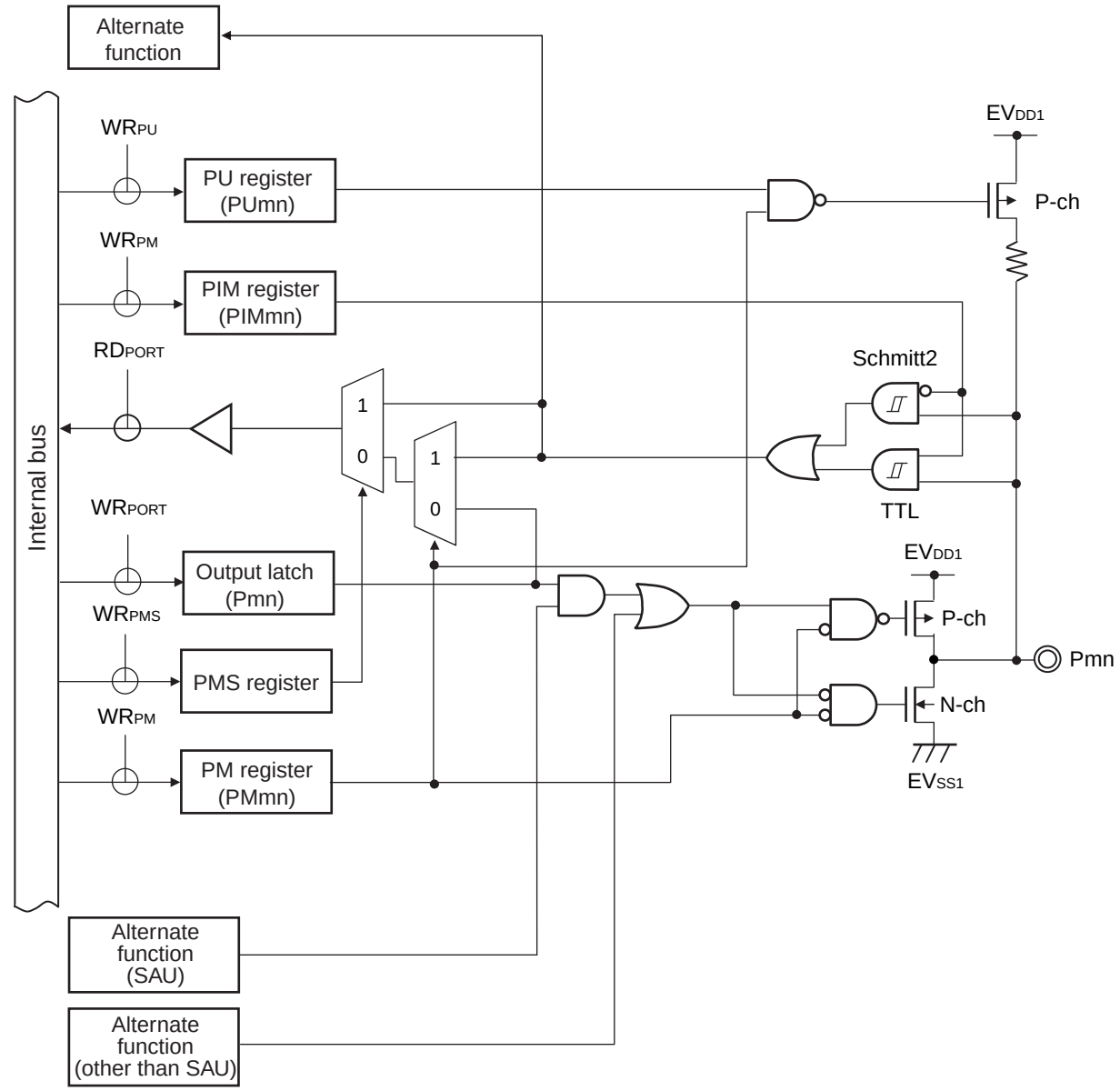
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, IrDA, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 5.5V
Data Converters	A/D 4x10b, 3x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10nmjdfb-30

Figure 2-12. Pin Block Diagram for Pin Type 8-1-3



Remarks 1. For alternate functions, see **2.1 Port Function**.

2. SAU: Serial array unit

Table 4-6. Setting Examples of Registers and Output Latches When Using Alternate Function (7/10)

Pin Name	Used Function		PIOR0×	POM××	PM××	P××	PFSEG×× (ISCVL3, ISCCAP)[Note]	Alternate Function Output		64-pin	80-pin	100-pin
	Function Name	I/O						SAU Output Function	Other than SAU			
P61	P61	Input	–	_	1	×	–	–	–	√	√	√
		N-ch open drain output (6 V tolerance)	×	_	0	0/1	–	–	SDAA0 = 0 (TO01) = 0			
	SDAA0	I/O	×	_	0	0	–	–	(TO01) = 0			
	(TI01)	Input	PIOR00 = 1	_	1	×	–	–	–			
	(TO01)	Output	PIOR00 = 1	_	0	0	–	–	SDAA0 = 0			
P62	P62	Input	–	_	1	×	–	–	–	√	√	√
		N-ch open drain output (6 V tolerance)	×	_	0	0/1	–	–	(TO02) = 0 (RTCOUT) = 0			
	(TI02)	Input	PIOR00 = 1	_	1	×	–	–	–			
	(TO02)	Output	PIOR00 = 1	_	0	0	–	–	(RTCOUT) = 0			
	(RTCOUT)	Output	PIOR03 = 1	_	0	0	–	–	(TO02) = 0			
P70	P70	Input	–	_	1	×	0	–	–	√	√	√
		Output	×	_	0	0/1	0	–	–			
	SEG16	Output	×	_	0	0	1	–	–			
	KR0	Input	×	_	1	×	0	–	–			
	(INTP0)	Input	PIOR04 = 1	_	1	×	0	–	–			
P71	P71	Input	–	_	1	×	0	–	–	√	√	√
		Output	×	_	0	0/1	0	–	–			
	SEG17	Output	×	_	0	0	1	–	–			
	KR1	Input	×	_	1	×	0	–	–			
	(INTP1)	Input	PIOR04 = 1	_	1	×	0	–	–			
P72	P72	Input	–	_	1	×	0	–	–	√	√	√
		Output	×	_	0	0/1	0	–	–			
	KR2	Input	×	_	1	×	0	–	–			
	SEG18	Output	×	_	0	0	1	–	–			
	(INTP2)	Input	PIOR04 = 1	_	1	×	0	–	–			
	(TI01)	Input	PIOR00 = 1	_	1	×	0	–	–	√	–	–
	(TO01)	Output	PIOR00 = 1	_	0	0	0	–	–			
P73	P73	Input	–	_	1	×	0	–	–	√	√	√
		Output	×	_	0	0/1	0	–	–			
	KR3	Input	×	_	1	×	0	–	–			
	SEG19	Output	×	_	0	0	1	–	–			
	(INTP3)	Input	PIOR04 = 1	_	1	×	0	–	–			
	(PCLBUZ1)	Output	PIOR03 = 1	_	1	0	0	–	–	√	–	–
P74	P74	Input	–	_	1	×	0	–	–	√	√	√
		Output	×	_	0	0/1	0	–	(PCLBUZ0) = 0			
	KR4	Input	×	_	1	×	0	–	–			
	SEG20	Output	×	_	0	0	1	–	–			
	(INTP4)	Input	PIOR04 = 1	_	1	×	0	–	–			
	(PCLBUZ0)	Output	PIOR03 = 1	_	0	0	0	–	–	√	–	–
P75	P75	Input	–	_	1	×	0	–	–	–	√	√
		Output	×	_	0	0/1	0	–	–			
	KR5	Input	×	_	1	×	0	–	–			
	SEG21	Output	×	_	0	0	1	–	–			
	(INTP5)	Input	PIOR04 = 1	_	1	×	0	–	–			

Note ISCVL3 and ISCCAP are registers that correspond to P125, and P126 and P127, respectively.

Figure 6 - 7 Format of Oscillation stabilization time counter status register (OSTC)

Address: FFFA2H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
OSTC	MOST8	MOST9	MOST 10	MOST 11	MOST 13	MOST 15	MOST 17	MOST 18

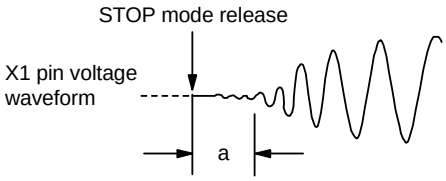
MOST 8	MOST 9	MOST 10	MOST 11	MOST 13	MOST 15	MOST 17	MOST 18	Oscillation stabilization time status		
									fx = 10 MHz	fx = 20 MHz
0	0	0	0	0	0	0	0	2^8/fx max.	25.6 μs max.	12.8 μs max.
1	0	0	0	0	0	0	0	2^8/fx min.	25.6 μs min.	12.8 μs min.
1	1	0	0	0	0	0	0	2^9/fx min.	51.2 μs min.	25.6 μs min.
1	1	1	0	0	0	0	0	2^{10}/fx min.	102 μs min.	51.2 μs min.
1	1	1	1	0	0	0	0	2^{11}/fx min.	204 μs min.	102 μs min.
1	1	1	1	1	0	0	0	2^{13}/fx min.	819 μs min.	409 μs min.
1	1	1	1	1	1	0	0	2^{15}/fx min.	3.27 ms min.	1.63 ms min.
1	1	1	1	1	1	1	0	2^{17}/fx min.	13.1 ms min.	6.55 ms min.
1	1	1	1	1	1	1	1	2^{18}/fx min.	26.2 ms min.	13.1 ms min.

Caution 1. After the above time has elapsed, the bits are set to 1 in order from the MOST8 bit and remain 1.

Caution 2. The oscillation stabilization time counter counts up to the oscillation stabilization time set by the oscillation stabilization time select register (OSTS).
In the following cases, set the oscillation stabilization time of the OSTS register to the value greater than the count value which is to be checked by the OSTC register.

- **If the X1 clock starts oscillation while the high-speed on-chip oscillator clock or subsystem clock is being used as the CPU clock.**
- **If the STOP mode is entered and then released while the high-speed on-chip oscillator clock is being used as the CPU clock with the X1 clock oscillating.**
  (Note, therefore, that only the status up to the oscillation stabilization time set by the OSTS register is set to the OSTC register after the STOP mode is released.)

Caution 3. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark fx: X1 clock oscillation frequency

6.6.7 Time required for switchover of CPU clock and main system clock

By setting bits 0, 4, 6 (MCM0, MCM1,CSS) of the system clock control register (CKC), the CPU clock can be switched (between the main system clock and the subsystem clock), main system clock can be switched (between the on-chip oscillator clock and the high-speed system clock), and on-chip oscillator clock can be switched (between the high-speed on-chip oscillator clock and the middle-speed on-chip oscillator clock).

The actual switchover operation is not performed immediately after rewriting to the CKC register; operation continues on the pre-switchover clock for several clocks (see **Tables 6 - 5** to **6 - 8**).

Whether the CPU is operating on the main system clock or the subsystem clock can be ascertained using bit 7 (CLS) of the CKC register. Whether the main system clock is operating on the high-speed system clock or main on-chip oscillator clock or PLL clock can be ascertained using bit 5 (MCS) of the CKC register. Whether the main system clock is operating on the high-speed on-chip oscillator clock or PLL clock can be ascertained using bit 7 (CKSTR) of the MCKC register. Whether the main on-chip oscillator clock is operating on the high-speed on-chip oscillator clock or middle-speed on-chip oscillator clock can be ascertained using bit 1 (MCS1) of the CKC register.

When the CPU clock is switched, the peripheral hardware clock is also switched.

Table 6 - 5 Maximum Time Required for Main System Clock Switchover

Clock A	Switching directions	Clock B	Remark
f_{OCO}	⟷	f_{MX}	See **Table 6 - 6**
f_{IH}	⟷	f_{IM}	See **Table 6 - 7**
f_{MAIN}	⟷	f_{SUB}	See **Table 6 - 8**

Table 6 - 6 Maximum Number of Clocks Required for f_{OCO} ↔ f_{MX}

Set Value Before Switchover		Set Value After Switchover	
MCM0		MCM0	
		0 ($f_{MAIN} = f_{OCO}$)	1 ($f_{MAIN} = f_{MX}$)
0 ($f_{MAIN} = f_{OCO}$)	$f_{MX} \geq f_{OCO}$		2 clocks
	$f_{MX} < f_{OCO}$		2 f_{OCO}/f_{MX} clocks
1 ($f_{MAIN} = f_{MX}$)	$f_{MX} \geq f_{OCO}$	2 f_{MX}/f_{OCO} clocks	
	$f_{MX} < f_{OCO}$	2 clocks	

Table 6 - 7 Maximum Number of Clocks Required for f_{IH} ↔ f_{IM}

Set Value Before Switchover		Set Value After Switchover	
MCM1		MCM1	
		0 ($f_{MAIN} = f_{IH}$)	1 ($f_{MAIN} = f_{IM}$)
0 ($f_{MAIN} = f_{IH}$)	$f_{IM} \geq f_{IH}$		2 clocks
	$f_{IM} < f_{IH}$		1 + f_{IH}/f_{IM} clock
1 ($f_{MAIN} = f_{IM}$)	$f_{IM} \geq f_{IH}$	2 f_{IM}/f_{IH} clocks	
	$f_{IM} < f_{IH}$	2 clocks	

9.2.23 RCR5 guard register (RCR5GD)

The RCR5GD register is used to control the guard function for RTC control register 5 (RCR5).

Figure 9 - 37 Format of RCR5 guard register 5 (RCR5GD)

Address: F05B9H After reset: 00H W

Symbol	7	6	5	4	3	2	1	0
RCR5GD	RCR5GD							

RCR5GD	Control of guard function for RTC control register 5 (RCR5)
When writing consecutively in order to 00H, 72H, 64H, RTC control register 5 (RCR5) can be accessed. To activate the guard function, write 00H once.	

Caution This register can only be accessed with an 8-bit memory manipulation instruction.
And, this register is a write-only register. When this register is read, the read value is always 0.

10.3.6 Frequency measurement clock select register (FMCKS)

The FMCKS register is used to select the operating clock and frequency count clock to be input to the frequency measurement circuit.

The FMCKS register can be used by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears the FMCKS register to 00H.

Figure 10 - 8 Format of Frequency measurement clock select register (FMCKS)

Address: F007AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
FMCKS	0	0	0	0	0	0	FMCKSEL1	FMCKSEL0

FMCKSEL1	FMCKSEL0	Selection of frequency count clock
0	0	f_{MX} selected
0	1	f_{IM} selected
1	×	f_{IH} selected

11.3.2 Peripheral reset control register 2 (PRR2)

This register is used for individual reset control of each peripheral hardware.

This MCU controls reset and reset release of each peripheral hardware supported by the PRR2 register.

To reset the 12-bit interval timer, be sure to set bit 7 (TMKARES) to 1.

The PRR2 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 11 - 3 Format of Peripheral reset control register 2 (PRR2)

Address: F00FDH After reset: 00H R/W

Symbol	<7>	<6>	5	4	3	<2>	1	0
PRR2	TMKARES	OSDCRES	0	0	0	MACRES	0	0

TMKARES	Reset control of 12-bit interval timer
0	12-bit interval timer reset release
1	12-bit interval timer reset state

Figure 13 - 2 Format of Clock output select registers n (CKSn)

Address: FFFA5H (CKS0), FFFA6H (CKS1) After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
CKSn	PCLOEn	0	0	0	CSELn	CCSn2	CCSn1	CCSn0

PCLOEn	PCLBUZn pin output enable/disable specification
0	Output disable (default)
1	Output enable

CSELn	CCSn2	CCSn1	CCSn0	PCLBUZn pin output clock selection				
					f_{MAIN} = 5 MHz	f_{MAIN} = 10 MHz	f_{MAIN} = 20 MHz	f_{MAIN} = 24 MHz
0	0	0	0	f_{MAIN}	5 MHz	10 MHz Note	Setting prohibited Note	Setting prohibited Note
0	0	0	1	$f_{MAIN}/2$	2.5 MHz	5 MHz	10 MHz Note	Setting prohibited Note
0	0	1	0	$f_{MAIN}/2^2$	1.25 MHz	2.5 MHz	5 MHz	6 MHz
0	0	1	1	$f_{MAIN}/2^3$	625 kHz	1.25 MHz	2.5 MHz	3 MHz
0	1	0	0	$f_{MAIN}/2^4$	312.5 kHz	625 kHz	1.25 MHz	1.5 MHz
0	1	0	1	$f_{MAIN}/2^{11}$	2.44 kHz	4.88 kHz	9.77 kHz	11.7 kHz
0	1	1	0	$f_{MAIN}/2^{12}$	1.22 kHz	2.44 kHz	4.88 kHz	5.86 kHz
0	1	1	1	$f_{MAIN}/2^{13}$	610 Hz	1.22 kHz	2.44 kHz	2.93 kHz
1	0	0	0	f_{SX}	32.768 kHz			
1	0	0	1	$f_{SX}/2$	16.384 kHz			
1	0	1	0	$f_{SX}/2^2$	8.192 kHz			
1	0	1	1	$f_{SX}/2^3$	4.096 kHz			
1	1	0	0	$f_{SX}/2^4$	2.048 kHz			
1	1	0	1	$f_{SX}/2^5$	1.024 kHz			
1	1	1	0	$f_{SX}/2^6$	512 Hz			
1	1	1	1	$f_{SX}/2^7$	256 Hz			

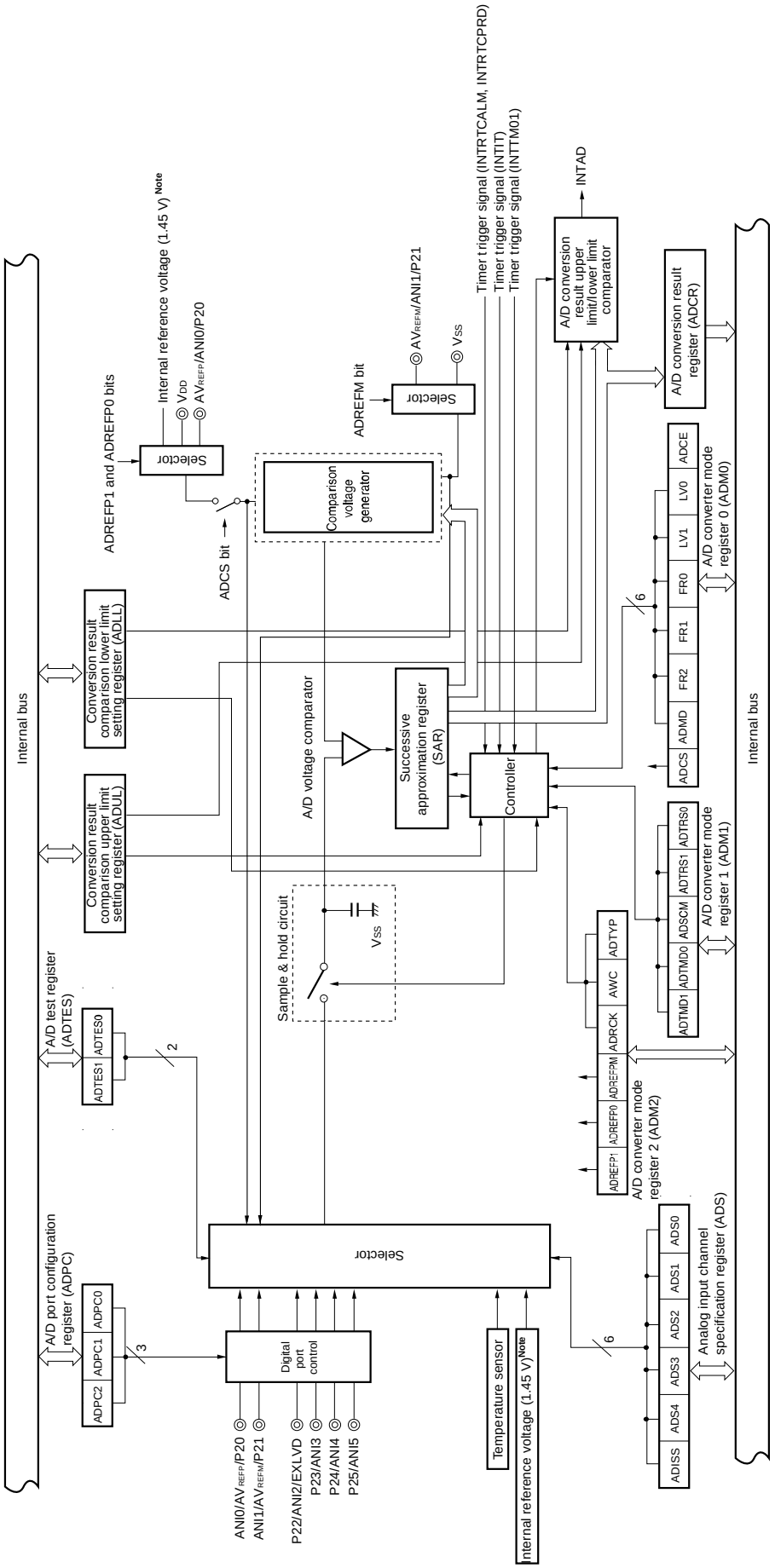
Note Use the output clock within a range of 16 MHz. See **41.4 AC Characteristics** for details.

Caution Change the output clock after disabling clock output (PCLOEn = 0).

Remark 1. n = 0, 1

Remark 2. f_{MAIN}: Main system clock frequency
f_{SX}: Sub clock

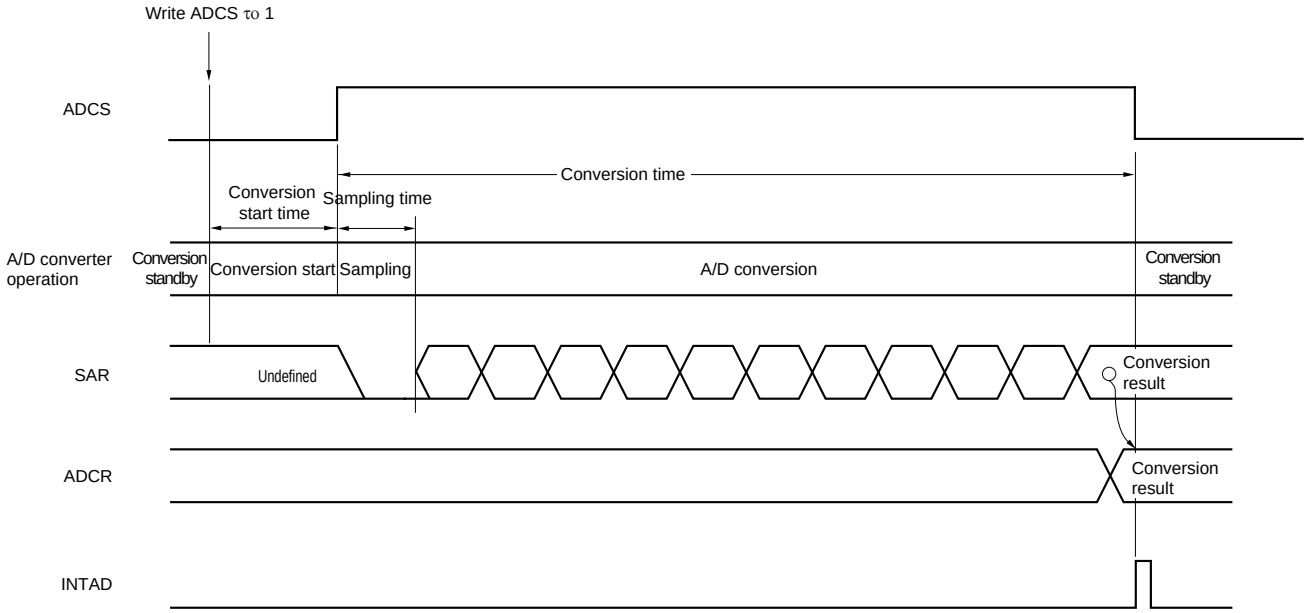
<R> **Figure 15-1. Block Diagram of A/D Converter**



Remark Analog input pin for figure 15-1 when a 100-pin product is used.

Note When using an internal reference voltage, it must be used in HS mode.
The minimum operating voltage in HS mode is 2.4 V.
Use an external reference voltage if you need to operate at 2.4 V or less.

Figure 15-16. Conversion Operation of A/D Converter (Software Trigger Mode)



In one-shot conversion mode, the ADCS bit is automatically cleared to 0 after completion of A/D conversion.

In sequential conversion mode, A/D conversion operations proceed continuously until the software clears bit 7 (ADCS) of the A/D converter mode register 0 (ADM0) to 0.

When the value of the analog input channel specification register (ADS) is rewritten or overwritten during conversion, the current A/D conversion is interrupted, and A/D conversion is performed on the analog input newly specified in the ADS register. The partially converted data is discarded.

Reset signal generation clears the A/D conversion result register (ADCR, ADCRH) to 0000H or 00H.

15.10 Cautions for A/D Converter

(1) Operating current in STOP mode

Shift to STOP mode after stopping the A/D converter (by setting bit 7 (ADCS) of A/D converter mode register 0 (ADM0) to 0). The operating current can be reduced by setting bit 0 (ADCE) of the ADM0 register to 0 at the same time.

To restart from the standby status, clear bit 0 (ADIF) of interrupt request flag register 1H (IF1H) to 0 and start operation.

(2) Input range of ANI0 to ANI5 pins

Observe the rated range of the ANI0 to ANI5 pins input voltage. If a voltage exceeding V_{DD} and AV_{REFP} or below V_{SS} and AV_{REFM} (even in the range of absolute maximum ratings) is input to an analog input channel, the converted value of that channel becomes undefined. In addition, the converted values of the other channels may also be affected.

When internal reference voltage (1.45 V) is selected reference voltage for the + side of the A/D converter, do not input voltage exceeding internal reference voltage (1.45 V) to a pin selected by the ADS register. However, it is no problem that a voltage exceeding the internal reference voltage (1.45 V) is input to a pin not selected by the ADS register.

Caution Internal reference voltage (1.45 V) can be used only in HS (high-speed main) mode.

(3) Conflicting operations

<1> Conflict between the A/D conversion result register (ADCR, ADCRH) write and the ADCR or ADCRH register read by instruction upon the end of conversion

The ADCR or ADCRH register read has priority. After the read operation, the new conversion result is written to the ADCR or ADCRH registers.

<2> Conflict between the ADCR or ADCRH register write and the A/D converter mode register 0 (ADM0) write, the analog input channel specification register (ADS), or A/D port configuration register (ADPC) write upon the end of conversion

The ADM0, ADS, or ADPC registers write has priority. The ADCR or ADCRH register write is not performed, nor is the conversion end interrupt signal (INTAD) generated.

(4) Noise countermeasures

To maintain the 10-bit resolution, attention must be paid to noise input to the AV_{REFP}, V_{DD}, ANI0 to ANI5 pins.

<1> Connect a capacitor with a low equivalent resistance and a good frequency response (capacitance of about 0.01 μF) via the shortest possible run of relatively thick wiring to the power supply.

<2> The higher the output impedance of the analog input source, the greater the influence. To reduce the noise, connecting an external capacitor as shown in Figure 15-45 is recommended.

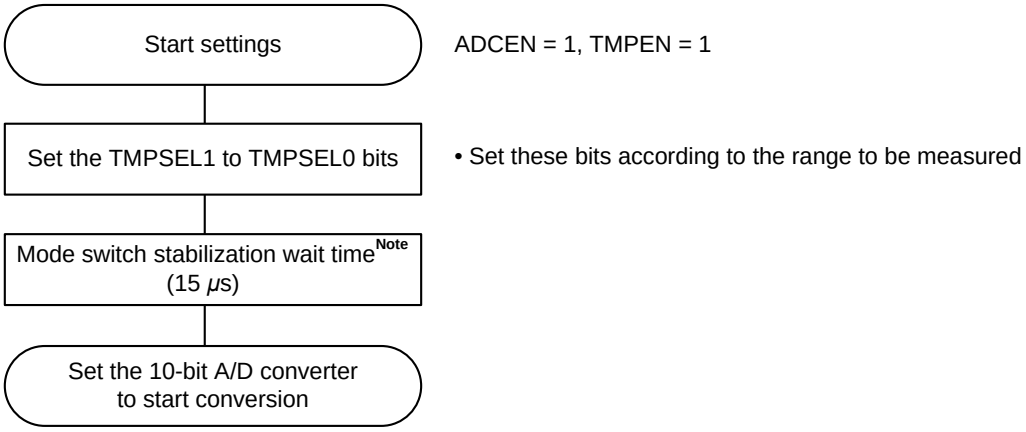
<3> Do not switch these pins with other pins during conversion.

<4> The accuracy is improved if the HALT mode is set immediately after the start of conversion.

16.3.2 Switching modes

Figure 16-7 shows the setting flowchart when switching mode of temperature sensor.

Figure 16-7. Setting Flowchart When Switching Mode of Temperature Sensor



Note Mode switch stabilization wait time is required until the A/D converter starts conversion.

Caution Select internal reference voltage for 10-bit A/D converter.

DSADZCEGNn bit, DSADZCEGPn bit (n = 0, 1)

These bits are used to set the valid edges that generate a zero-cross detection interrupt to the DF output. The DF output zero-cross detection conditions and relationships between waveforms of the DF output and the DSADZCn bit are shown in the Figures 17-8 to 17-11.

Table 17-4. Zero-cross Detection Conditions for the DF Output

DSADZC EGPn	DSADZC EGNn	Detection Edge Selection
0	0	Zero-cross detection disabled
0	1	Falling edge of DSADZCn
1	0	Rising edge of DSADZCn
1	1	Both rising and falling edges of DSADZCn

Figure 17-8. INTDSADZCn Interrupt Generation Timing
(Pulse output: DSADZCMDn = 0, DSADZCEGNn = 0, DSADZCEGPn = 0)

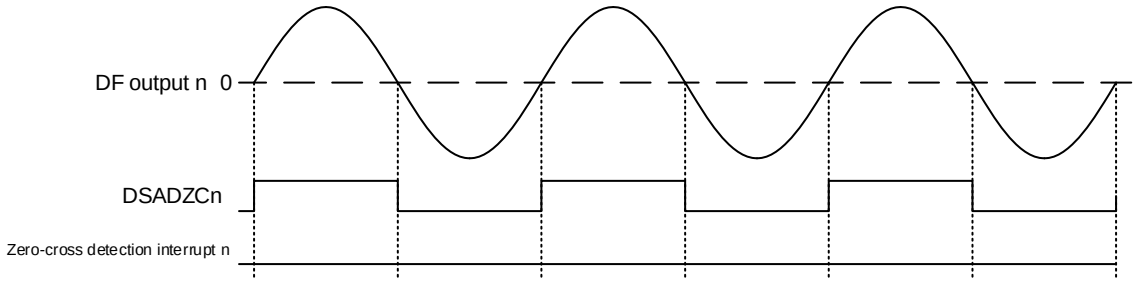
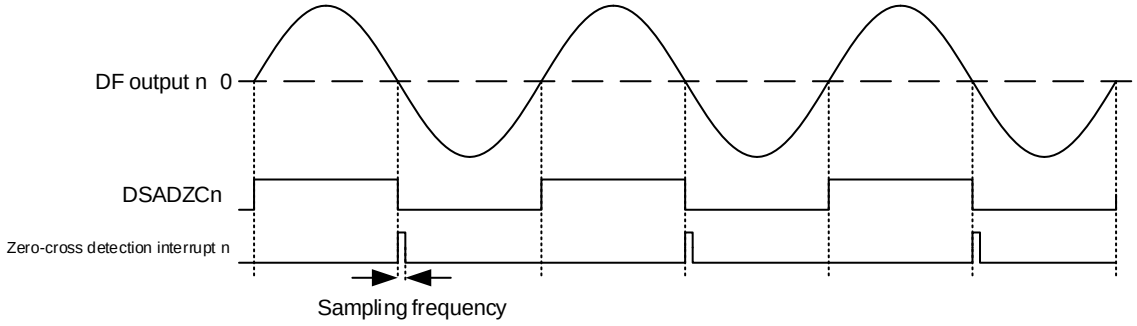


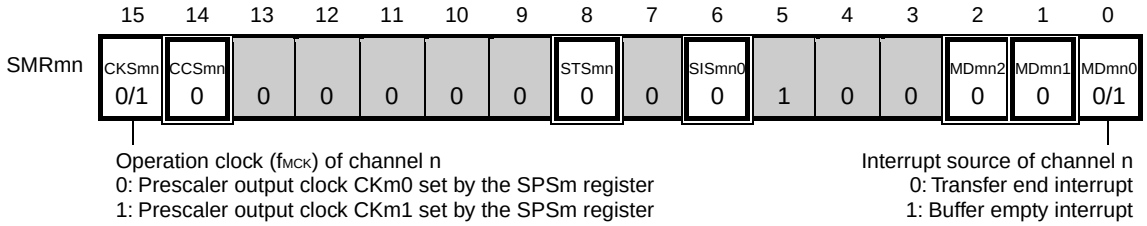
Figure 17-9. INTDSADZCn Interrupt Generation Timing
(Pulse output: DSADZCMDn = 0, DSADZCEGNn = 1, DSADZCEGPn = 0)



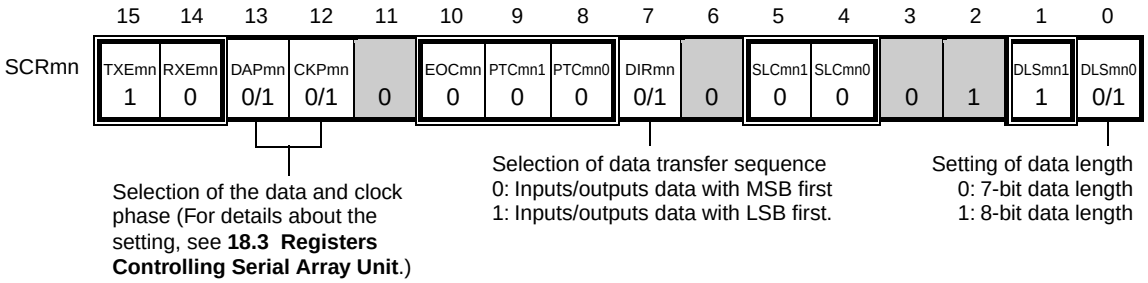
(1) Register setting

Figure 18-26. Example of Contents of Registers for Master Transmission of 3-Wire Serial I/O (CSI00, CSI10, CSI30) (1/2)

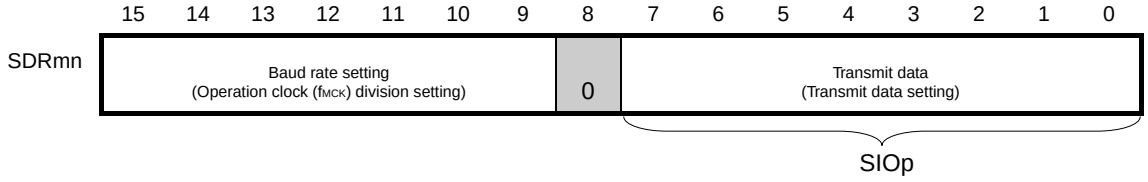
(a) Serial mode register mn (SMRmn)



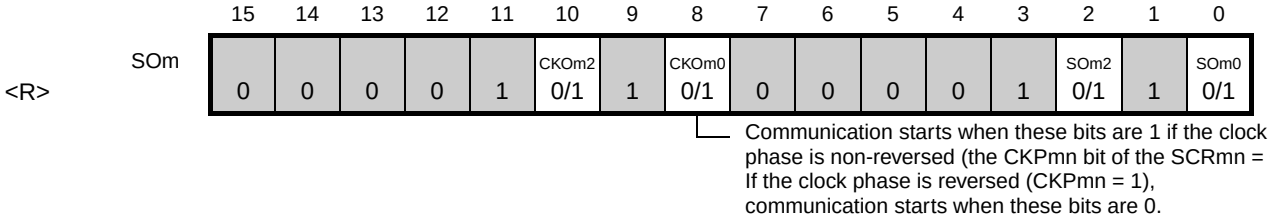
(b) Serial communication operation setting register mn (SCRmn)



(c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)



(d) Serial output register m (SOm) … Sets only the bits of the target channel.



<R>

<R>

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: CSI number (p = 00, 10, 30), mn = 00, 02, 12

2. ☐: Setting is fixed in the CSI master transmission mode, ▒: Setting disabled (set to the initial value)
0/1: Set to 0 or 1 depending on the usage of the user

(2) Baud rate error during transmission

The baud rate error of UART (UART0 to UART3) communication during transmission can be calculated by the following expression. Make sure that the baud rate at the transmission side is within the permissible baud rate range at the reception side.

(Baud rate error) = (Calculated baud rate value) ÷ (Target baud rate) × 100 − 100 [%]

Here is an example of setting a UART baud rate at f_{CLK} = 24 MHz.

UART Baud Rate (Target Baud Rate)	f_{CLK} = 24 MHz			
	Operation Clock (f_{MCK})	SDRmn[15:9]	Calculated Baud Rate	Error from Target Baud Rate
300 bps	$f_{CLK}/2^9$	77	300.48 bps	+0.16 %
600 bps	$f_{CLK}/2^8$	77	600.96 bps	+0.16 %
1200 bps	$f_{CLK}/2^7$	77	1201.92 bps	+0.16 %
2400 bps	$f_{CLK}/2^6$	77	2403.85 bps	+0.16 %
4800 bps	$f_{CLK}/2^5$	77	4807.69 bps	+0.16 %
9600 bps	$f_{CLK}/2^4$	77	9615.38 bps	+0.16 %
19200 bps	$f_{CLK}/2^3$	77	19230.8 bps	+0.16 %
31250 bps	$f_{CLK}/2^3$	47	31250.0 bps	±0.0 %
38400 bps	$f_{CLK}/2^2$	77	38461.5 bps	+0.16 %
76800 bps	$f_{CLK}/2$	77	76923.1 bps	+0.16 %
153600 bps	f_{CLK}	77	153846 bps	+0.16 %
312500 bps	f_{CLK}	37	315789 bps	+1.05 %

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 02, 10, 12

(b) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop

(i) When WTIMn = 0 (after restart, matches with SVAn)

▲1: IICSn = 0001×110B
▲2: IICSn = 0001×000B
▲3: IICSn = 0001×110B
▲4: IICSn = 0001×000B
△5: IICSn = 00000001B

Remark ▲: Always generated
△: Generated only when SPIEn = 1
×: Don't care

(ii) When WTIMn = 1 (after restart, matches with SVAn)

▲1: IICSn = 0001×110B
▲2: IICSn = 0001××00B
▲3: IICSn = 0001×110B
▲4: IICSn = 0001××00B
△5: IICSn = 00000001B

Remark ▲: Always generated
△: Generated only when SPIEn = 1
×: Don't care

Remark n = 0

CHAPTER 21 LCD CONTROLLER/DRIVER

The number of LCD display function pins of the RL78/I1C differs depending on the product. The following table shows the number of pins of each product.

Table 21-1. Number of LCD Display Function Pins of Each Product

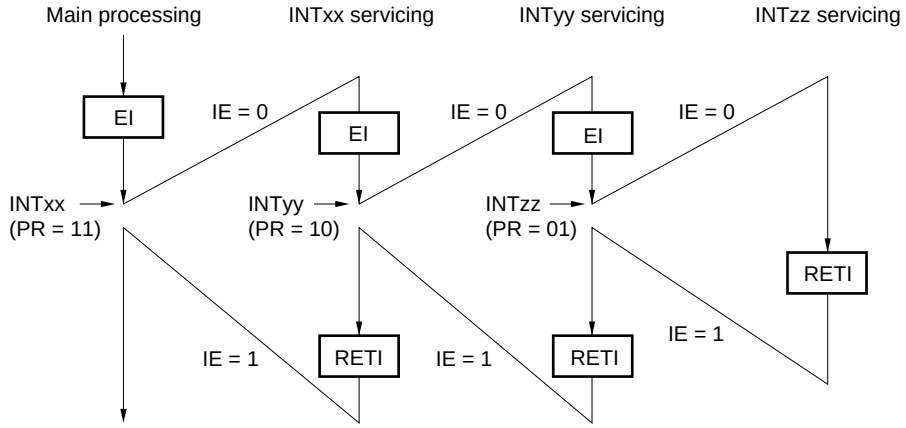
<R>

Item		RL78/I1C																									
		64 pins (R5F10NLx (x = G, E))								80 pins (R5F10NMx (x = J, G, E))								100 pins (R5F10NPx (x = J, G))							
LCD controller/driver		Segment signal outputs: 19 (15)Note Common signal outputs: 8								Segment signal outputs: 34 (30)Note Common signal outputs: 8								Segment signal outputs: 42 (38)Note Common signal outputs: 8							
Multiplexed I/O port		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Segment	P0	–	–	–	–	–	–	–	–	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32	–	–	–	–	–	–	–	–	–	–	–	–
	P1	SEG 11	SEG 10	SEG 9	SEG 8	SEG 7	SEG 6	SEG 5	SEG 4	SEG 11	SEG 10	SEG 9	SEG 8	SEG 7	SEG 6	SEG 5	SEG 4	SEG 11	SEG 10	SEG 9	SEG 8	SEG 7	SEG 6	SEG 5	SEG 4
	P3	–	–	–	–	–	–	SEG 25	SEG 24	–	–	–	–	SEG 27	SEG 26	SEG 25	SEG 24	SEG 31	SEG 30	SEG 29	SEG 28	SEG 27	SEG 26	SEG 25	SEG 24
	P5	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	SEG 39	SEG 38	SEG 37	SEG 36	SEG 35	SEG 34	SEG 33	SEG 32
	P7	–	–	–	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16	SEG 23	SEG 22	SEG 21	SEG 20	SEG 19	SEG 18	SEG 17	SEG 16
	P8	–	–	–	–	–	–	–	–	–	–	–	–	SEG 15	SEG 14	SEG 13	SEG 12	–	–	SEG 41	SEG 40	SEG 15	SEG 14	SEG 13	SEG 12
Alternate relationship between COM signal output pins and I/O pots		–																							
Alternate relationship between COM signal output pins and LCD display function pins	COM 4	SEG0								SEG0								SEG0							
	COM 5	SEG1								SEG1								SEG1							
	COM 6	SEG2								SEG2								SEG2							
	COM 7	SEG3								SEG3								SEG3							

Note ( ) indicates the number of signal output pins when 8 com is used.

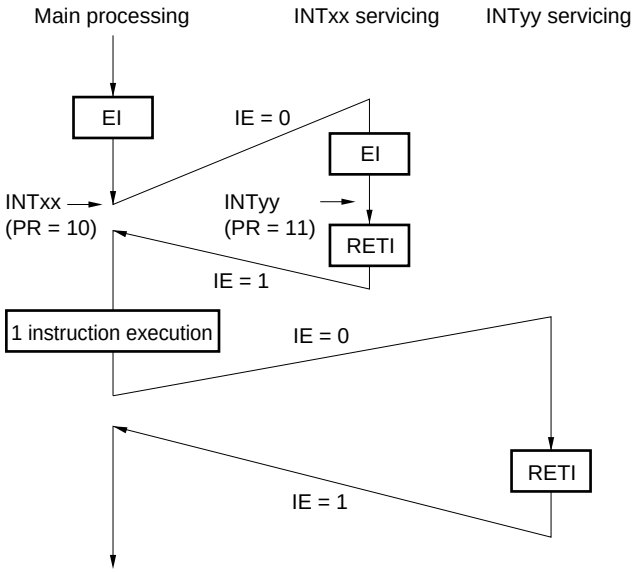
Figure 24-10. Examples of Multiple Interrupt Servicing (1/2)

Example 1. Multiple interrupt servicing occurs twice



During servicing of interrupt INTxx, two interrupt requests, INTyy and INTzz, are acknowledged, and multiple interrupt servicing takes place. Before each interrupt request is acknowledged, the EI instruction must always be issued to enable interrupt request acknowledgment.

Example 2. Multiple interrupt servicing does not occur due to priority control



Interrupt request INTyy issued during servicing of interrupt INTxx is not acknowledged because its priority is lower than that of INTxx, and multiple interrupt servicing does not take place. The INTyy interrupt request is held pending, and is acknowledged following execution of one main processing instruction.

PR = 00: Specify level 0 with ××PR1× = 0, ××PR0× = 0 (higher priority level)
PR = 01: Specify level 1 with ××PR1× = 0, ××PR0× = 1
PR = 10: Specify level 2 with ××PR1× = 1, ××PR0× = 0
PR = 11: Specify level 3 with ××PR1× = 1, ××PR0× = 1 (lower priority level)
IE = 0: Interrupt request acknowledgment is disabled
IE = 1: Interrupt request acknowledgment is enabled.

36.4.3 Selecting communication mode

Communication mode of the RL78 microcontroller as follows.

Table 36 - 6 Communication Modes

Communication Mode	Standard Setting Note 1				Pins Used
	Port	Speed Note 2	Frequency	Multiply Rate	
1-line mode (when flash memory programmer is used, or when external device is used)	UART	115200 bps, 250000 bps, 500000 bps, 1 Mbps	—	—	TOOL0
Dedicated UART (when external device is used)	UART	115200 bps, 250000 bps, 500000 bps, 1 Mbps	—	—	TOOLTxD, TOOLRxD

Note 1. Selection items for Standard settings on GUI of the flash memory programmer.

Note 2. Because factors other than the baud rate error, such as the signal waveform slew, also affect UART communication, thoroughly evaluate the slew as well as the baud rate error.

Table 40-5. Operation List (3/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag
				Note 1	Note 2		Z AC CY
8-bit data transfer	MOV	A, [HL+B]	2	1	4	A ← (HL + B)	
		[HL+B], A	2	1	–	(HL + B) ← A	
		A, ES:[HL+B]	3	2	5	A ← ((ES, HL) + B)	
		ES:[HL+B], A	3	2	–	((ES, HL) + B) ← A	
		A, [HL+C]	2	1	4	A ← (HL + C)	
		[HL+C], A	2	1	–	(HL + C) ← A	
		A, ES:[HL+C]	3	2	5	A ← ((ES, HL) + C)	
		ES:[HL+C], A	3	2	–	((ES, HL) + C) ← A	
		X, !addr16	3	1	4	X ← (addr16)	
		X, ES:!addr16	4	2	5	X ← (ES, addr16)	
		X, saddr	2	1	–	X ← (saddr)	
		B, !addr16	3	1	4	B ← (addr16)	
		B, ES:!addr16	4	2	5	B ← (ES, addr16)	
		B, saddr	2	1	–	B ← (saddr)	
		C, !addr16	3	1	4	C ← (addr16)	
		C, ES:!addr16	4	2	5	C ← (ES, addr16)	
		C, saddr	2	1	–	C ← (saddr)	
		ES, saddr	3	1	–	ES ← (saddr)	
	XCH	A, r Note 3	1 (r = X) 2 (other than r = X)	1	–	A ←→ r	
		A, !addr16	4	2	–	A ←→ (addr16)	
		A, ES:!addr16	5	3	–	A ←→ (ES, addr16)	
		A, saddr	3	2	–	A ←→ (saddr)	
		A, sfr	3	2	–	A ←→ sfr	
		A, [DE]	2	2	–	A ←→ (DE)	
		A, ES:[DE]	3	3	–	A ←→ (ES, DE)	
		A, [HL]	2	2	–	A ←→ (HL)	
		A, ES:[HL]	3	3	–	A ←→ (ES, HL)	
		A, [DE+byte]	3	2	–	A ←→ (DE + byte)	
		A, ES:[DE+byte]	4	3	–	A ←→ ((ES, DE) + byte)	
		A, [HL+byte]	3	2	–	A ←→ (HL + byte)	
		A, ES:[HL+byte]	4	3	–	A ←→ ((ES, HL) + byte)	

Notes 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

2. Number of CPU clocks (f_{CLK}) when the code flash area is accessed.

3. Except r = A

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.