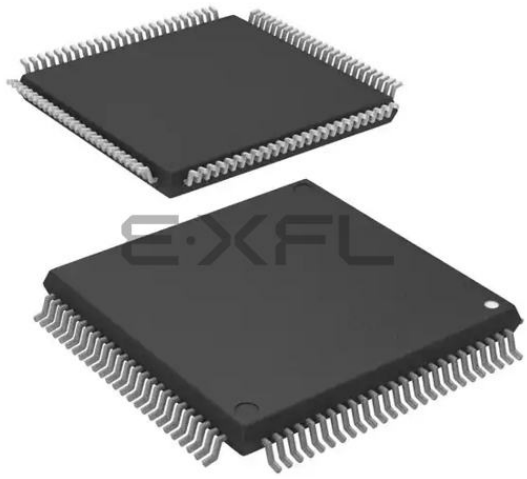
Renesas Electronics America Inc - R5F10NPGDFB#30 Datasheet



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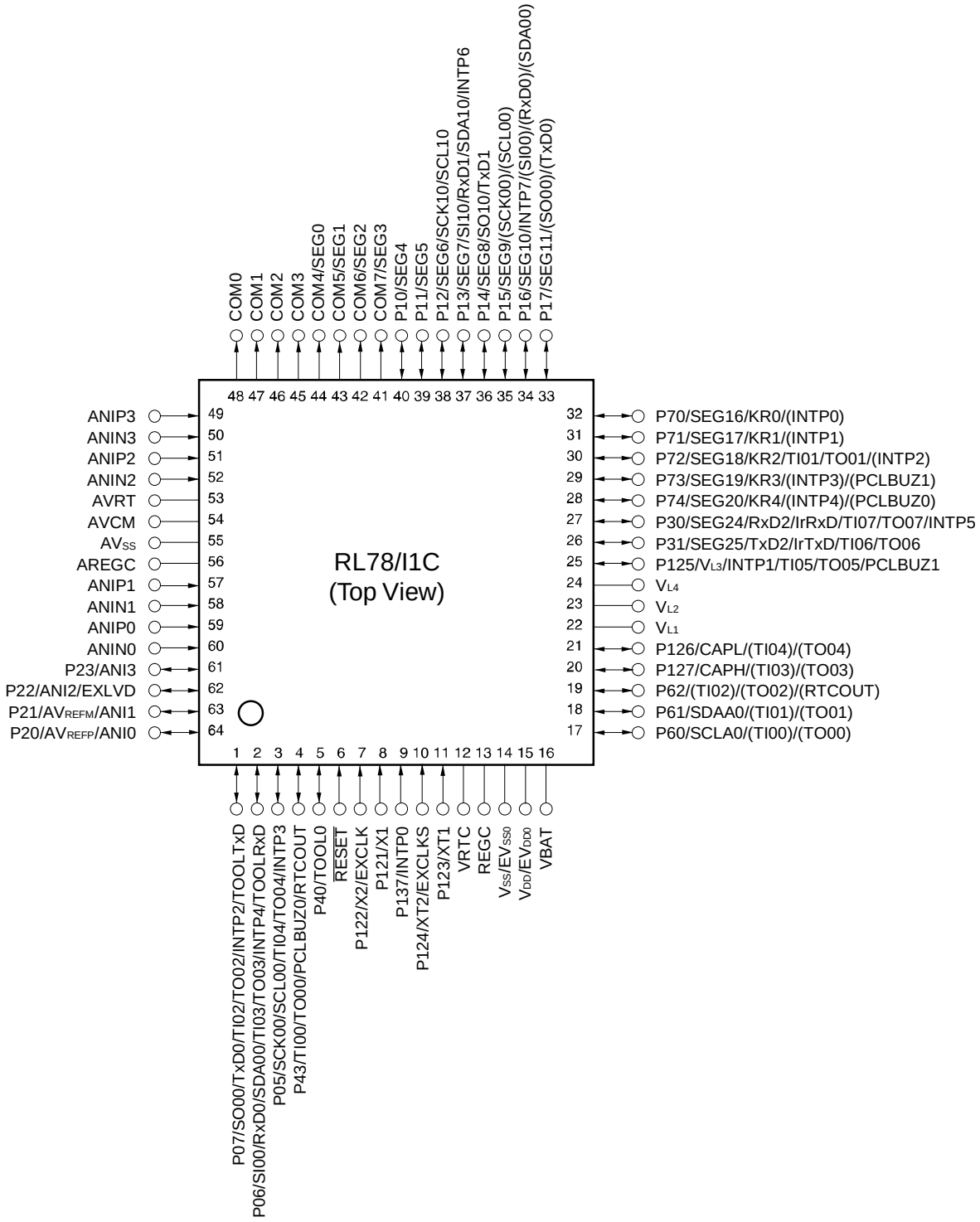
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, IrDA, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	68
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 5.5V
Data Converters	A/D 6x10b, 4x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10npgdfb-30

1.3 Pin Configuration (Top View)

1.3.1 64-pin products

<R> • 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)



Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification.**

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR0). See **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR0).**

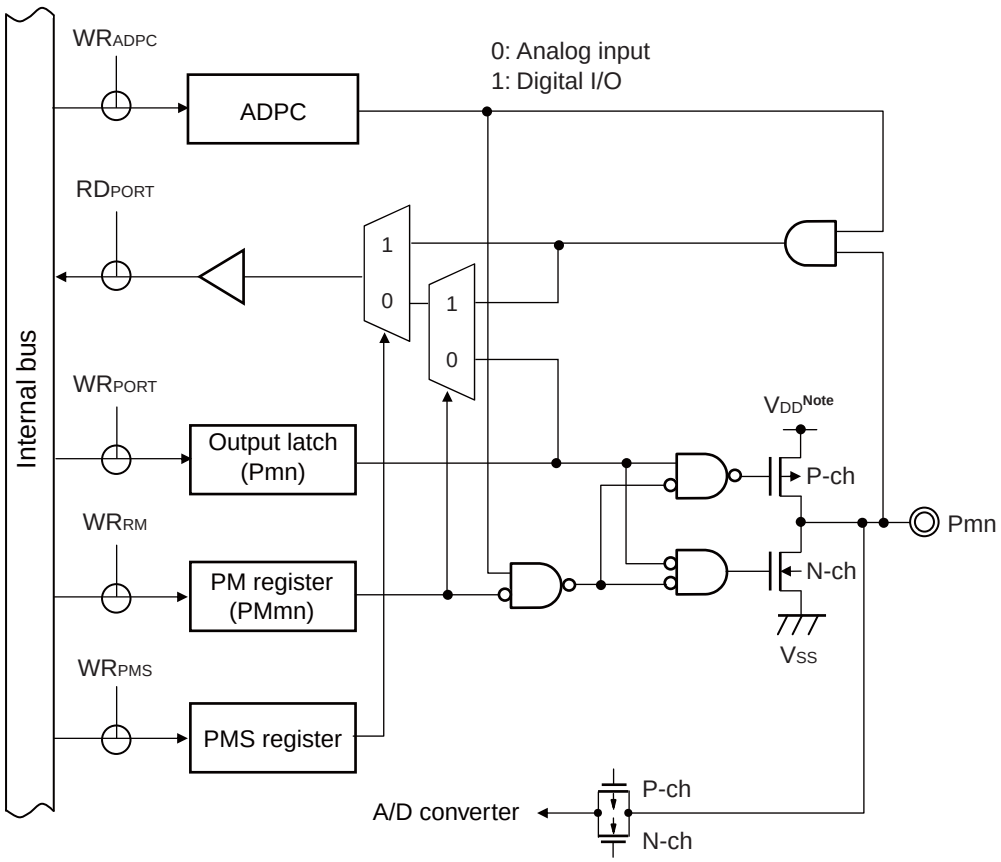
(3/3)

Item		64-pin		80-pin			100-pin	
<R>		R5F10NLEDFB	R5F10NLGDFB	R5F10NMEDFB	R5F10NMGDFB	R5F10NMJDFB	R5F10NPGDFB	R5F10NPJDFB
Key interrupt input		5		8				
AES circuit		Cipher modes of operation: GCM/ECB/CBC Encryption key length: 128/192/256-bit						
Reset	MCU	• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset of internal V_{DD} Note 1 power supply • Internal reset by voltage detector of internal V_{DD} Note 1 power supply • Internal reset by illegal instruction execution Note 2 • Internal reset by RAM parity error • Internal reset by illegal-memory access						
<R>	RTC	• RTC circuit reset by RTC Power-on-reset						
Power-on-reset circuit	Internal V_{DD} Note 1	• Power-on-reset: 1.51 V (TYP.) • Power-down-reset: 1.50 V (TYP.)						
	VRTC	• RTC Power-on-reset: 1.52 V (TYP.) • RTC Power-down-reset: 1.50 V (TYP.)						
Voltage detector	Internal V_{DD} Note 1	• Rising edge: 1.77 V to 4.06 V (13 stages) • Falling edge: 1.73 V to 3.98 V (13 stages)						
	V_{DD}	• Rising edge: 2.54 V to 3.78 V (6 stages) • Falling edge: 2.47 V to 3.71 V (6 stages)						
	VBAT	• Rising edge: 2.12 V to 2.74 V (7 stages) • Falling edge: 2.06 V to 2.68 V (7 stages)						
	VRTC	• Rising edge: 2.22 V to 2.84 V (4 stages) • Falling edge: 2.16 V to 2.78 V (4 stages)						
	EXLVD	• Rising edge: 1.33 V • Falling edge: 1.28 V						
Battery backup function	CPU	V_{DD}/VBAT						
	ΔΣ A/D Converter	V_{DD}/VBAT						
	RTC	VRTC (independent power supply)						
On-chip debug function		Provided						
Power supply voltage		V_{DD} = 1.7 to 5.5 V						
Operating ambient temperature		T_A = −40 to +85 °C						

Notes 1. Either V_{DD} or VBAT is selected by the battery backup function.

2. This reset occurs when instruction code FFH is executed.
This reset does not occur during emulation using an in-circuit emulator or an on-chip debugging emulator.

Figure 2-4. Pin Block Diagram for Pin Type 4-3-3



Note Either V_{DD} or V_{BAT} selected by the battery backup function.

[High-speed on-chip oscillator frequency select register (HOCODIV) setting]

Address: F00A8H

Symbol	7	6	5	4	3	2	1	0
HOCODIV	0	0	0	0	0	HOCODIV2	HOCODIV1	HOCODIV0

HOCODIV2	HOCODIV1	HOCODIV0	Selection of high-speed on-chip oscillator clock frequency	
			FRQSEL3 = 0	FRQSEL3 = 1Note 2
0	0	0	f_{IH} = 24 MHzNote 1	Setting prohibitedNote 1
0	0	1	f_{IH} = 12 MHz	f_{IH} = 16 MHzNote 2
0	1	0	f_{IH} = 6 MHz	f_{IH} = 8 MHzNote 2
0	1	1	f_{IH} = 3 MHz	f_{IH} = 4 MHzNote 2
1	0	0	f_{IH} = 1.5 MHz	f_{IH} = 2 MHzNote 2
1	0	1	Setting prohibited	f_{IH} = 1 MHzNote 2
Other than above			Setting prohibited	

Note 1. When 32 MHz is selected for the CPU/peripheral hardware clock (f_{CLK}), set the high-speed on-chip oscillator clock (f_{IH}) to 24 MHz and select the PLL clock (32 MHz).

Note 2. When the high-speed on-chip oscillator clock (f_{IH}) is selected as the operating clock for the 24-bit ΔΣ A/D converter (the DSADCK bit in the PCKC register is set to 0), the 24-bit ΔΣ A/D converter cannot be used.

9.2.5 Hour counter (RHRCNT)/binary counter 2 (BCNT2)

(1) In calendar count mode:

The RHRCNT counter is used for setting and counting the BCD-coded hour value. It counts carries generated once per hour in the minute counter.
The specifiable time differs according to the setting in the hours mode bit (RCR2.HR24).
When the RCR2.HR24 bit is 0: From 00 to 11 (in BCD)
When the RCR2.HR24 bit is 1: From 00 to 23 (in BCD)
If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, be sure to stop the count operation through the setting of the START bit in RCR2.
The PM bit is only enabled when the RCR2.HR24 bit is 0. Otherwise, the setting in the PM bit has no effect.
To read this counter, follow the procedure in section 9.3.6, Reading 64-Hz counter and time.

Figure 9 - 8 Format of Hour Counter (RHRCNT)

Address: F0587H After reset: Undefined R/W

Symbol	7	6	5	4	3	2	1	0
RHRCNT	0	PM	HR10		HR1			

PM	PM
0	a.m.
1	p.m.
Time Counter Setting for a.m./p.m.	

HR10	10-Hour Count
Counts from 0 to 2 once per carry from the ones place.	

HR1	1-Hour Count
Counts from 0 to 9 once per hour. When a carry is generated, 1 is added to the tens place.	

(2) In binary count mode:

The BCNT2 counter is a readable/writable 32-bit binary counter b23 to b16.
The 32-bit binary counter performs count operation by a carry generating for each second of the 64-Hz counter.
Before writing to this register, be sure to stop the count operation through the setting of the START bit in RCR2.
To read this counter, follow the procedure in section 9.3.6, Reading 64-Hz counter and time.

Figure 9 - 9 Format of Binary Counter 2 (BCNT2)

Address: F0587H After reset: Undefined

Symbol	7	6	5	4	3	2	1	0
BCNT2	BCNT[23:16]							

9.3.9.1 Automatic adjustment

Enable automatic adjustment by setting the RCR2.AADJE bit to 1.
Automatic adjustment is the addition or subtraction of the value counted by the prescaler to or from the value in the RADJ register every time the adjustment period selected by the RCR2.AADJE bit elapses.
Examples are shown below.

[Example 1] Sub-clock running at 32.769 kHz
Adjustment procedure:
When the sub-clock is running at 32.769 kHz, 1 second elapses every 32,769 clock cycles. The RTC is meant to run at 32,768 clock cycles, so the clock runs fast by one clock cycle every second. The time on the clock is fast by 60 clock cycles per minute, so adjustment can take the form of setting the clock back by 60 cycles every minute.

Register settings: (when RCR2.CNTMD = 0)

- RCR2.AADJP = 0 (adjustment every minute)
- RADJ.PMADJ[1:0] = 10b (adjustment is performed by the subtraction from the prescaler.)
- RADJ.ADJ[5:0] = 60 (3Ch)

[Example 2] Sub-clock running at 32.766 kHz
Adjustment procedure:
When the sub-clock is running at 32.766 kHz, 1 second elapses every 32,766 clock cycles. The RTC is meant to run at 32,768 clock cycles, so the clock runs slow by two clock cycles every second. The time on the clock is slow by 20 clock cycles every 10 seconds, so adjustment can take the form of setting the clock forward by 20 cycles every 10 seconds.

Register settings: (when RCR2.CNTMD = 0)

- RCR2.AADJP = 1 (adjustment every 10 seconds)
- RADJ.PMADJ[1:0] = 01b (adjustment is performed by the addition to the prescaler.)
- RADJ.ADJ[5:0] = 20 (14h)

[Example 3] Sub-clock running at 32.764 kHz
Adjustment procedure:
At 32.764 kHz, 1 second elapses on 32,764 clock cycles. Since the RTC operates for 32,768 clock cycles as 1 second, the clock is delayed for four clock cycles per second. In 8 seconds, the delay is 32 clock cycles, so correction can be made by proceeding the clock for 32 clock cycles every 8 seconds.

Register settings when the RCR2.CNTMD bit is 1

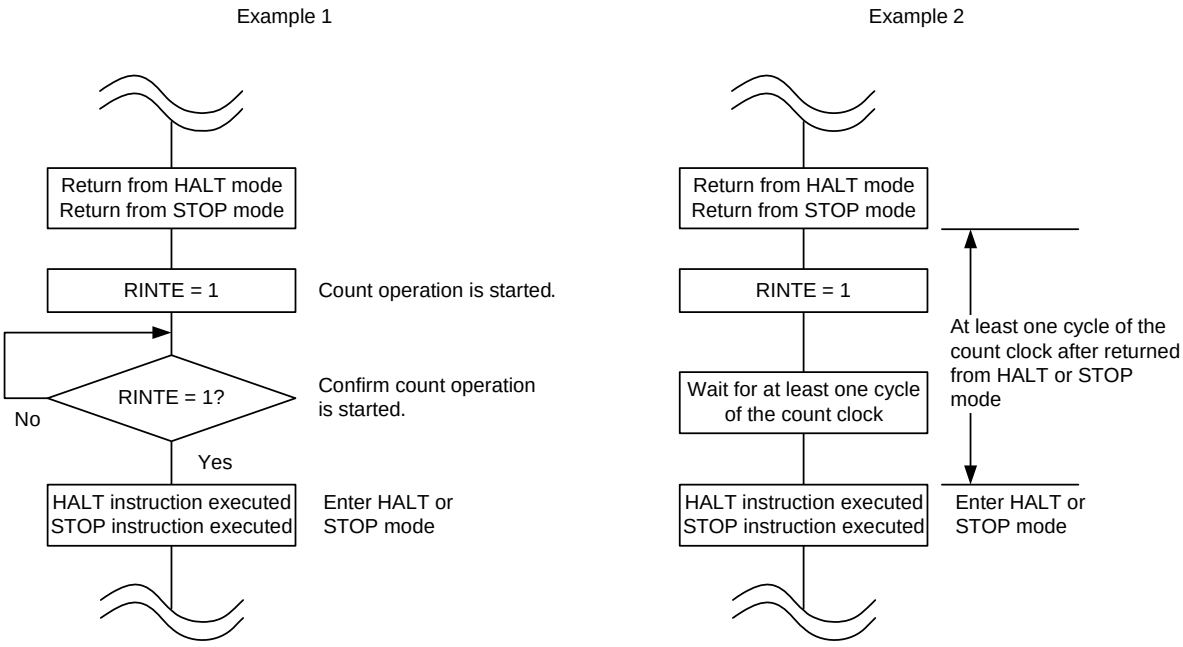
- RCR2.AADJP = 1 (adjustment every 8 seconds)
- RADJ.PMADJ[1:0] = 01b (adjustment is performed by the addition to the prescaler.)
- RADJ.ADJ[5:0] = 32 (20h)

11.4.2 Start of count operation and re-enter to HALT/STOP mode after returned from HALT/STOP mode

When setting the RINTE bit after returned from HALT or STOP mode and entering HALT or STOP mode again, write 1 to the RINTE bit, and confirm the written value of the RINTE bit is reflected or wait for at least one cycle of the count clock.
Then, enter HALT or STOP mode.

- After setting RINTE to 1, confirm by polling that the RINTE bit has become 1, and then enter HALT or STOP mode (see **Example 1** in **Figure 11 - 7**).
- After setting RINTE to 1, wait for at least one cycle of the count clock and then enter HALT or STOP mode (see **Example 2** in **Figure 11 - 7**).

Figure 11 - 7 Procedure of entering to HALT or STOP mode after setting RINTE to 1



15.4 A/D Converter Conversion Operations

The A/D converter conversion operations are described below.

<1> The voltage input to the selected analog input channel is sampled by the sample & hold circuit.

<2> When sampling has been done for a certain time, the sample & hold circuit is placed in the hold state and the sampled voltage is held until the A/D conversion operation has ended.

<3> Bit 9 of the successive approximation register (SAR) is set. The series resistor string voltage tap is set to (1/2) AV_{REF} by the tap selector.

<4> The voltage difference between the series resistor string voltage tap and sampled voltage is compared by the voltage comparator. If the analog input is greater than (1/2) AV_{REF}, the MSB bit of the SAR register remains set to 1. If the analog input is smaller than (1/2) AV_{REF}, the MSB bit is reset to 0.

<5> Next, bit 8 of the SAR register is automatically set to 1, and the operation proceeds to the next comparison. The series resistor string voltage tap is selected according to the preset value of bit 9, as described below.

- Bit 9 = 1: (3/4) AV_{REF}
- Bit 9 = 0: (1/4) AV_{REF}

The voltage tap and sampled voltage are compared and bit 8 of the SAR register is manipulated as follows.

- Sampled voltage ≥ Voltage tap: Bit 8 = 1
- Sampled voltage < Voltage tap: Bit 8 = 0

<6> Comparison is continued in this way up to bit 0 of the SAR register.

<7> Upon completion of the comparison of 10 bits, an effective digital result value remains in the SAR register, and the result value is transferred to the A/D conversion result register (ADCR, ADCRH) and then latched[Note 1].
At the same time, the A/D conversion end interrupt request (INTAD) can also be generated[Note 1].

<8> Repeat steps <1> to <7>, until the ADCS bit is cleared to 0[Note 2].
To stop the A/D converter, clear the ADCS bit to 0.

Notes 1. If the A/D conversion result is outside the A/D conversion result range specified by the ADRCK bit and the ADUL and ADLL registers (see **Figure 15-9**), the A/D conversion result interrupt request signal is not generated and no A/D conversion results are stored in the ADCR and ADCRH registers.

2. While in the sequential conversion mode, the ADCS flag is not automatically cleared to 0. This flag is not automatically cleared to 0 while in the one-shot conversion mode of the hardware trigger no-wait mode, either. Instead, 1 is retained.

Remarks 1. Two types of the A/D conversion result registers are available.

- ADCR register (16 bits): Store 10-bit A/D conversion value
- ADCRH register (8 bits): Store 8-bit A/D conversion value

2. AV_{REF}: The + side reference voltage of the A/D converter. This can be selected from AV_{REFP}, the internal reference voltage (1.45 V), and V_{DD}.

Figure 18-77. Example of Contents of Registers for UART Transmission of UART (UART0 to UART3) (2/2)

(e) Serial output register m (SOm) … Sets only the bits of the target channel.

<R> SOm

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	CKOm2 ×	1	CKOm0 ×	0	0	0	0	1	SOm2 0/1 Note	1	SOm0 0/1 Note

0: Serial data output value is “0”
1: Serial data output value is “1”

(f) Serial output enable register m (SOEm) … Sets only the bits of the target channel to 1.

SOEm

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	SOEm2 0/1	0	SOEm0 0/1

(g) Serial channel start register m (SSm) … Sets only the bits of the target channel to 1.

SSm

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	SSm3 ×	SSm2 0/1	SSm1 ×	SSm0 0/1

Note Before transmission is started, be sure to set to 1 when the SOLmn bit of the target channel is set to 0, and set to 0 when the SOLmn bit of the target channel is set to 1. The value varies depending on the communication data during communication operation.

Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 3), q: UART number (q = 0 to 3)
mn = 00, 02, 10, 12

2. ☐ : Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

19.3.2 Peripheral reset control register 0 (PRR0)

The PRR0 register is used to control resetting of the on-chip peripheral modules.

Each bit in this register controls resetting and release of the reset state of the corresponding on-chip peripheral module.

To reset the serial interface IICA0, be sure to set bits 4 (IICA0RES) to 1.

The PRR0 register can be set by a 1-bit or an 8-bit memory manipulation instruction.

Reset signal generation clears the PRR0 register to 00H.

Figure 19-6. Format of Peripheral Reset Control Register 0 (PRR0)

Address: F00F1H After reset: 00H R/W

Symbol	7	<6>	<5>	<4>	<3>	<2>	1	<0>
PRR0	0	IRDARES	ADCRES	IICA0RES	SAU1RES	SAU0RES	0	TAU0RES

IICA0RES	Control resetting of the serial interface IICA0
0	Release of the reset state of the serial interface IICA0
1	The serial interface IICA0 is in the reset state.

19.3.3 IICA control register n0 (IICCTLn0)

This register is used to enable/stop I^2C operations, set wait timing, and set other I^2C operations.

The IICCTLn0 register can be set by a 1-bit or 8-bit memory manipulation instruction. However, set the SPIEn, WTIMn, and ACKEn bits while IICEn = 0 or during the wait period. These bits can be set at the same time when the IICEn bit is set from “0” to “1”.

Reset signal generation clears this register to 00H.

Remark n = 0

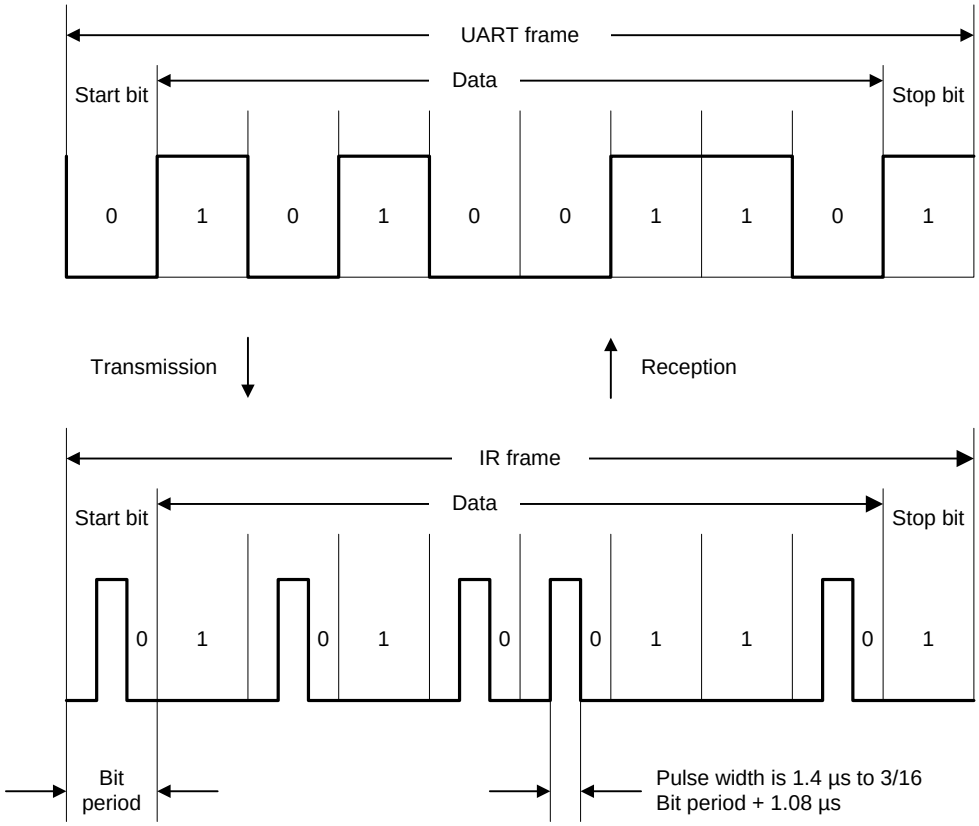
20.3.2 Transmission

In transmission, the signals output from the SAU (UART frames) are converted to the IR frame data through the IrDA (see **Figure 20-5**). When IRTXINV bit is 0 and serial data is 0, high-level pulses with the width of 3/16 the bit rate (1-bit width period) are output (initial setting). The high-level pulse width can be changed by using the IRCKS2 to IRCKS0 bits. The standard prescribes that the minimum high-level pulse width should be 1.41 μs and the maximum high-level pulse width be (3/16 + 2.5%) $\times$ bit rate or (3/16 $\times$ bit rate) + 1.08 μs.

When the CPU/peripheral hardware clock (f_{CLK}) is 20 MHz, the high-level pulse width can be 1.41 μs to 1.6 μs.

When serial data is 1, no pulses are output.

Figure 20-5. IrDA Transmission/Reception



21.10.6 Eight-time-slice display example

Figure 21-42 shows how the 15x8 dot LCD panel having the display pattern shown in Figure 21-41 is connected to the segment signals (SEG4 to SEG18) and the common signals (COM0 to COM7). This example displays data “123” in the LCD panel. The contents of the display data register (addresses F0404H to F0412H) correspond to this display.

The following description focuses on numeral “3.” (∃) displayed in the first digit. To display “3.” in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG4 to SEG8 pins according to Table 21-19 at the timing of the common signals COM0 to COM7; see Figure 21-41 for the relationship between the segment signals and LCD segments.

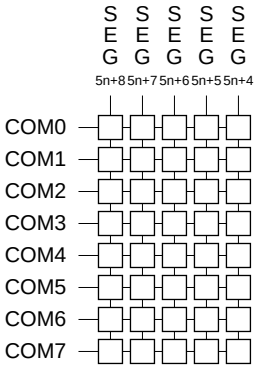
Table 21-19. Select and Deselect Voltages (COM0 to COM7)

Segment / Common	SEG4	SEG5	SEG6	SEG7	SEG8
COM0	Select	Select	Select	Select	Select
COM1	Deselect	Select	Deselect	Deselect	Deselect
COM2	Deselect	Deselect	Select	Deselect	Deselect
COM3	Deselect	Select	Deselect	Deselect	Deselect
COM4	Select	Deselect	Deselect	Deselect	Deselect
COM5	Select	Deselect	Deselect	Deselect	Select
COM6	Deselect	Select	Select	Select	Deselect
COM7	Deselect	Deselect	Deselect	Deselect	Deselect

According to Table 21-19, it is determined that the display data register location (F0404H) that corresponds to SEG4 must contain 00110001.

Figure 21-43 shows examples of LCD drive waveforms between the SEG4 signal and each common signal. When the select voltage is applied to SEG4 at the timing of COM0, a waveform is generated to turn on the corresponding LCD segment.

Figure 21-41. Eight-Time-Slice LCD Display Pattern and Electrode Connections



Remark 100-pin products: n = 0 to 6

<R>

Table 26 - 1 Operating Statuses in HALT Mode (3/4)

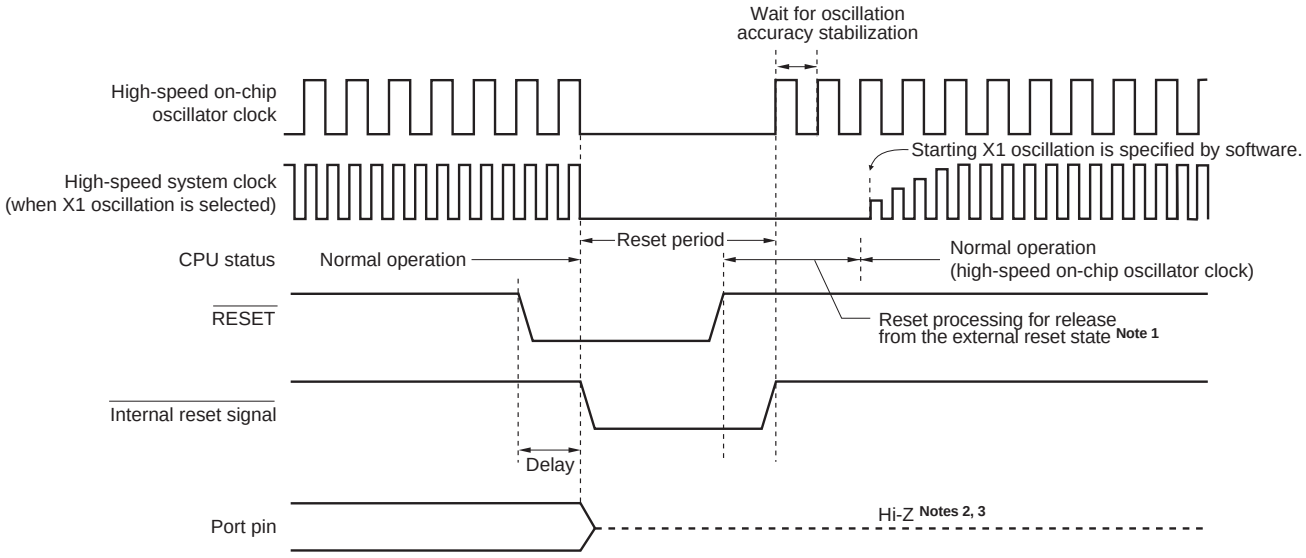
Item \ HALT Mode Setting			When HALT Instruction is Executed While CPU is Operating on Subsystem Clock		
			When CPU is Operating on XT1 Clock (f_{XT})	When CPU is Operating on External Subsystem Clock (f_{EXS})	When CPU is Operating on Low-speed on-chip oscillator clock (f_{IL})
System clock			Clock supply to the CPU is stopped.		
	Main system clock	f_{IH}	Operation disabled		
		f_{IM}			
		f_X			
		f_{EX}			
		f_{PLL}			
	Subsystem clock	f_{XT}	Operation continues (cannot be stopped) (Operation disabled when RTC power-on-reset occurs)	Cannot operate	Operation disabled
		f_{EXS}	Cannot operate	Operation continues (cannot be stopped) (Operation disabled when RTC power-on-reset occurs)	Operation disabled
	Low-speed on-chip oscillator clock	f_{IL}	Set by bits 0 (WDSTBYON) and 4 (WDTON) of the option byte (000C0H) and bit 4 (WUTMMCK0) of the subsystem clock supply option control register (OSMC). • WUTMMCK0 = 1 or SELLOSC = 1: Oscillates (However, setting the WUTMMCK0 and SELLOSC bits to 1 is prohibited while the sub clock (f_{SX}) operates.) • WUTMMCK0 = 0, SELLOSC = 0, and WDTON=0: Stops • WUTMMCK0 = 0, SELLOSC = 0, WDTON = 1, and WDSTBYON = 1: Oscillates • WUTMMCK0 = 0, SELLOSC = 0, WDTON = 1, and WDSTBYON = 0: Stops		Operation continues (cannot be stopped)
CPU			Operation stopped		
Code flash memory					
Data flash memory					
RAM			Operation stopped (Operable while in the DTC is executed)		
Port (latch)			Status before HALT mode was set is retained (rewriting the port register by the DTC can change the port pin setting).		
Timer array unit			Operates when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).		Operable
Independent power supply real-time clock (RTC)			Operable (Operation stopped when RTC power-on-reset occurs)		
Frequency measurement function			Operation disabled		
High-speed on-chip oscillator clock frequency correction function					
Oscillation stop detection					
Battery backup function			Operable		
12-bit Interval timer					
8-bit Interval timer					
Watchdog timer			See **CHAPTER 14 WATCHDOG TIMER**.		
Clock output/buzzer output			Operates when the subsystem clock is selected as the clock source for counting.		
10-bit resolution A/D converter			Operation disabled		
24-bit ΔΣ A/D converter					
Temperature sensor 2					
Serial array unit (SAU)			Operates when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).		Operable
IrDA			Operation disabled		
Serial interface (IICA)			Operation disabled		
LCD controller/driver			Operable (However, this depends on the status of the clock selected as the LCD source clock:operation is possible if the selected clock is operating, but operation will stop if the selected clock is stopped.)		
Data transfer controller (DTC)			Operates when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).		Operable
Event link controller (ELC)			Operable function blocks can be linked		
32-bit multiplier and multiply accumulator			Operation disable		

(**Remark** is listed on the next page.)

27.1 Timing of Reset Operation

This LSI is reset by input of the low level on the $\overline{\text{RESET}}$ pin and released from the reset state by input of the high level on the $\overline{\text{RESET}}$ pin. After reset processing, execution of the program with the high-speed on-chip oscillator clock as the operating clock starts.

Figure 27-2. Timing of Reset by $\overline{\text{RESET}}$ Input

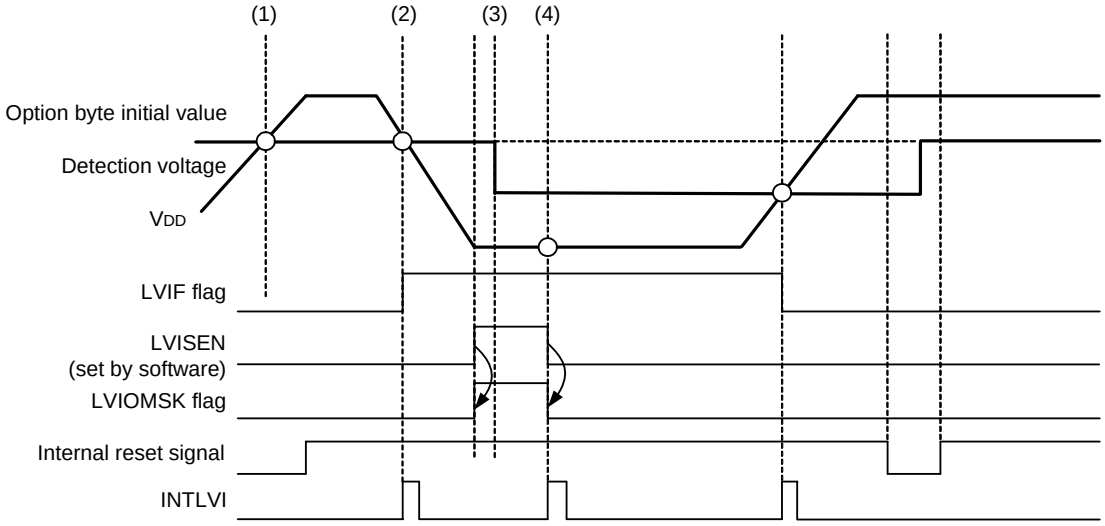


The input buffer of the $\overline{\text{RESET}}$ pin is connected to internal V_{DD}. When using the battery backup function, input signal based on the voltage of the selected power supply source (V_{DD} pin or VBAT pin).

Release from the reset state is automatic in the case of a reset due to a watchdog timer overflow, execution of an illegal instruction, detection of a RAM parity error, or detection of illegal memory access. After reset processing, program execution starts with the high-speed on-chip oscillator clock as the operating clock.

(**Notes** and **Caution** are listed on the next page.)

Figure 29 - 28 Example of Timing for Changing LVD Detection Voltage Using LVIS When $V_{DD} < V_{LVD}$



Operation

(1) When the supply voltage rises, the detection voltage set by the option byte is used to release the reset.

(2) At LVD detection (falling), the detection voltage set by the option byte

(3) The value of the LVIS register is changed.

(4) If $V_{DD} < V_{LVD}$ at the same time the masking is released, an interrupt is generated.

32.3.8.1 A/D test register (ADTES)

This register is used to select the A/D converter's positive reference voltage, A/D converter's negative reference voltage, analog input channel (ANIxx), temperature sensor output voltage, or internal reference voltage (1.45 V) as the target of A/D conversion.

When using the A/D test function, specify the following settings:

- Select negative reference voltage as the target of A/D conversion for zero-scale measurement.
- Select positive reference voltage as the target of A/D conversion for full-scale measurement.

The ADTES register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 32-16. Format of A/D Test Register (ADTES)

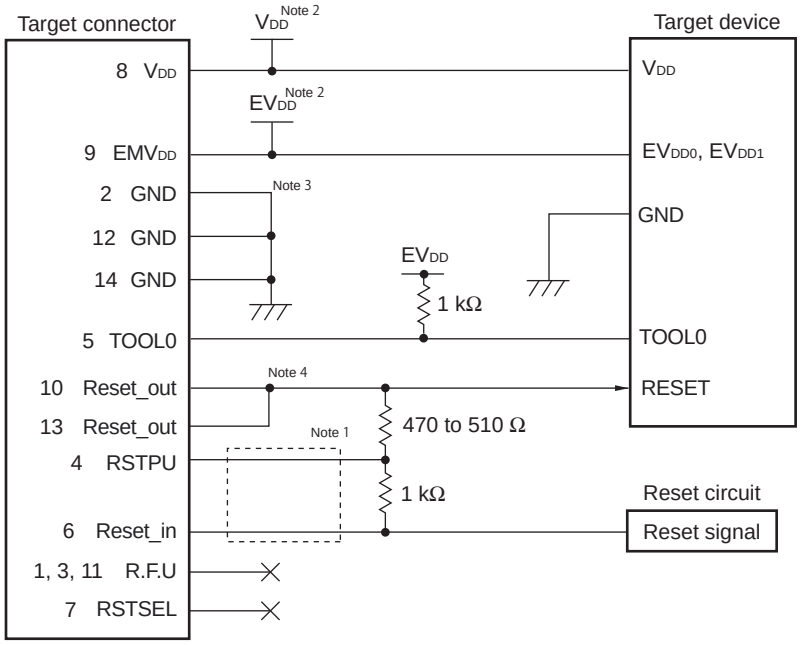
Address: F0013H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADTES	0	0	0	0	0	0	ADTES1	ADTES0

ADTES1	ADTES0	A/D conversion target
0	0	ANIxx/temperature sensor output voltage[Note]/internal reference voltage (1.45 V)[Note] (This is specified using the analog input channel specification register (ADS).)
1	0	Negative reference voltage (selected with the ADREFM bit in ADM2)
1	1	Positive reference voltage (selected with the ADREFP1 or ADREFP0 bit in ADM2)
Other than above		Setting prohibited

Note Temperature sensor output voltage/internal reference voltage (1.45 V) can be used only in HS (high-speed main) mode.

Figure 37-2. Example of Connections with the E1 On-chip Debugging Emulator (when the Battery Backup Function is Not in Use)



Notes 1. These connections must be made if the on-chip debugging function is to be used. Flash programming can proceed whether or not these connections are made.

2. Depending on the number of pins the microcontroller has, V_{DD} and EV_{DD} may be multiplexed on the same pin.
In this case, connect both V_{DD} and EMV_{DD} of the E1 emulator to the power supply pin of the microcontroller.

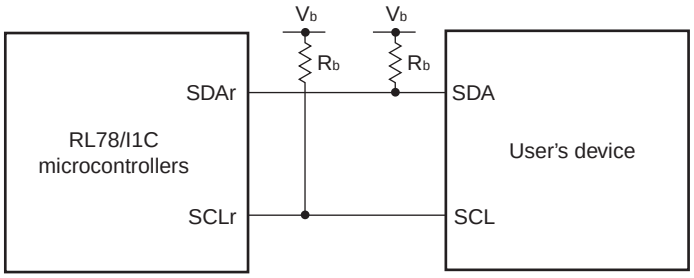
3. Be sure to connect pins 2, 12, and 14 of the E1 emulator to the ground pins on the user system.
As well as being used as electrical ground pins, these pins are used for monitoring connection of an E1 or E20 emulator to the user system.

4. Pins 10 and 13 of the E1 emulator must be connected.

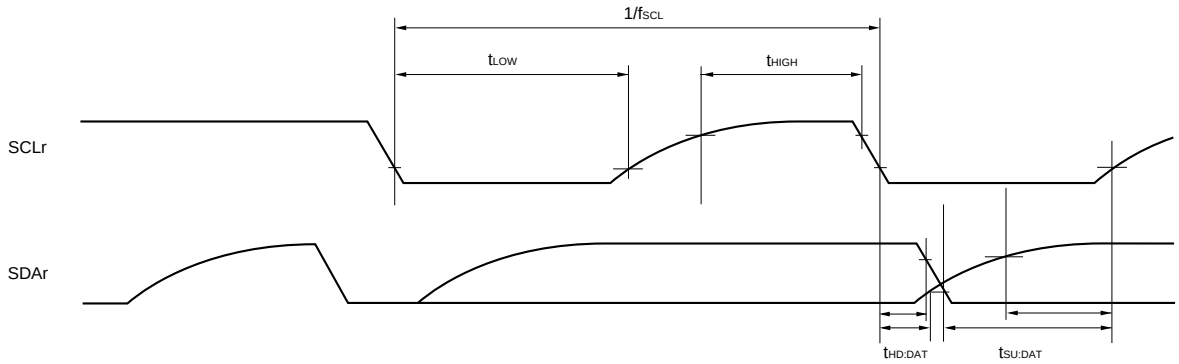
Caution The values in the connection example are for reference. Before proceeding with flash programming for mass production, sufficiently evaluate the values in use to confirm that they satisfy the specifications of the target device. Do not use the battery backup function when the circuits for the connection are as shown in the figure.

Remark With products not provided with an EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} pin, replace EV_{DD0} and EV_{DD1} with V_{DD}, or replace EV_{SS0} and EV_{SS1} with V_{SS}.

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. R_b[Ω]:Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

2. r: IIC number (r = 00, 10, 30), g: PIM, POM number (g = 0, 1, 8)

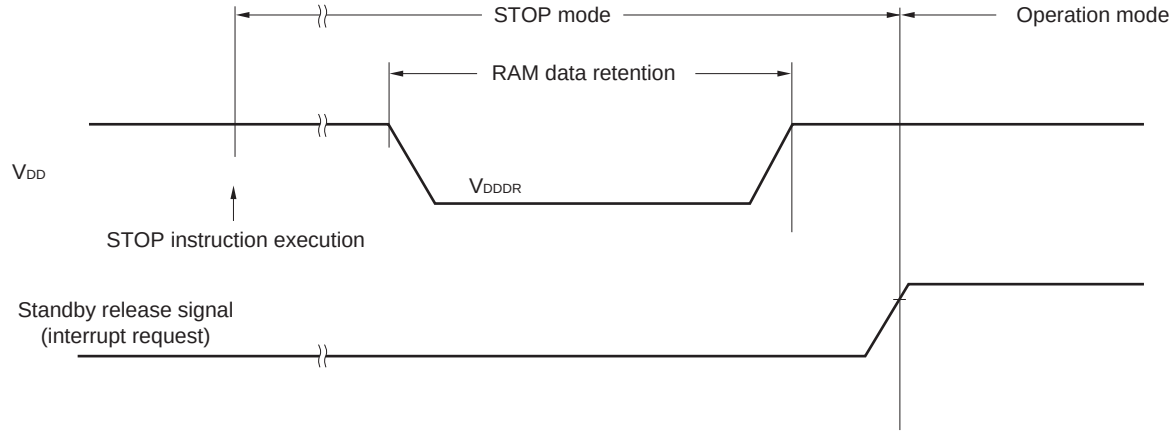
3. f_{MCK}: Serial array unit operation clock frequency
(Operating clock that is set with the serial clock select register m (SPSm) and the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 02, 12))

<R> 41.9 RAM Data Retention Characteristics

(T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46[Note]		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



41.10 Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 1.9 V ≤ V_{DD}[Note 4] ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}	1.9 V ≤ V_{DD}[Note 4] ≤ 5.5 V	1		24	MHz
Number of code flash rewrites[Notes 1, 2, 3]	C_{erwr}	Retained for 20 years T_A = 85°C	1,000			Times
Number of data flash rewrites[Notes 1, 2, 3]		Retained for 1 year T_A = 25°C		1,000,000		
		Retained for 5 years T_A = 85°C	100,000			
		Retained for 20 years T_A = 85°C	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. This characteristic indicates the flash memory characteristic and based on Renesas Electronics reliability test.

4. Either V_{DD} or VBAT is selected by the battery backup function.

41.11 Dedicated Flash Memory Programmer Communication (UART)

(T_A = –40 to +85°C, 1.9 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD}[Note] ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

Note Either V_{DD} or VBAT is selected by the battery backup function.