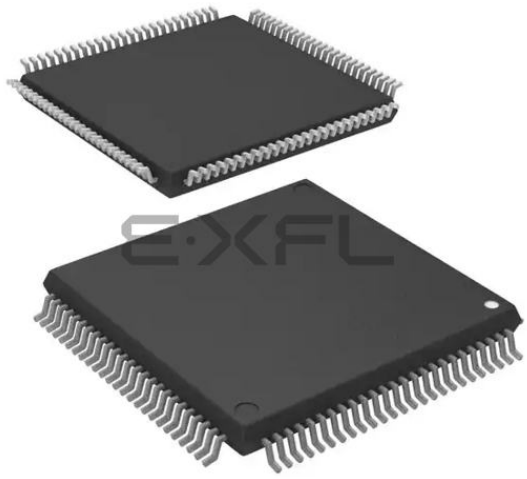
Renesas Electronics America Inc - R5F10NPJDFB#50 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, IrDA, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	68
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 5.5V
Data Converters	A/D 6x10b, 4x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10npjdfb-50

CHAPTER 3 CPU ARCHITECTURE

3.1 Memory Space

Products in the RL78/I1C can access a 1 MB address space. Figures 3-1 and 3-3 show the memory maps.

Table 3-5. SFR List (3/4)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
FFF90H	12-bit interval timer control register	ITMC		R/W	–	–	√	0FFFH
FFF91H								
FFFA0H	Clock operation mode control register	CMC		R/W	–	√	–	00H Note 1
FFFA1H	Clock operation status control register	CSC		R/W	√	√	–	C0H Note 1
FFFA2H	Oscillation stabilization time counter status register	OSTC		R	√	√	–	00H
FFFA3H	Oscillation stabilization time select register	OSTS		R/W	–	√	–	07H
FFFA4H	System clock control register	CKC		R/W	√	√	–	00H
FFFA5H	Clock output select register 0	CKS0		R/W	√	√	–	00H
FFFA6H	Clock output select register 1	CKS1		R/W	√	√	–	00H
FFFA7H	Subsystem clock select resister	CKSEL		R/W	√	√	–	00H
FFFA8H	Reset control flag register	RESF		R	–	√	–	Undefined Note 2
FFFA9H	Voltage detection register	LVIM		R/W	√	√	–	00H Note 2
FFFAAH	Voltage detection level register	LVIS		R/W	√	√	–	00H/01H/ 81H Note 2
FFFABH	Watchdog timer enable register	WDTE		R/W	–	√	–	1AH/9AH Note 3
FFFACH	CRC input register	CRCIN		R/W	–	√	–	00H
FFFD0H	Interrupt request flag register 2L	IF2L	IF2	R/W	√	√	√	00H
FFFD1H	Interrupt request flag register 2H	IF2H		R/W	√	√		00H
FFFD2H	Interrupt request flag register 3L	IF3L	IF3	R/W	√	√	√	00H
FFFD4H	Interrupt mask flag register 2L	MK2L	MK2	R/W	√	√	√	FFH
FFFD5H	Interrupt mask flag register 2H	MK2H		R/W	√	√		FFH
FFFD6H	Interrupt mask flag register 3L	MK3L	MK3	R/W	√	√	√	FFH

Notes 1. This register is reset only by a power-on reset.

2. The reset values of the registers vary depending on the reset source as shown below.

Register \ Reset Source		$\overline{\text{RESET}}$ Input	Reset by POR	Reset by Execution of Illegal Instruction	Reset by WDT	Reset by RAM Parity Error	Reset by Illegal-Memory Access	Reset by LVD
RESF	TRAP	Cleared (0)		Set (1)	Held			Held
	WDTRF			Held	Set (1)	Held		
	RPERF			Held		Set (1)	Held	
	IAWRF			Held			Set (1)	
	LVIRF			Held				Set (1)
LVIM	LVISEN	Cleared (0)						Held
	LVIOMSK	Held						
	LVIF							
LVIS		Cleared (00H/01H/81H)						Clear (00H/81H) Note 4

3. The reset value of the WDTE register is determined by the setting of the option byte.

4. When option byte LVIMDS1, LVIMDS0 = 0, 1: LVD reset is not generated.

Table 3-6. Extended SFR (2nd SFR) List (4/11)

	Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
						1-bit	8-bit	16-bit	
<R>	F0154H	Serial mode register 12	SMR12		R/W[Note 1]	—	—	√	0020H/0000H[Note 2]
	F0155H								
<R>	F0156H	Serial mode register 13	SMR13		R/W[Note 1]	—	—	√	0020H/0000H[Note 2]
	F0157H								
	F0158H	Serial communication operation setting register 10	SCR10		R/W	–	–	√	0087H
	F0159H								
	F015AH	Serial communication operation setting register 11	SCR11		R/W	–	–	√	0087H
	F015BH								
<R>	F015CH	Serial communication operation setting register 12	SCR12		R/W[Note 1]	—	—	√	0087H/0000H[Note 3]
	F015DH								
<R>	F015EH	Serial communication operation setting register 13	SCR13		R/W[Note 1]	—	—	√	0087H/0000H[Note 3]
	F015FH								
	F0160H	Serial channel enable status register 1	SE1L	SE1	R	√	√	√	0000H
	F0161H		–			–	–		
	F0162H	Serial channel start register 1	SS1L	SS1	R/W	√	√	√	0000H
	F0163H		–			–	–		
	F0164H	Serial channel stop register 1	ST1L	ST1	R/W	√	√	√	0000H
	F0165H		–			–	–		
	F0166H	Serial clock select register 1	SPS1L	SPS1	R/W	–	√	√	0000H
	F0167H		–			–	–		
	F0168H	Serial output register 1	SO1		R/W	–	–	√	0F0FH/0303H[Note 4]
	F0169H								
	F016AH	Serial output enable register 1	SOE1L	SOE1	R/W	√	√	√	0000H
	F016BH		–			–	–		
	F0174H	Serial output level register 1	SOL1L	SOL1	R/W	–	√	√	0000H
	F0175H		–			–	–		
	F0180H	Timer counter register 00	TCR00		R	–	–	√	FFFFH
	F0181H								
	F0182H	Timer counter register 01	TCR01		R	–	–	√	FFFFH
	F0183H								
	F0184H	Timer counter register 02	TCR02		R	–	–	√	FFFFH
	F0185H								
	F0186H	Timer counter register 03	TCR03		R	–	–	√	FFFFH
	F0187H								
	F0188H	Timer counter register 04	TCR04		R	–	–	√	FFFFH
	F0189H								
	F018AH	Timer counter register 05	TCR05		R	–	–	√	FFFFH
	F018BH								
	F018CH	Timer counter register 06	TCR06		R	–	–	√	FFFFH
	F018DH								

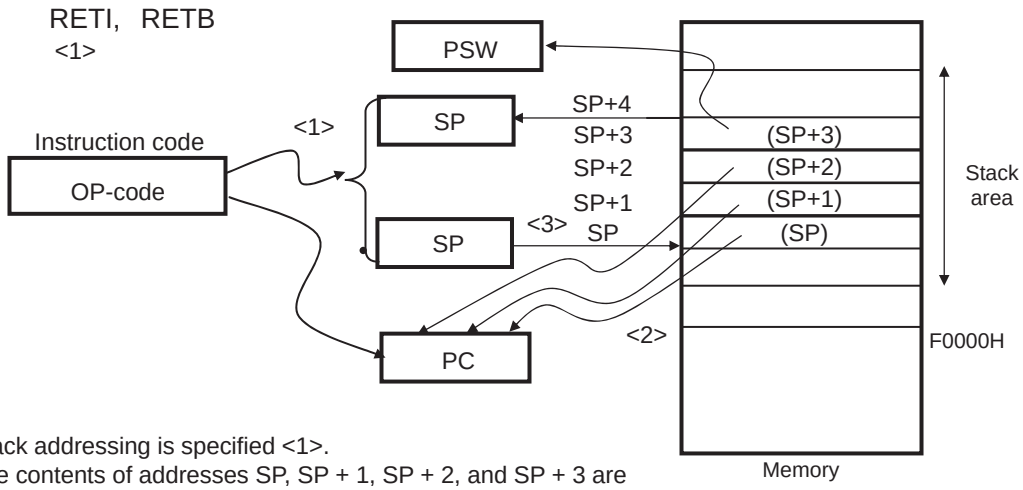
<R> **Notes 1.** These registers for R5F10NMG, R5F10NLG, R5F10NME, and R5F10NLE can only be read.

<R> **2.** R5F10NPJ, R5F10NMJ, R5F10NPG: 0020H
R5F10NMG, R5F10NLG, R5F10NME, R5F10NLE: 0000H

<R> **3.** R5F10NPJ, R5F10NMJ, R5F10NPG: 0087H
R5F10NMG, R5F10NLG, R5F10NME, R5F10NLE: 0000H

<R> **4.** R5F10NPJ, R5F10NMJ, R5F10NPG: 0F0FH
R5F10NMG, R5F10NLG, R5F10NME, R5F10NLE: 0303H

Figure 3-39. Example of RETI, RETB



- Stack addressing is specified <1>.
- The contents of addresses SP, SP + 1, SP + 2, and SP + 3 are stored in PC bits 7 to 0, 15 to 8, 19 to 16, and the PSW, respectively <2>.
- The value of SP <3> is increased by four.

5.5.2 Details of LS (low-speed main) mode

LS (low-speed main) mode supports both CPU processing capacity and operating voltage performance, suitable for applications that require low-power consumption at 1 to 8 MHz.

LS mode can be operated immediately after a reset release. Also, this mode can be entered from HS (high-speed main) mode, LV (low-voltage main) mode, or LP (low-power main) mode. When entering from HS mode to LS mode, make sure that the operating frequency is 1 MHz ≤ f_{CLK} ≤ 8 MHz.

In LS mode, low-power consumption can be set by the MCSEL bit in the regulator mode control register (PMMC). When setting low-power consumption, set the MCSEL bit to 1 while the operating frequency is 1 MHz ≤ f_{CLK} ≤ 4 MHz.

The suitable operating range in LS mode is when the supply voltage is 1.9 V ≤ V_{DD} ≤ 5.5 V and the operating frequency is 4 MHz < f_{CLK} ≤ 8 MHz if MCSEL = 0, and when the supply voltage is 1.9 V ≤ V_{DD} ≤ 5.5 V and the operating frequency is 1 MHz < f_{CLK} ≤ 4 MHz if MCSEL = 1.

Figure 5 - 8 Operating Range in LS Mode (MCSEL = 0)

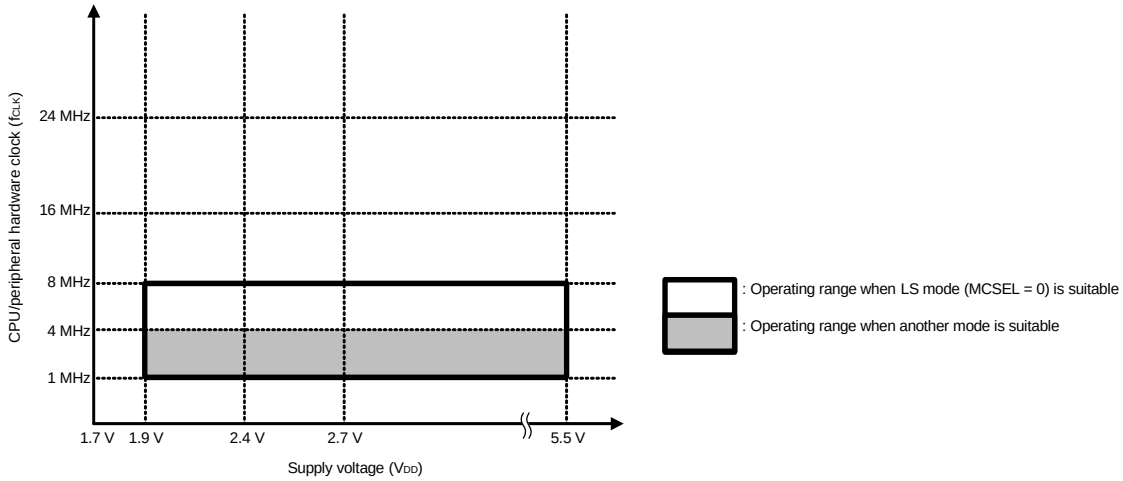
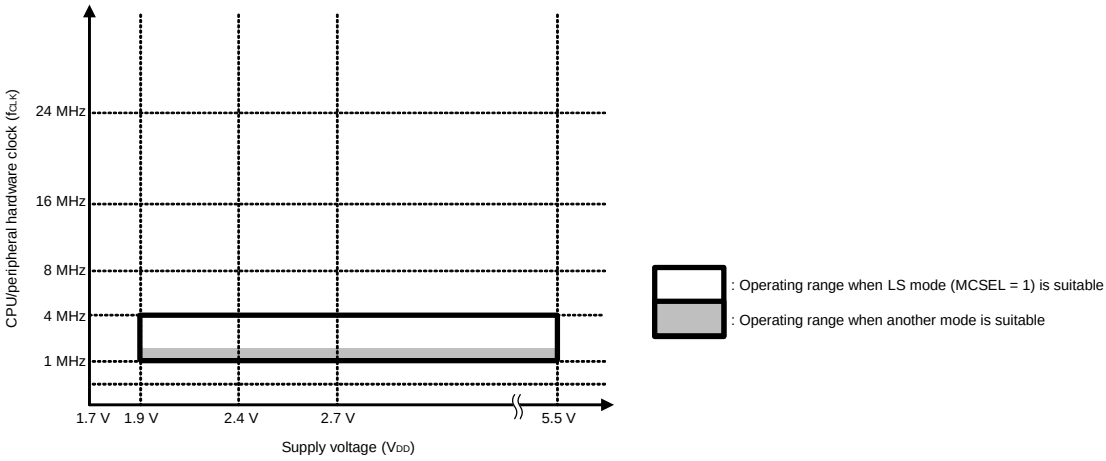


Figure 5 - 9 Operating Range in LS Mode (MCSEL = 1)



Caution When entering another flash operation mode, make sure that MCSEL = 0.

Figure 6 - 11 Format of Peripheral enable register 1 (PER1)

Address: F00FAH After reset: 00H R/W

Symbol	7	<6>	5	4	<3>	2	1	<0>
PER1	0	FMCEN	0	0	DTCEN	0	0	DSADCEN

FMCEN	Control of frequency measurement circuit input clock supply
0	Stops input clock supply. • SFR used by the frequency measurement circuit cannot be written. The read value is 00H. • The frequency measurement circuit is in the reset state.
1	Enables input clock supply. • SFR used by the frequency measurement circuit can be read and written.

DTCEN	Control of DTC input clock supply
0	Stops input clock supply. • DTC cannot run.
1	Enables input clock supply. • DTC can run.

DSADCEN	Control of 24-bit ΔΣ A/D converter input clock supply
0	Stops input clock supply. • SFR used by the 24-bit ΔΣ A/D converter cannot be written. The read value is 00H. However, the SFR is not initialized. Note
1	Enables input clock supply. • SFR used by the 24-bit ΔΣ A/D converter can be read and written.

Note To initialize the 24-bit ΔΣ A/D converter and the SFR used by the 24-bit ΔΣ A/D converter, use bit 0 (DSADRES) of PRR1.

Caution 1. Be sure to clear the following bits to 0.
Bits 1, 2, 4, 5 and 7

Caution 2. Do not change the target bit in the PER1 register while operation of each peripheral function is enabled. Change the setting specified by PER1 while operation of each peripheral function assigned to PER1 is stopped.

9.2 Register Descriptions

When writing to or reading from RTC registers, do so in accordance with section 9.6.5, Notes when writing to and reading from registers.

If the value in an RTC register after a reset is given as undefined in the list, it is not initialized by a reset. When RTC enters the reset state or a low power consumption state during counting operations (i.e. while the RCR2.START bit is 1), the year, month, day of the week, date, hours, minutes, seconds, and 64-Hz counters continue to operate. Note that a reset generated during writing to or updating of a register might destroy the register value. In addition, do not allow the chip to <R> enter STOP mode immediately after setting any of these registers. For details, refer to section 9.6.4, Transitions to low power consumption modes after setting registers.

9.2.1 Peripheral enable register 2 (PER2)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to the hardware that is not used is also stopped so as to decrease the power consumption and noise.

To manipulate of the registers of the independent power supply real-time clock, set (1) the bit 0 (VRTCEN). Other than time when read/write accessing, clear (0) the bit 0 (VRTCEN).

The PER2 register can be set by a 1-bit or an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 9 - 2 Format of Peripheral enable register 2 (PER2)

Address: F00FDH After reset: 00H R/W

Symbol	<7>	<6>	5	4	3	<2>	1	<0>
PER2	TMKAEN	OSDCEN	0	0	0	MACEN	0	VRTCEN

VRTCEN	Control of independent power supply RTC input clock supply
0	Stops input clock supply. • SFR used by the independent power supply RTC cannot be written. The read value is 00H. The sub clock (f_{SX}) clock can drive counting by the independent power supply RTC.
1	Enables input clock supply. • SFR used by the independent power supply RTC can be read and written.

Note 1. If the battery back-up function isn't used, leak current may be generated via the VRTC pin when the V_{DD} pin power supply voltage is less than 1.9 V. Therefore, set the VRTCEN bit to 0 except during reading or writing of the SFRs of the independent power supply RTC.

Note 2. If the battery back-up function is used, leak current may be generated via the VRTC pin when the VBAT pin power supply voltage is less than 1.9 V. Therefore, set the VRTCEN bit to 0 except during reading or writing of the SFRs of the independent power supply RTC.

Note 3. When the power of the VRTC pin is not supplied, set the VRTCEN bit to 0.

<R> **Caution Be sure to clear the following bits to 0.**
Bits 1 and 3 to 5

9.2.31 RTC status register (RSR)

RSR is a flag register of the periodic interrupt, carry, and alarm. This register is a common function with the calendar count mode and the binary count mode.
Each flag is set to 1 when the prescaler or the clock counter matches each interrupt setting condition. The prescaler, clock counter, and the setting register of each interrupt are not reset, so each flag may be set before it is read.
This register is set to 00h by an RTC software reset.

Figure 9 - 49 Format of RTC Status Register (RSR)

Address:F05A1H After reset: 00H[Note 1] R/W

Symbol	7	6	5	4	3	2	1	0
RSR	0	0	0	0	0	PF	CF	AF

PF	Periodic interrupt flag
0	No interrupt occurs at a period that is set with RCR1.PES[3:0] bits
1	Interrupt occurs at a period that is set with RCR1.PES[3:0] bits [Note 2]

This flag indicates that the interrupt occurs at a period that is set with RCR1.PES[3:0] bits.
During PF = 1, the periodic interrupt occurs.
<Clear condition>
• 0 is written to the PF flag.
<Set condition>
• Interrupt occurs at a period that is set with RCR1.PES[3:0] bits.

CF	Carry flag
0	No carry of second counter/binary counter 0, and no carry of the 64 Hz counter when the 64 Hz counter is reading
1	Carry of second counter/binary counter 0, or carry of the 64 Hz counter when the 64 Hz counter is reading

During CF = 1, be sure to read again because the value which is read from the count register is not guaranteed.
<Clear conditions>
• 0 is written to the CF flag.
<Set condition>
• Carry of second counter/binary counter 0, or carry of the 64 Hz counter when the 64 Hz counter is reading
• 1 is written to the CF flag.

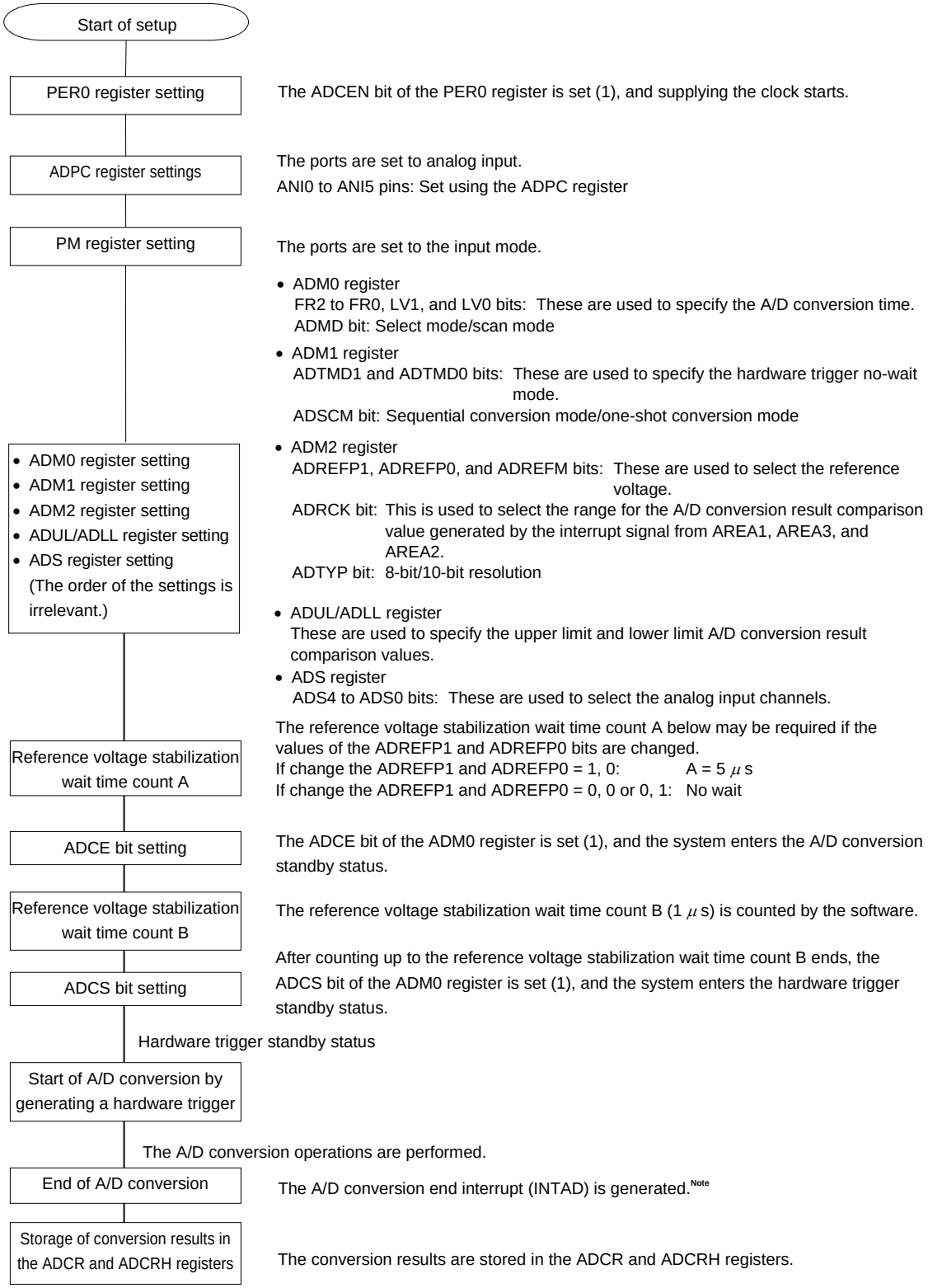
AF	Alarm flag
0	The counter does not match the alarm registers
1	The counter matches the alarm registers [Note 2]

• This bit is set to 1 when the counter matches the alarm time set with the alarm registers (calender count mode: RSECAR, RMINAR, RHRAR, RWKAR, RDAYAR, RMONAR, RYRAR; binary count mode: BCNT0AR, BCNT1AR, BCNT2AR, BCNT3AR) (only registers that the ENB bit is set to 1).
<Clear conditions>
• 0 is written to the AF flag.
<Set condition>
• The counter matches the alarm registers (only registers that the ENB bit is set to 1).

Note 1. After reset is released, read value may be undefind.
Note 2. Writing “1” to this bit is invalid.

15.7.2 Setting up hardware trigger no-wait mode

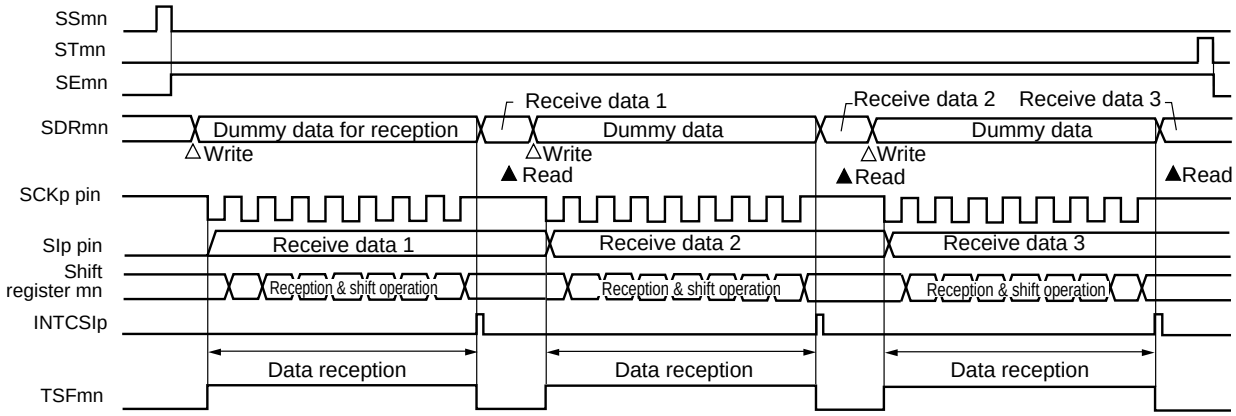
Figure 15-31. Setting up Hardware Trigger No-wait Mode



Note Depending on the settings of the ADRCK bit and ADUL/ADLL register, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCR, ADCRH registers.

(3) Processing flow (in single-reception mode)

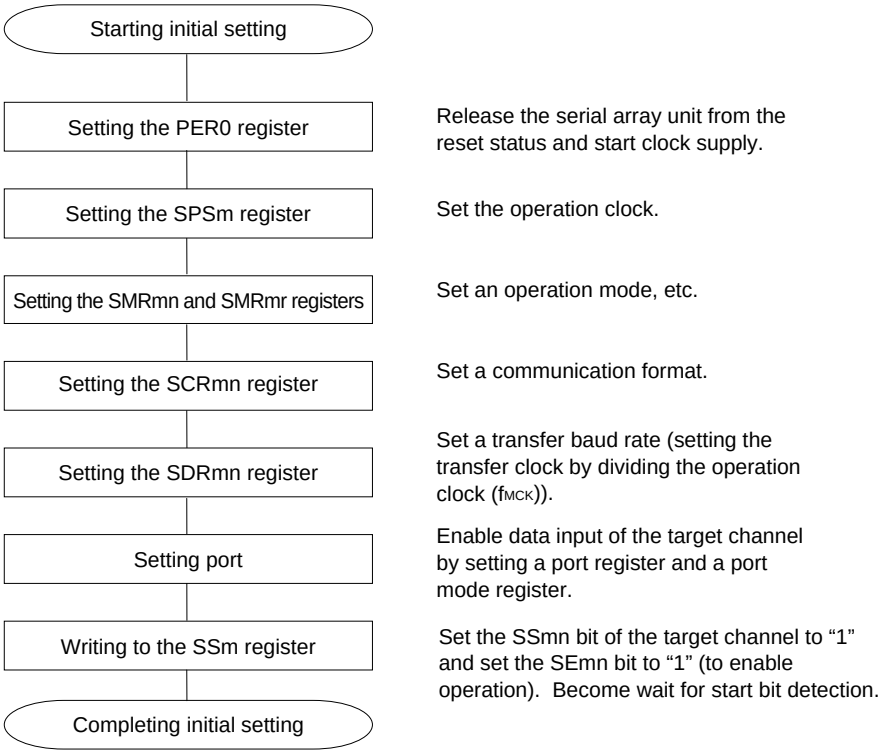
Figure 18-38. Timing Chart of Master Reception (in Single-reception Mode)
(Type 1: DAPmn = 0, CKPmn = 0)



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), p: CSI number (p = 00, 10, 30), mn = 00, 02, 12

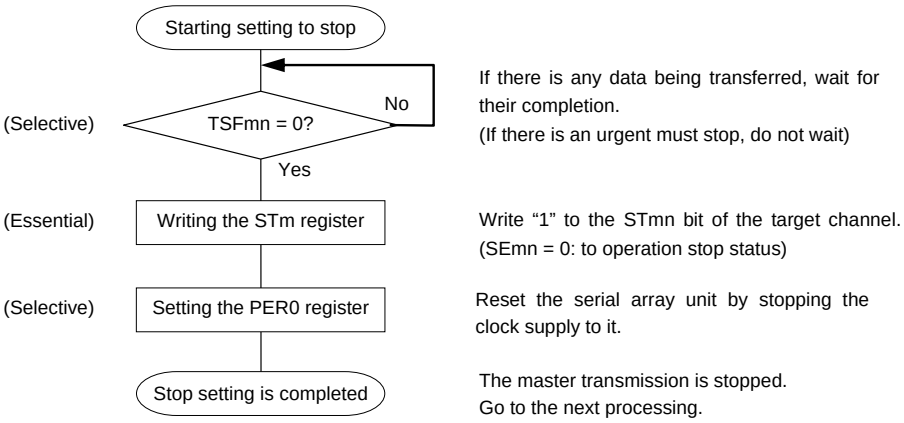
(2) Operation procedure

Figure 18-86. Initial Setting Procedure for UART Reception



Caution Set the RXEmn bit of SCRmn register to 1, and then be sure to set SSmn to 1 after 4 or more f_{MCK} clocks have elapsed.

Figure 18-87. Procedure for Stopping UART Reception



19.5.16 Communication operations

The following shows three operation procedures with the flowchart.

(1) Master operation in single master system

The flowchart when using the RL78/I1C as the master in a single master system is shown below.

This flowchart is broadly divided into the initial settings and communication processing. Execute the initial settings at startup. If communication with the slave is required, prepare the communication and then execute communication processing.

(2) Master operation in multimaster system

In the I^2C bus multimaster system, whether the bus is released or used cannot be judged by the I^2C bus specifications when the bus takes part in a communication. Here, when data and clock are at a high level for a certain period (1 frame), the RL78/I1C takes part in a communication with bus released state.

This flowchart is broadly divided into the initial settings, communication waiting, and communication processing. The processing when the RL78/I1C looses in arbitration and is specified as the slave is omitted here, and only the processing as the master is shown. Execute the initial settings at startup to take part in a communication. Then, wait for the communication request as the master or wait for the specification as the slave. The actual communication is performed in the communication processing, and it supports the transmission/reception with the slave and the arbitration with other masters.

(3) Slave operation

An example of when the RL78/I1C is used as the I^2C bus slave is shown below.

When used as the slave, operation is started by an interrupt. Execute the initial settings at startup, then wait for the INTIICAn interrupt occurrence (communication waiting). When an INTIICAn interrupt occurs, the communication status is judged and its result is passed as a flag over to the main processing.

By checking the flags, necessary communication processing is performed.

Remark n = 0

20.2.2 Peripheral reset control register 0 (PRR0)

The PRR0 register is used to control resetting of the on-chip peripheral modules.

Each bit in this register controls resetting and release of the reset state of the corresponding on-chip peripheral module.

To reset the IrDA, be sure to set bit 6 (IRDARES) to 1.

The PRR0 register can be set by a 1-bit or an 8-bit memory manipulation instruction.

Reset signal generation clears the PRR0 register to 00H.

Figure 20-3. Format of Peripheral Reset Control Register 0 (PRR0)

Address: F00F1H After reset: 00H R/W

Symbol	7	<6>	<5>	<4>	<3>	<2>	1	<0>
PRR0	0	IRDARES	ADCRES	IICA0RES	SAU1RES	SAU0RES	0	TAU0RES

IRDARES	Control resetting of the IrDA
0	Releases the IrDA from the reset state.
1	The IrDA is in the reset state.

20.4 Usage Notes on IrDA

(1) The IrDA function cannot be used to transition to SNOOZE via IrRxD reception.

(2) The input of IrDA operating clock can be disabled/enabled with the peripheral enable register. Initially, register access is disabled because clock input is disabled. Enable IrDA operating clock input with the peripheral enable register before setting the register.

(3) During HALT mode, the IrDA function continues to run.

(4) The use of SAU initialization function (SS bit= 1) is prohibited during IrDA communication.

(5) The IRCR register bits IRRXINV, IRTXINV, and IRCKS[2:0] can be set only when IRE bit is 0.

21.1 Functions of LCD Controller/Driver

The functions of the LCD controller/driver in the RL78/I1C microcontrollers are as follows.

(1) Waveform A or B selectable
(2) The LCD driver voltage generator can switch internal voltage boosting method, capacitor split method, and external resistance division method.
(3) Automatic output of segment and common signals based on automatic display data register read
(4) The reference voltage to be generated when operating the voltage boost circuit can be selected from 16 steps (contrast adjustment).
(5) LCD blinking is available

Table 21-2 lists the maximum number of pixels that can be displayed in each display mode.

Table 21-2. Maximum Number of Pixels (1/3)

(a) 64-pin products

Drive Waveform for LCD Driver	LCD Driver Voltage Generator	Bias Mode	Number of Time Slices	Maximum Number of Pixels
Waveform A	External resistance division	–	Static	19 (19 segment signals, 1 common signal)
		1/2	2	38 (19 segment signals, 2 common signals)
			3	57 (19 segment signals, 3 common signals)
		1/3	3	
			4	76 (19 segment signals, 4 common signals)
			6	102 (17 segment signals, 6 common signals)
			8	120 (15 segment signals, 8 common signals)
		1/4	8	
	Internal voltage boosting	1/3	3	57 (19 segment signals, 3 common signals)
			4	76 (19 segment signals, 4 common signals)
			6	102 (17 segment signals, 6 common signals)
			8	120 (15 segment signals, 8 common signals)
		1/4	6	102 (17 segment signals, 6 common signals)
			8	120 (15 segment signals, 8 common signals)
	Capacitor split	1/3	3	57 (19 segment signals, 3 common signals)
			4	76 (19 segment signals, 4 common signals)
			6	102 (17 segment signals, 6 common signals)
			8	120 (15 segment signals, 8 common signals)
Waveform B	External resistance division, internal voltage boosting	1/3	3	57 (19 segment signals, 3 common signals)
			4	76 (19 segment signals, 4 common signals)
			6	102 (17 segment signals, 6 common signals)
			8	120 (15 segment signals, 8 common signals)
		1/4	8	
	Capacitor split	1/3	3	57 (19 segment signals, 3 common signals)
			4	76 (19 segment signals, 4 common signals)
			6	102 (17 segment signals, 6 common signals)
			8	120 (15 segment signals, 8 common signals)

Table 24-1. Interrupt Source List (1/4)

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]	100-pin	80-pin	64-pin
		Name	Trigger						
Maskable	0	INTWDTI	Watchdog timer interval[Note 3] (75% of overflow time+1/2f_{IL})	Internal	0004H	(A)	√	√	√
	1	INTLVI	Voltage detection[Note 4]		0006H		√	√	√
	2	INTP0[Note 5]	Pin input edge detection	External	0008H	(B)	√	√	√
	3	INTP1			000AH		√	√	√
	4	INTP2			000CH		√	√	√
	5	INTP3			000EH		√	√	√
	6	INTP4			0010H		√	√	√
	7	INTP5			0012H		√	√	√
	8	INTST2	UART2 transmission transfer end or buffer empty interrupt	Internal	0014H	(A)	√	√	√
	9	INTSR2	UART2 reception transfer end		0016H		√	√	√
	10	INTSRE2	UART2 reception communication error occurrence		0018H		√	√	√
	11	INTCR	End of high-speed on-chip oscillator clock frequency correction		001AH		√	√	√
	12	INTAES	AES encryption/decryption end		001CH		√	√	√
		INTAESF	AES encryption/decryption end of first block				√	√	√
	13	INTST0/ INTCSI00/ INTIIC00	UART0 transmission transfer end or buffer empty interrupt/CSI00 transfer end or buffer empty interrupt/IIC00 transfer end		001EH		√	√	√
	14	INTIICA0	End of IICA0 communication		0020H		√	√	√
	15	INTSR0	UART0 reception transfer end		0022H		√	√	√
	16	INTSRE0	UART0 reception communication error occurrence		0024H		√	√	√
		INTTM01H	End of timer channel 01 count or capture (at higher 8-bit timer operation)				√	√	√
	17	INTST1/ INTCSI10/ INTIIC10	UART1 transmission transfer end or buffer empty interrupt/CSI10 transfer end or buffer empty interrupt/IIC10 transfer end		0026H		√	√	√
	18	INTSR1	UART1 reception transfer end		0028H		√	√	√
	19	INTSRE1	UART1 reception communication error occurrence		002AH		√	√	√
		INTTM03H	End of timer channel 03 count or capture (at higher 8-bit timer operation)				√	√	√

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 42 indicates the lowest priority.

2. Basic configuration types (A) to (C) correspond to (A) to (C) in Figure 24-1.

3. When bit 7 (WDTINT) of the option byte (000C0H) is set to 1.

4. When bit 7 (LVIMD) of the voltage detection level register (LVIS) is cleared to 0.

<R> **5.** The input buffer power supply of P137 pins is connected to internal V_{DD}. For PIOR04 = 0, interrupts can be accepted even when a battery backup function is used and power is supplied from the VBAT pin.

39.4 Operations of 32-bit Multiply-accumulator

39.4.1 Basic operation

The register configuration shows as follow when multiplication or multiply-accumulation is executed.

■ Register configuration during unsigned multiplication

<Multiplier A>		<Multiplier B>		<Product>
32-bit		32-bit		64-bit
Unsigned		Unsigned		Unsigned
[MUL32UH, MUL32UL]	×	[MDBH, MDBL]	=	[MULR3, MULR2, MULR1, MULR0]

■ Register configuration during signed multiplication

<Multiplier A>		<Multiplier B>		<Product>
32-bit		32-bit		64-bit
Signed		Signed		Signed
[MUL32SH, MUL32SL]	×	[MDBH, MDBL]	=	[MULR3, MULR2, MULR1, MULR0]

■ Register configuration during unsigned multiply-accumulation

<Multiplier A>		<Multiplier B>		<Accumulated value>		<Product>
32-bit		32-bit		64-bit		64-bit
Unsigned		Unsigned		Unsigned		Unsigned
[MAC32UH, MAC32UL]	×	[MDBH, MDBL]	+	[MULR3, MULR2, MULR1, MULR0]	=	[MULR3, MULR2, MULR1, MULR0]

■ Register configuration during signed multiply-accumulation

<Multiplier A>		<Multiplier B>		<Accumulated value>		<Product>
32-bit		32-bit		64-bit		64-bit
Signed		Signed		Signed		Signed
[MAC32SH, MAC32SL]	×	[MDBH, MDBL]	+	[MULR3, MULR2, MULR1,MULR0]	=	[MULR3, MULR2, MULR1, MULR0]

39.4.2 Number of clocks for result availability

In case of multiplication or multiply-accumulation, the calculation is started automatically by setting upper 16-bit of the multiplier data (MULBH). Table 39-2 gives the number of clocks necessary to calculation.

Table 39-2. Number of Clocks Necessary to Calculation

Operation Mode	Operation	The Number of Clocks Necessary to Calculation				
		MULR0	MULR1	MULR2	MULR3	MACOF MACSF
Unsigned multiply	32 bits × 32 bits	2	4	5	5	5
Signed multiply	32 bits × 32 bits	2	4	5	5	5
Unsigned multiply-accumulate	32 bits × 32 bits + 64 bits	2	4	5	5	5
Signed multiply-accumulate	32 bits × 32 bits + 64 bits	2	4	5	5	5

Remark There is no difference in the clock number between the enabled and disabled fixed point modes.

39.6 Precautions for 32-bit Multiply-accumulator

39.6.1 Precautions during operation (MULST = 1)

Rewriting of the multiplication data register A (L)/(H), multiplication data register B (L)/(H), multiplication result register 0/1/2/3, and multiplication control register is prohibited during the operation. Otherwise, the operation result will be an undefined value.

Before rewriting to the multiplication data register B (H) as the operation start, rewriting the multiplication data register A (L)/(H), multiplication data register B (L), multiplication result register 0/1/2/3, and multiplication control register must be completed.

Table 40-5. Operation List (11/18)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Clocks	Flag		
				Note 1	Note 2		Z	AC	CY
16-bit operation	ADDW	AX, #word	3	1	–	AX, CY ← AX+word	×	×	×
		AX, AX	1	1	–	AX, CY ← AX+AX	×	×	×
		AX, BC	1	1	–	AX, CY ← AX+BC	×	×	×
		AX, DE	1	1	–	AX, CY ← AX+DE	×	×	×
		AX, HL	1	1	–	AX, CY ← AX+HL	×	×	×
		AX, !addr16	3	1	4	AX, CY ← AX+(addr16)	×	×	×
		AX, ES:!addr16	4	2	5	AX, CY ← AX+(ES:addr16)	×	×	×
		AX, saddrp	2	1	–	AX, CY ← AX+(saddrp)	×	×	×
		AX, [HL+byte]	3	1	4	AX, CY ← AX+(HL+byte)	×	×	×
		AX, ES: [HL+byte]	4	2	5	AX, CY ← AX+((ES:HL)+byte)	×	×	×
	SUBW	AX, #word	3	1	–	AX, CY ← AX – word	×	×	×
		AX, BC	1	1	–	AX, CY ← AX – BC	×	×	×
		AX, DE	1	1	–	AX, CY ← AX – DE	×	×	×
		AX, HL	1	1	–	AX, CY ← AX – HL	×	×	×
		AX, !addr16	3	1	4	AX, CY ← AX – (addr16)	×	×	×
		AX, ES:!addr16	4	2	5	AX, CY ← AX – (ES:addr16)	×	×	×
		AX, saddrp	2	1	–	AX, CY ← AX – (saddrp)	×	×	×
		AX, [HL+byte]	3	1	4	AX, CY ← AX – (HL+byte)	×	×	×
		AX, ES: [HL+byte]	4	2	5	AX, CY ← AX – ((ES:HL)+byte)	×	×	×
	CMPW	AX, #word	3	1	–	AX – word	×	×	×
		AX, BC	1	1	–	AX – BC	×	×	×
		AX, DE	1	1	–	AX – DE	×	×	×
		AX, HL	1	1	–	AX – HL	×	×	×
		AX, !addr16	3	1	4	AX – (addr16)	×	×	×
		AX, ES:!addr16	4	2	5	AX – (ES:addr16)	×	×	×
		AX, saddrp	2	1	–	AX – (saddrp)	×	×	×
		AX, [HL+byte]	3	1	4	AX – (HL+byte)	×	×	×
		AX, ES: [HL+byte]	4	2	5	AX – ((ES:HL)+byte)	×	×	×

Notes 1. Number of CPU clocks (f_{CLK}) when the internal RAM area, SFR area, or extended SFR area is accessed, or when no data is accessed.

2. Number of CPU clocks (f_{CLK}) when the code flash area is accessed.

Remark Number of clock is when program exists in the internal ROM (flash memory) area. If fetching the instruction from the internal RAM area, the number becomes double number plus 3 clocks at a maximum.