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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM9®
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	Audio Codec, EBI/EMI, IrDA, Memory Card, SmartCard, SSP, UART/USART, USB
Peripherals	AC'97, DMA, LCD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-BGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/socle/lh7a400n0b000b3a

Table 1. Functional Pin List (Cont'd)

PBGA PIN	CABGA PIN	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE
R11	P12	VDDA	Analog Power for PLL			
N12	M10					
P12	R13	VSSA	Analog Ground for PLL			
T11	N11					
D3	E4	nPOR	Power On Reset	Input	Input	
H6	D1	nURESET	User Reset; should be pulled HIGH for normal or JTAG operation.	Input (Schmitt)	Input	
D4	E2	WAKEUP	Wake Up	Input (Schmitt)	Input	
E4	F2	nPWRFL	Power Fail Signal	Input (Schmitt)	Input	
C2	D2	nEXTPWR	External Power	Input (Schmitt)	Input	
R13	R14	XTALIN	14.7456 MHz Crystal Oscillator pins. An external clock source can be connected to XTALIN leaving XTALOUT open.	Input	Input	
T13	R15	XTALOUT		LOW	LOW	
P16	N14	XTAL32IN	32.768 kHz Real Time Clock Crystal Oscillator pins. An external clock source can be connected to XTAL32IN leaving XTAL32OUT open.	Input	Input	
P15	M13	XTAL32OUT		Output	Output	
P14	M12	CLKEN	External Oscillator Clock Enable Output	LOW	LOW	8 mA
J6	J5	PGMCLK	Programmable Clock (14.7456 MHz MAX.)	LOW	LOW	8 mA
K11	P14	nCS0	Asynchronous Memory Chip Select 0	HIGH	HIGH	12 mA
K10	P16	nCS1	Asynchronous Memory Chip Select 1	HIGH	HIGH	12 mA
P13	N15	nCS2	Asynchronous Memory Chip Select 2	HIGH	HIGH	12 mA
M12	N16	nCS3/ nMMSPICS	• Asynchronous Memory Chip Select 3 • MultiMediaCard SPI Mode Chip Select	HIGH: nCS3	HIGH	12 mA

Table 1. Functional Pin List (Cont'd)

PBGA PIN	CABGA PIN	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE
L12	L11	D0	Data Bus	LOW	LOW	12 mA
M15	L13	D1				
N13	L14	D2				
L16	K11	D3				
L15	L16	D4				
L14	K14	D5				
H11	J15	D6				
K12	J12	D7				
J15	J10	D8				
J13	H16	D9				
J10	H14	D10				
H15	H11	D11				
H13	G16	D12				
G15	G9	D13				
G11	G14	D14				
G12	G12	D15				
F15	F15	D16				
F12	E15	D17				
E14	D16	D18				
D16	F12	D19				
H10	E13	D20				
D14	D14	D21				
F10	E12	D22				
A16	B16	D23				
A14	D12	D24				
B13	A16	D25				
C13	B13	D26				
E12	B14	D27				
G10	C12	D28				
B12	A14	D29				
B11	B12	D30				
D11	A12	D31				
M16	M15	A0/nWE1	• Asynchronous Address Bus • Asynchronous Memory Write Byte Enable 1	HIGH: nWE1	HIGH	12 mA
N14	M16	A1/nWE2	• Asynchronous Address Bus • Asynchronous Memory Write Byte Enable 2	HIGH: nWE2	HIGH	12 mA

Table 1. Functional Pin List (Cont'd)

PBGA PIN	CABGA PIN	SIGNAL	DESCRIPTION	RESET STATE	STANDBY STATE	OUTPUT DRIVE
L6	P4	PG2/nPCIOR	• GPIO Port G • I/O Read Strobe for PC Card (PCMCIA or CompactFlash) in single or dual card mode	LOW: PG2	No Change	8 mA
M6	R3	PG3/nPCIOW	• GPIO Port G • I/O Write Strobe for PC Card (PCMCIA or CompactFlash) in single or dual card mode	LOW: PG3	No Change	8 mA
N6	T2	PG4/nPCREG	• GPIO Port G • Register Memory Access for PC Card (PCMCIA or CompactFlash) in single or dual card mode	LOW: PG4	No Change	8 mA
M7	P5	PG5/nPCCE1	• GPIO Port G • Card Enable 1 for PC Card (PCMCIA or CompactFlash) in single or dual card mode. This signal and nPCCE2 are used by the PC Card for decoding low and high byte accesses.	LOW: PG5	No Change	8 mA
M8	R4	PG6/nPCCE2	• GPIO Port G • Card Enable 2 for PC Card (PCMCIA or CompactFlash) in single or dual card mode. This signal and nPCCE1 are used by the PC Card for decoding low and high byte accesses.	LOW: PG6	No Change	8 mA
N4	T3	PG7/PCDIR	• GPIO Port G • Direction for PC Card (PCMCIA or CompactFlash) in single or dual card mode	LOW: PG7	No Change	8 mA
P4	P6	PH0/ PCRESET1	• GPIO Port H • Reset Card 1 for PC Card (PCMCIA or CompactFlash) in single or dual card mode	Input: PH0	No Change	8 mA
R4	T4	PH1/CFA8/ PCRESET2	• GPIO Port H • Address Bit 8 for PC Card (CompactFlash) in single card mode • Reset Card 2 for PC Card (PCMCIA or CompactFlash) in dual card mode	Input: PH1	No Change	8 mA
T4	M7	PH2/ nPCSLOTE1	• GPIO Port H • Enable Card 1 for PC Card (PCMCIA or CompactFlash) in single or dual card mode. This signal is used for gating other control signals to the appropriate PC Card.	Input: PH2	No Change	8 mA
N7	T5	PH3/CFA9/ PCMCIAA25/ nPCSLOTE2	• GPIO Port H • Address Bit 9 for PC Card (CompactFlash) in single card mode • Address Bit 25 for PC Card (PCMCIA) in single card mode • Enable Card 2 for PC Card (PCMCIA or CompactFlash) in dual card mode. This signal is used for gating other control signals to the appropriate PC Card.	Input: PH3	No Change	8 mA
P8	R6	PH4/ nPCWAIT1	• GPIO Port H • WAIT Signal for Card 1 for PC Card (PCMCIA or CompactFlash) in single or dual card mode	Input: PH4	No Change	8 mA
P5	R7	PH5/CFA10/ PCMCIAA24/ nPCWAIT2	• GPIO Port H • Address Bit 10 for PC Card (CompactFlash) in single card mode • Address Bit 24 for PC Card (PCMCIA) in single card mode • WAIT Signal for Card 2 for PC Card (PCMCIA or CompactFlash) in dual card mode	Input: PH5	No Change	8 mA

Table 3. LCD Data Multiplexing

PBGA PIN	CABGA PIN	LCD DATA SIGNAL	STN						TFT	AD-TFT/ HR-TFT
			MONO 4-BIT		MONO 8-BIT		COLOR			
			SINGLE PANEL	DUAL PANEL	SINGLE PANEL	DUAL PANEL	SINGLE PANEL	DUAL PANEL		
K1	K2	LCDVD17								LOW
J5	K1	LCDVD16								LOW
R10	T13	LCDVD15				MLSTN7		CLSTN7	Intensity	Intensity
P10	R12	LCDVD14				MLSTN6		CLSTN6	BLUE4	BLUE4
T9	R11	LCDVD13				MLSTN5		CLSTN5	BLUE3	BLUE3
R9	T12	LCDVD12				MLSTN4		CLSTN4	BLUE2	BLUE2
N11	T11	LCDVD11				MLSTN3		CLSTN3	BLUE1	BLUE1
K8	P10	LCDVD10				MLSTN2		CLSTN2	BLUE0	BLUE0
L11	K10	LCDVD9				MLSTN1		CLSTN1	GREEN4	GREEN4
M11	M9	LCDVD8				MLSTN0		CLSTN0	GREEN3	GREEN3
M10	R10	LCDVD7		MLSTN3	MUSTN7	MUSTN7	CUSTN7	CUSTN7	GREEN2	GREEN2
M9	T10	LCDVD6		MLSTN2	MUSTN6	MUSTN6	CUSTN6	CUSTN6	GREEN1	GREEN1
N10	K9	LCDVD5		MLSTN1	MUSTN5	MUSTN5	CUSTN5	CUSTN5	GREEN0	GREEN0
L10	T9	LCDVD4		MLSTN0	MUSTN4	MUSTN4	CUSTN4	CUSTN4	RED4	RED4
N8	T8	LCDVD3	MUSTN3	MUSTN3	MUSTN3	MUSTN3	CUSTN3	CUSTN3	RED3	RED3
T7	R8	LCDVD2	MUSTN2	MUSTN2	MUSTN2	MUSTN2	CUSTN2	CUSTN2	RED2	RED2
R7	P8	LCDVD1	MUSTN1	MUSTN1	MUSTN1	MUSTN1	CUSTN1	CUSTN1	RED1	RED1
P7	M8	LCDVD0	MUSTN0	MUSTN0	MUSTN0	MUSTN0	CUSTN0	CUSTN0	RED0	RED0

NOTES:
1. The Intensity bit is identically generated for all three colors.
2. MU = Monochrome Upper
3. CU = Color Upper
4. CL = Color Lower

Table 4. 256-Ball PBGA Package Numerical Pin List (Cont'd)

BGA PIN	SIGNAL	RESET STATE	STANDBY STATE
F11	A19	LOW	LOW
F12	D17	LOW	LOW
F13	VDD		
F14	A16/SB0	LOW: SBANK0	LOW
F15	D16	LOW	LOW
F16	A15/SA13	LOW: SA13	LOW
G1	COL2	HIGH	HIGH
G2	COL3	HIGH	HIGH
G3	VSS		
G4	COL4	HIGH	HIGH
G5	COL5	HIGH	HIGH
G6	VSSC		
G7	VDD		
G8	A25/SCIO	LOW: A25	LOW
G9	SCKE3	LOW	LOW
G10	D28	LOW	LOW
G11	D14	LOW	LOW
G12	D15	LOW	LOW
G13	A14/SA12	LOW: SA12	LOW
G14	A13/SA11	LOW: SA11	LOW
G15	D13	LOW	LOW
G16	A12/SA10	LOW: SA10	LOW
H1	COL6	HIGH	HIGH
H2	COL7	HIGH	HIGH
H3	TBUZ	LOW	LOW
H4	SSPCLK	LOW	LOW
H5	VSSC		
H6	nURESET	Input	Input
H7	VSS		
H8	PF3/INT3	Input: PF3	No Change
H9	VSS		
H10	D20	LOW	LOW
H11	D6	LOW	LOW
H12	VSSC		
H13	D12	LOW	LOW
H14	A11/SA9	LOW: SA9	LOW
H15	D11	LOW	LOW
H16	A10/SA8	LOW: SA8	LOW
J1	SSPRX	Input	Input
J2	SSPTX	LOW	LOW
J3	SSPFRM/nSSPFRM	Input: nSSPFRM	Input
J4	VDDC		
J5	PA0/LCDVD16	Input: PA0	No Change
J6	PGMCLK	LOW	LOW
J7	UARTRX2	Input	Input

Table 5. 256-Ball CABGA Package Numerical Pin List

CABGA PIN	SIGNAL	RESET STATE	STANDBY STATE
A1	ACOUT	LOW	LOW
A2	ACBITCLK	Input	Input
A3	PF7/INT7/PCRDY2	Input: PF7 (Schmitt)	No Change
A4	PF6/INT6/PCRDY1	Input: PF6 (Schmitt)	No Change
A5	PF0/INT0	Input: PF0 (Schmitt)	No Change
A6	nPWME1	Input	Input
A7	A27/SCRST	LOW: A27	LOW
A8	DQM3	HIGH	HIGH
A9	DQM1	HIGH	HIGH
A10	CS7/SCKE0	LOW: CS7	LOW
A11	SCKE3	LOW	LOW
A12	D31	LOW	LOW
A13	nSWE	HIGH	HIGH
A14	D29	LOW	LOW
A15	nSCS1	HIGH	HIGH
A16	D25	LOW	LOW
B1	MMCCMD/MMSPIDIN	Input: MMCCMD	Input
B2	ACSYNC	LOW	LOW
B3	PF3/INT3	Input: PF3 (Schmitt)	No Change
B4	PF1/INT1	Input: PF1 (Schmitt)	No Change
B5	PWM1	Input	Input
B6	PWM0	Input	Input
B7	A26/SCCLK	LOW: A26	LOW
B8	VSS		
B9	DQM2	HIGH	HIGH
B10	SCLK	LOW	LOW
B11	nCAS	HIGH	HIGH
B12	D30	LOW	LOW
B13	D26	LOW	LOW
B14	D27	LOW	LOW
B15	A23	LOW	LOW
B16	D23	LOW	LOW
C1	TMS	Input with Pull-up	Input with Pull-up
C2	TCK	Input	Input
C3	MMCCLK/MMSPICLK	LOW: MMCCLK	LOW
C4	VDDC		
C5	PF4/INT4/SCVCCEN	Input: PF4 (Schmitt)	LOW if SCI is Enabled; otherwise, No Change
C6	VSS		
C7	nPWME0	Input	Input
C8	nOE	HIGH	HIGH
C9	DQM0	HIGH	HIGH
C10	VDD		
C11	nRAS	HIGH	HIGH

Table 5. 256-Ball CABGA Package Numerical Pin List

CABGA PIN	SIGNAL	RESET STATE	STANDBY STATE
F7	VSS		
F8	nWE0	HIGH	HIGH
F9	VDD		
F10	VDDC		
F11	VDD		
F12	D19	LOW	LOW
F13	A17/SB1	LOW	LOW
F14	VDD		
F15	D16	LOW	LOW
F16	A15/SA13	LOW	LOW
G1	COL1	HIGH	HIGH
G2	COL0	HIGH	HIGH
G3	UARTRX2	Input	Input
G4	UARTDSR2	Input	Input
G5	UARTIRTX1	LOW	LOW
G6	UARTIRRX1	Input	Input
G7	VSSC		
G8	VDD		
G9	D13	LOW	LOW
G10	A13/SA11	LOW	LOW
G11	A14/SA12	LOW	LOW
G12	D15	LOW	LOW
G13	VSS		
G14	D14	LOW	LOW
G15	A12/SA10	LOW	LOW
G16	D12	LOW	LOW
H1	COL7	HIGH	HIGH
H2	COL6	HIGH	HIGH
H3	COL2	HIGH	HIGH
H4	VSSC		
H5	COL3	HIGH	HIGH
H6	COL4	HIGH	HIGH
H7	COL5	HIGH	HIGH
H8	VSSC		
H9	VSS		
H10	A10/SA8	LOW	LOW
H11	D11	LOW	LOW
H12	A11/SA9	LOW	LOW
H13	VDD		
H14	D10	LOW	LOW
H15	A9/SA7	LOW	LOW
H16	D9	LOW	LOW
J1	TBUZ	LOW	LOW

Table 5. 256-Ball CABGA Package Numerical Pin List

CABGA PIN	SIGNAL	RESET STATE	STANDBY STATE
L13	D1	LOW	LOW
L14	D2	LOW	LOW
L15	A2/SA0	LOW	LOW
L16	D4	LOW	LOW
M1	PB1/UARTTX3	Input: PB1	LOW if UART3 is Enabled, otherwise No Change
M2	PB2/UARTRX3	Input: PB2	No Change
M3	PB3/UARTCTS3	Input: PB3	No Change
M4	PB7/SMBCLK	Input: PB7	Input if SMB is Enabled, otherwise No Change
M5	PC3/LCDREV	LOW: PC3	No Change
M6	PG0/nPCOE	LOW: PG0	No Change
M7	PH2/nPCSLOTE1	Input: PH2	No Change
M8	LCDVD0	LOW	LOW
M9	PD0/LCDVD8	LOW: PD0	LOW if Dual-Panel LCD is Enabled; otherwise, No Change
M10	VDDA		
M11	VSS		
M12	CLKEN	LOW	LOW
M13	XTAL32OUT	Output	Output
M14	VSS		
M15	A0/nWE1	HIGH: nWE1	HIGH
M16	A1/nWE2	HIGH: nWE2	HIGH
N1	PB5/UARTDSR3	Input: PB5	No Change
N2	PB6/SWID/SMBD	Input: PB6	Input if SMB is Enabled, otherwise No Change
N3	VSSC		
N4	PC5/LCDCLS	LOW: PC5	No Change
N5	PC7/LCDSPL	LOW: PC7	No Change
N6	VDD		
N7	VSSC		
N8	VDD		
N9	LCDDCLK	LOW	LOW
N10	VSSC		
N11	VSSA		
N12	VDD		
N13	VDD		
N14	XTAL32IN	Input	Input
N15	nCS2	HIGH	HIGH
N16	nCS3/nMMSPICS	HIGH: nCS3	HIGH
P1	PC0/UARTTX1	LOW: PC0	No Change
P2	PC1/LCDPS	LOW: PC1	No Change
P3	PC4/LCDSPS	LOW: PC4	No Change
P4	PG2/nPCIOR	LOW: PG2	No Change
P5	PG5/nPCCE1	LOW: PG5	No Change
P6	PH0/PCRESET1	Input: PH0	No Change

Table 5. 256-Ball CABGA Package Numerical Pin List

CABGA PIN	SIGNAL	RESET STATE	STANDBY STATE
P7	PH6/AC97RESET	Input: PH6	No Change
P8	LCDVD1	LOW	LOW
P9	LCDENAB/LCDM	LOW: LCDENAB	LOW
P10	PD2/LCDVD10	LOW: PD2	No Change
P11	VDD		No Change
P12	VDDA		
P13	nTEST1	Input with Pull-up	Input with Pull-up
P14	nCS0	HIGH	HIGH
P15	nTEST0	Input with Pull-up	Input with Pull-up
P16	nCS1	HIGH	HIGH
R1	PC2/LCDVDDEN	LOW: PC2	No Change
R2	PC6/LCDHRLP	LOW: PC6	No Change
R3	PG3/nPCIOW	LOW: PG3	No Change
R4	PG6/nPCCE2	LOW: PG6	No Change
R5	VSSC		
R6	PH4/nPCWAIT1	Input: PH4	No Change
R7	PH5/CFA10/PCMCIAA24/nPCWAIT2	Input: PH5	No Change
R8	LCDVD2	LOW	LOW
R9	LCDLP	LOW	LOW
R10	PE3/LCDVD7	Input: PE3	No Change
R11	PD5/LCDVD13	LOW: PD5	No Change
R12	PD6/LCDVD14	LOW: PD6	No Change
R13	VSSA		
R14	XTALIN	Input	Input
R15	XTALOUT	LOW	LOW
R16	USBDN	Input	Input
T1	PG1/nPCWE	LOW: PG1	No Change
T2	PG4/nPCREG	LOW: PG4	No Change
T3	PG7/PCDIR	LOW: PG7	No Change
T4	PH1/CFA8/PCRESET2	Input: PH1	No Change
T5	PH3/CFA9/PCMCIAA25/nPCSLOTE2	Input: PH3	No Change
T6	PH7/nPCSTATRE	Input: PH7	No Change
T7	LCDFP	LOW	LOW
T8	LCDVD3	LOW	LOW
T9	PE0/LCDVD4	Input: PE0	LOW if 8-bit LCD is Enabled, otherwise No Change
T10	PE2/LCDVD6	Input: PE2	No Change
T11	PD3/LCDVD11	LOW: PD3	No Change
T12	PD4/LCDVD12	LOW: PD4	No Change
T13	PD7/LCDVD15	LOW: PD7	No Change
T14	WIDTH0	Input (Schmitt)	Input
T15	WIDTH1	Input (Schmitt)	Input
T16	USBDP	Input	Input

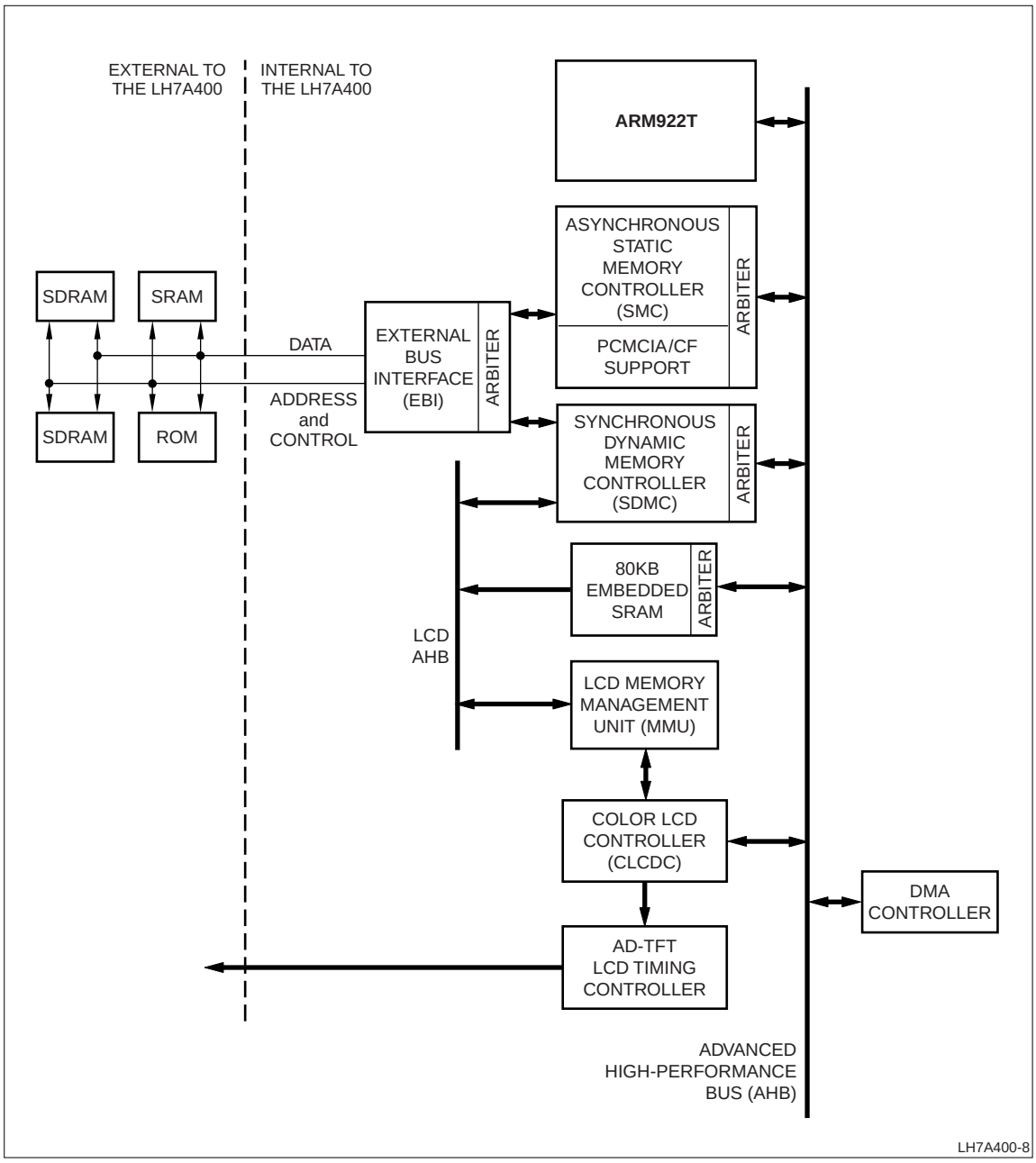


Figure 5. External Bus Interface Block Diagram

The Asynchronous Memory Controller has six main functions:

- Memory bank select
- Access sequencing
- Wait states generation
- Byte lane write control
- External bus interface
- CompactFlash or PCMCIA interfacing.

Synchronous Memory Controller

The Synchronous memory controller provides a high speed memory interface to a wide variety of Synchronous memory devices, including SDRAM, Synchronous Flash and Synchronous ROMs.

The key features of the controller are:

- LCD DMA port for high bandwidth
- Up to four Synchronous Memory banks that can be independently set up
- Special configuration bits for Synchronous ROM operation
- Ability to program Synchronous Flash devices using write and erase commands
- On booting from Synchronous ROM, (and optionally with Synchronous Flash), a configuration sequence is performed before releasing the processor from reset
- Data is transferred between the controller and the SDRAM in quad-word bursts. Longer transfers within the same page are concatenated, forming a seamless burst
- Programmable for 16- or 32-bit data bus size
- Two reset domains are provided to enable SDRAM contents to be preserved over a ‘soft’ reset
- Power saving Synchronous Memory SCKE and external clock modes provided.

MultiMediaCard (MMC)

The MMC adapter combines all of the requirements and functions of an MMC host. The adapter supports the full MMC bus protocol, defined by the MMC Definition Group’s specification v.2.11. The controller can also implement the SPI interface to the cards.

INTERFACE DESCRIPTION AND MMC OVERVIEW

The MMC controller uses the three-wire serial data bus (clock, command, and data) to transfer data to and from the MMC card, and to configure and acquire status information from the card’s registers.

MMC bus lines can be divided into three groups:

- Power supply: VDD and VSS
- Data Transfer: MMCCMD, MMCDATA
- Clock: MMCLK.

MULTIMEDIACARD ADAPTER

The MultiMediaCard Adapter implements MultiMediaCard specific functions, serves as the bus master for the MultiMediacard Bus and implements the standard interface to the MultiMediaCard Cards (card initialization, CRC generation and validation, command/response transactions, etc.).

Smart Card Interface (SCI)

The SCI (ISO7816) interfaces to an external Smart Card reader. The SCI can autonomously control data transfer to and from the smart card. Transmit and receive data FIFOs are provided to reduce the required interaction between the CPU core and the peripheral.

SCI FEATURES

- Supports asynchronous T0 and T1 transmission protocols
- Supports clock rate conversion factor F = 372, with bit rate adjustment factors D = 1, 2, or 4 supported
- Eight-character-deep buffered Tx and Rx paths
- Direct interrupts for Tx and Rx FIFO level monitoring
- Interrupt status register
- Hardware-initiated card deactivation sequence on detection of card removal
- Software-initiated card deactivation sequence on transaction complete
- Limited support for synchronous Smart Cards via registered input/output.

PROGRAMMABLE PARAMETERS

- Smart Card clock frequency
- Communication baud rate
- Protocol convention
- Card activation/deactivation time
- Check for maximum time for first character of Answer to Reset - ATR reception
- Check for maximum duration of ATR character stream
- Check for maximum time of receipt of first character of data stream
- Check for maximum time allowed between characters
- Character guard time
- Block guard time
- Transmit/receive character retry.

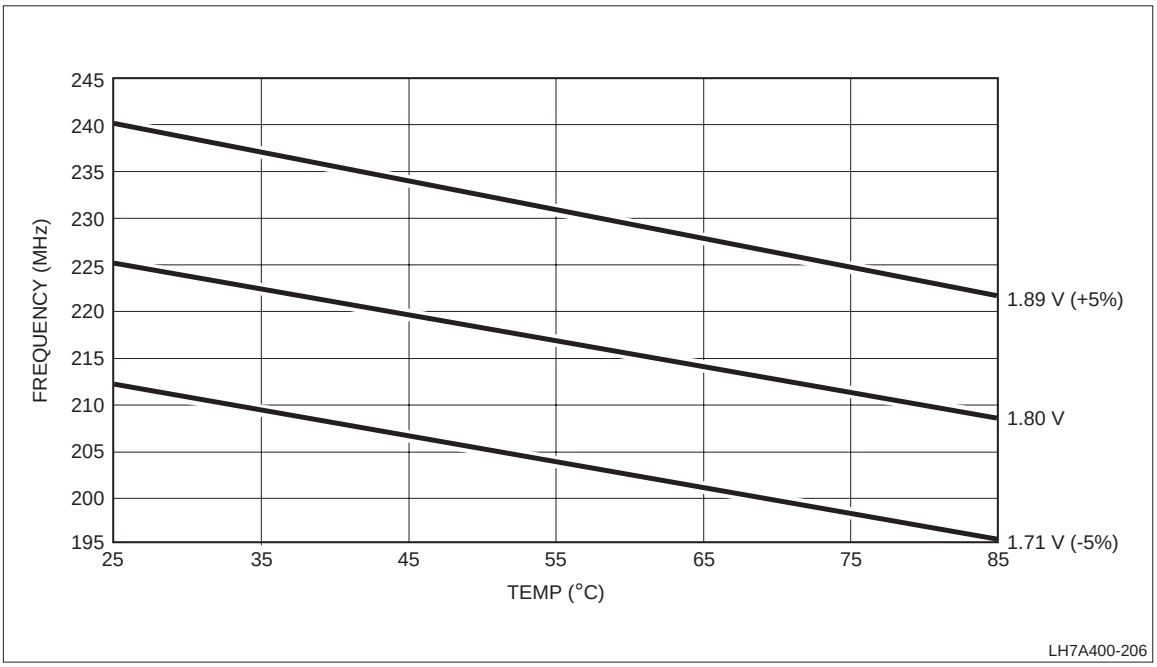


Figure 6. Temperature/Voltage/Speed Chart

Table 10. AC Signal Characteristics

SIGNAL	TYPE	LOAD	SYMBOL	MIN.	MAX.	DESCRIPTION
ASYNCHRONOUS MEMORY INTERFACE SIGNALS (+ wait states × C)[1]						
A[27:0]	Output	50 pF	tRC	4C ns		Read Cycle Time
	Output	50 pF	tWC	4C ns		Write Cycle Time
	Output	50 pF	tAW	2C – 10 ns		Address Valid to Write Edge
	NA		None	1C ns	1C ns	Wait State Width
D[31:0]	Output	50 pF	tDW	1C – 9 ns		Data Valid to Write Edge
			tDH	1C + 3 ns		Data Hold after Write Edge
	Input		tAA	3C – 20 ns		Address Valid to Data Valid
			tOH	0 ns		Data Output Hold
nCS[3:0]/CS[7:6]	Output	30 pF	tCO	3C – 20 ns		Chip Select Valid to Data Valid (Read)
			tCW		1C – 10 ns	Chip Select Valid to Write edge
			tAS (Write)	1C ns		Address Valid to Chip Select Valid (Address setup time)
			tAS (Read)	0		Address Valid to Chip Select Valid (Address setup time)
nWE[3:0]	Output	30 pF	tWP	1C – 10 ns		Write Pulse Width
			tWHZ	0 ns		Write Edge to High Z on SRAM
nOE	Output	30 pF	tOE		2C – 20 ns	Output Enable Valid to Data Valid
			tOHZ	0 ns		Output Enable invalid to High Z on SRAM
SYNCHRONOUS MEMORY INTERFACE SIGNALS						
SA[13:0]	Output	50 pF	tOVA		7.5 ns	Address Valid
			tOHA	1.5 ns		Address Hold
SA[17:16]/SB[1:0]	Output	50 pF	tOVB		7.5 ns	Bank Select Valid
D[31:0]	Output	50 pF	tOVD	2 ns	7.5 ns	Data Valid
	Input		tISD	2.5 ns		Data Setup
			tIHD	1.5 ns		Data Hold
nCAS	Output	30 pF	tOVCA	2 ns	7.5 ns	CAS Valid
			tOHCA	2 ns		CAS Hold
nRAS	Output	30 pF	tOVRA	2 ns	7.5 ns	RAS Valid
			tOHRA	2 ns		RAS Hold
nSWE	Output	30 pF	tOVSDW	2 ns	7.5 ns	Write Enable Valid
			tOHSDW	2 ns		Write Enable Hold
SCKE[1:0]	Output	30 pF	tOVC	2 ns	7.5 ns	Clock Enable Valid
DQM[3:0]	Output	30 pF	tOVDQ	2 ns	7.5 ns	Data Mask Valid
nSCS[3:0]	Output	30 pF	tOVSC	2 ns	7.5 ns	Synchronous Chip Select Valid
			tOHSC	2 ns		Synchronous Chip Select Hold
PCMCIA INTERFACE SIGNALS (+ wait states × C)[1]						
nPCREG	Output	30 pF	tOVDREG		1C	nREG Valid
			tOHDREG	4C – 5 ns		nREG Hold
D[31:0]	Output	50 pF	tOVD		1C	Data Valid
			tOHD	4C – 5 ns		Data Hold
	Input		tISD		1C - 10 ns	Data Setup Time
			tIHD	4C – 5 ns		Data Hold Time
nPCCE1	Output	30 pF	tOVCE1		1C	Chip Enable 1 Valid
			tOHCE1	4C – 5 ns		Chip Enable 1 Hold
nPCCE2	Output	30 pF	tOVCE2		1C	Chip Enable 2 Valid
			tOHCE2	4C – 5 ns		Chip Enable 2 Hold
nPCOE	Output	30 pF	tOVOE		1C + 1 ns	Output Enable Valid
			tOHOE	3C – 5 ns		Output Enable Hold
nPCWE	Output	30 pF	tOVWE		1C + 1 ns	Write Enable Valid
			tOHWE	3C – 5 ns		Write Enable Hold
PCDIR	Output	30 pF	tOVPCD		1C	Card Direction Valid
			tOHPCD	4C – 5 ns		Card Direction Hold

Table 10. AC Signal Characteristics (Cont'd)

SIGNAL	TYPE	LOAD	SYMBOL	MIN.	MAX.	DESCRIPTION
MMC INTERFACE SIGNALS						
MMCCMD	Output	100 pF	tOVCMD		3 ns	MMC Command Valid
			tOHCMD	3 ns		MMC Command Hold
MMCDATA	Output	100 pF	tOVDAT		3 ns	MMC Data Valid
			tOHDAT	3 ns		MMC Data Hold
MMCDATA	Input		tISDAT	5 ns		MMC Data Setup
			tIHDAT	5 ns		MMC Data Hold
MMCCMD	Input		tISCMD	5 ns		MMC Command Setup
			tIHCMD	5 ns		MMC Command Hold
AC97 INTERFACE SIGNALS						
ACOUT/ACSYNC	Output	30 pF	tOVAC97		15 ns	AC97 Output Valid/Sync Valid
			tOHAC97	10 ns		AC97 Output Hold/Sync Hold
ACIN	Input		tISAC97	10 ns		AC97 Input Setup
			tIHAC97	2.5 ns		AC97 Input Hold
ACBITCLK	Input		tACBITCLK	72 ns	90 ns	AC97 Clock Period
SYNCHRONOUS SERIAL PORT (SSP)						
SSPFRM	Input		tISSSPFRM	14 ns		SSPFRM Input Valid
SSPTX	Output	50 pF	tOVSSPOUT		14 ns	SSP Transmit Valid
SSPRX	Input		tISSSPIN	14 ns		SSP Receive Setup
AUDIO CODEC INTERFACE (ACI)						
ACOUT/ACSYNC	Output	30 pF	tOS	TBD	TBD	ACOUT delay from rising clock edge
			tOH	TBD	TBD	ACOUT Hold
ACIN	Input		tIS	TBD	TBD	ACIN Setup
			tIH	TBD	TBD	ACIN Hold

NOTES:
1. 'nC' in the MIN./MAX. columns indicates the number of system clock (HCLK) periods after valid address.
2. For Output Drive strength specifications, refer to Table 1.

SMC Waveforms

Figure 8 and Figure 9 show the waveform and timing for an External Asynchronous Memory Write. Note that the deassertion of nWE can precede the deassertion of nCS by a maximum of one HCLK, or at minimum, can coincide (see Table 10). Figure 10 and Figure 11 show the waveform and timing for an External Asynchronous Memory Read.

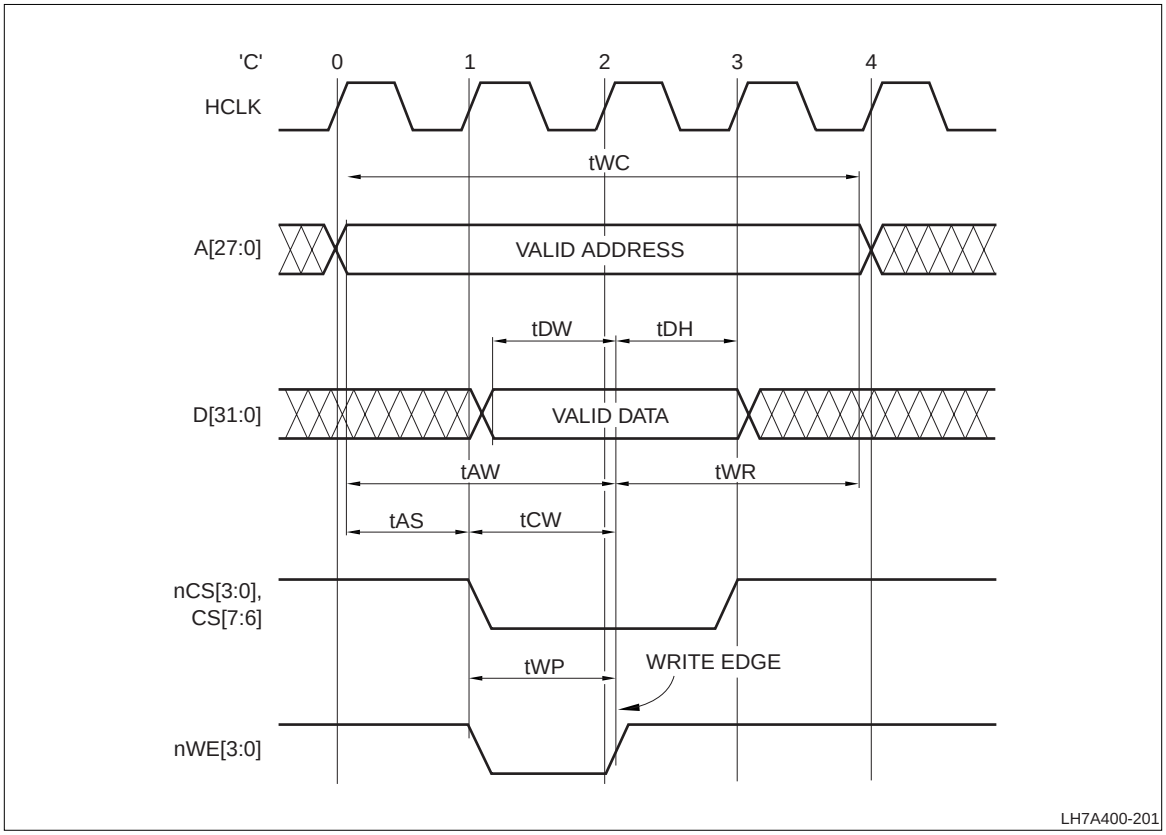


Figure 8. External Asynchronous Memory Write with 0 Wait States (BCRx:WST1 = 0b000)

Synchronous Memory Controller Waveforms

Figure 12 shows the waveform and timing for a Synchronous Burst Read (page already open). Figure 13 shows the waveform and timing for Synchronous memory to Activate a Bank and Write.

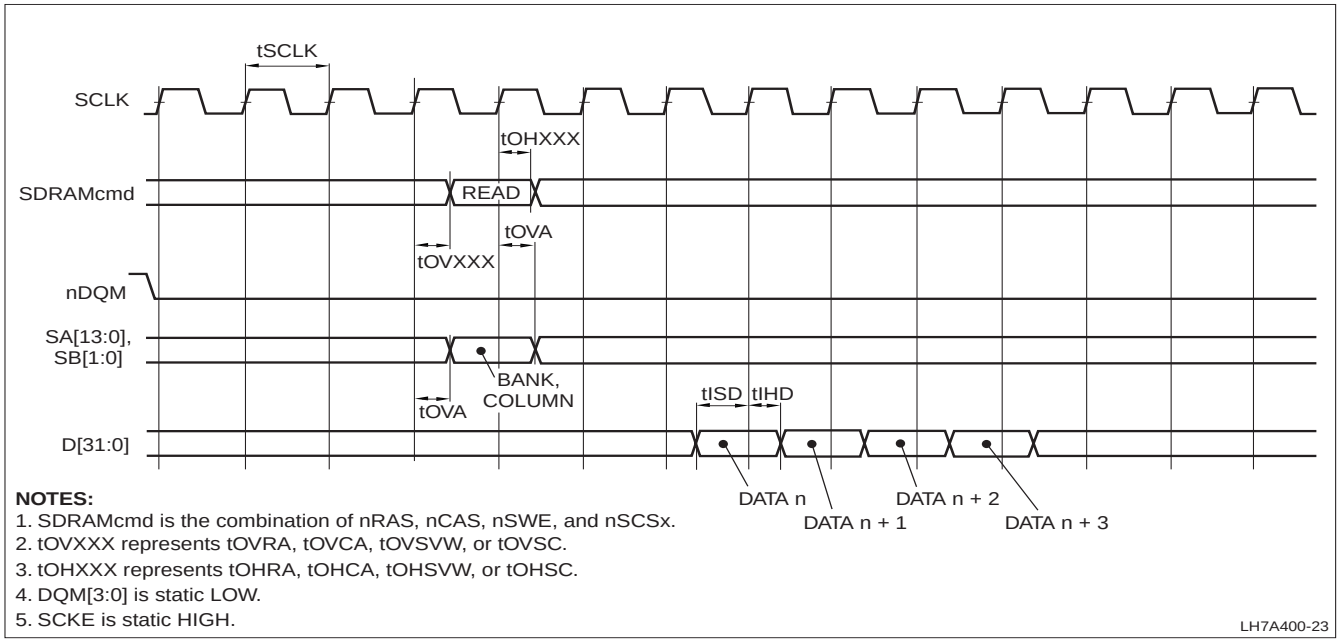


Figure 12. Synchronous Burst Read

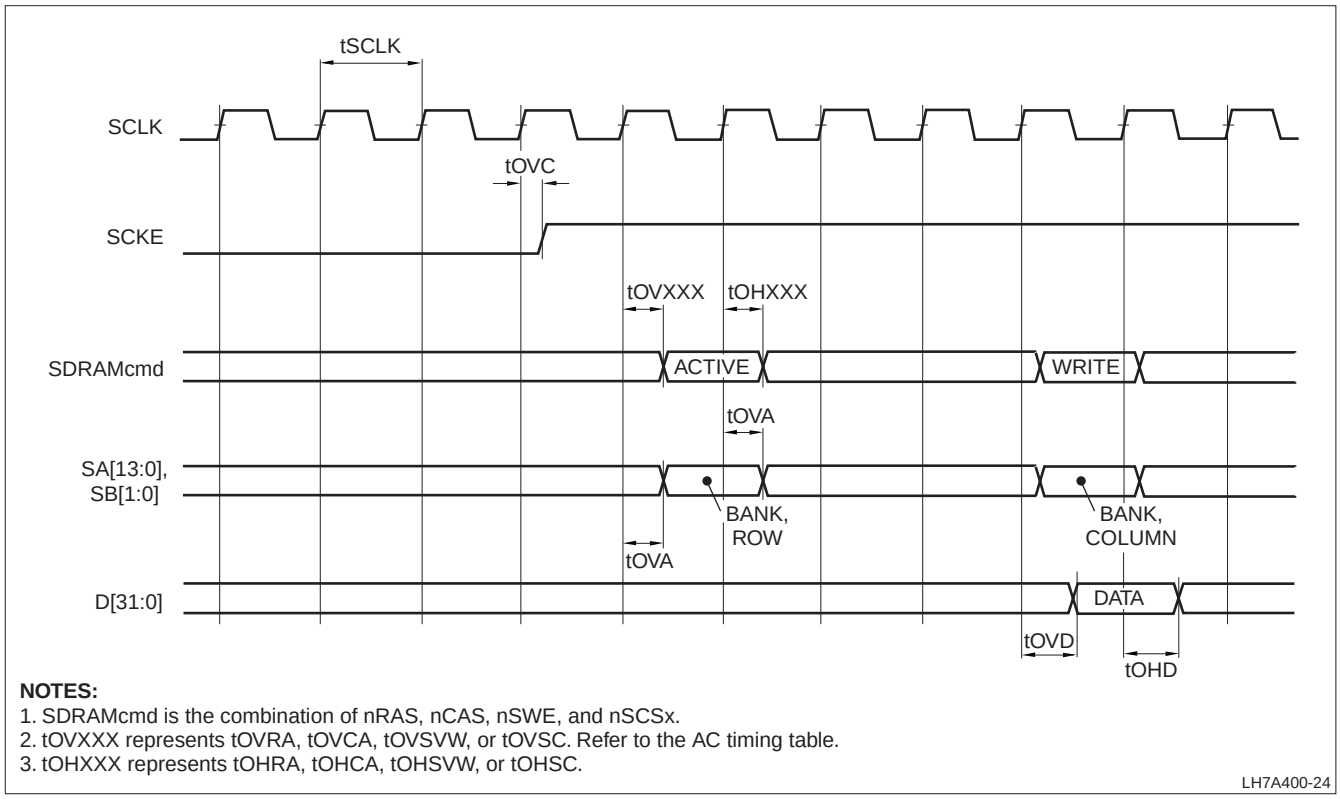
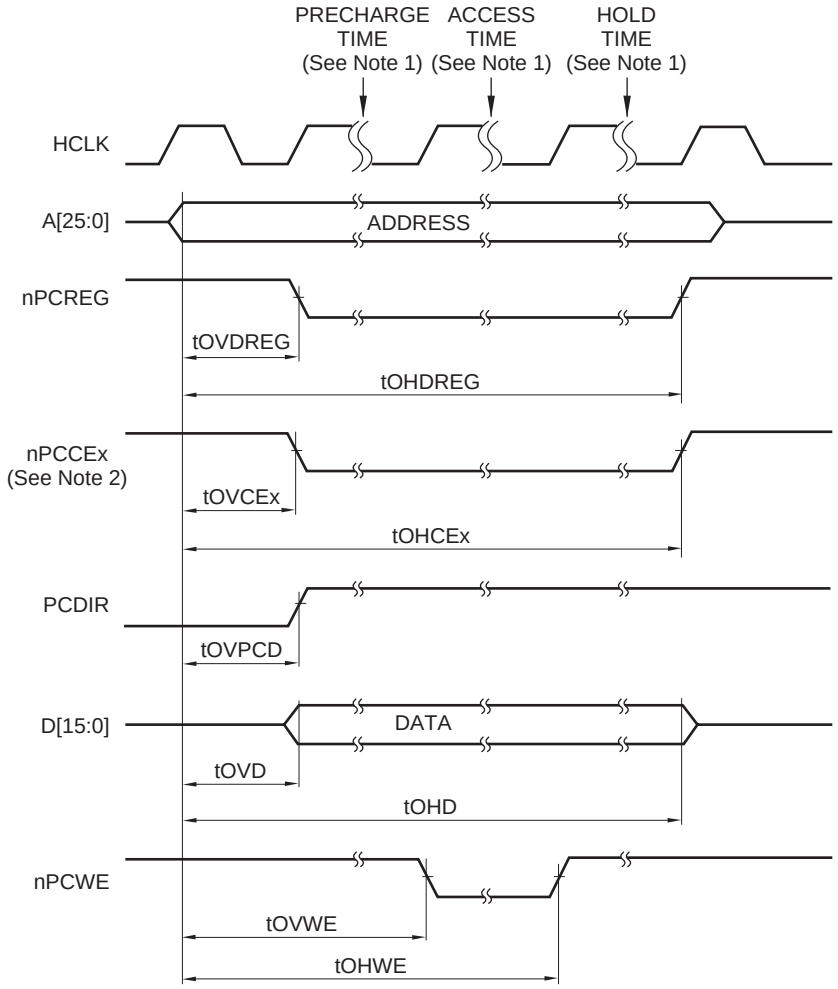


Figure 13. Synchronous Bank Activate and Write



NOTES:

1. Precharge time, access time, and hold time are programmable wait-state times.
2.

nPCCE1	nPCCE2	TRANSFER TYPE
0	0	Common Memory
0	1	Attribute Memory
1	0	I/O
1	1	None

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Figure 15. PCMCIA Write Transfer

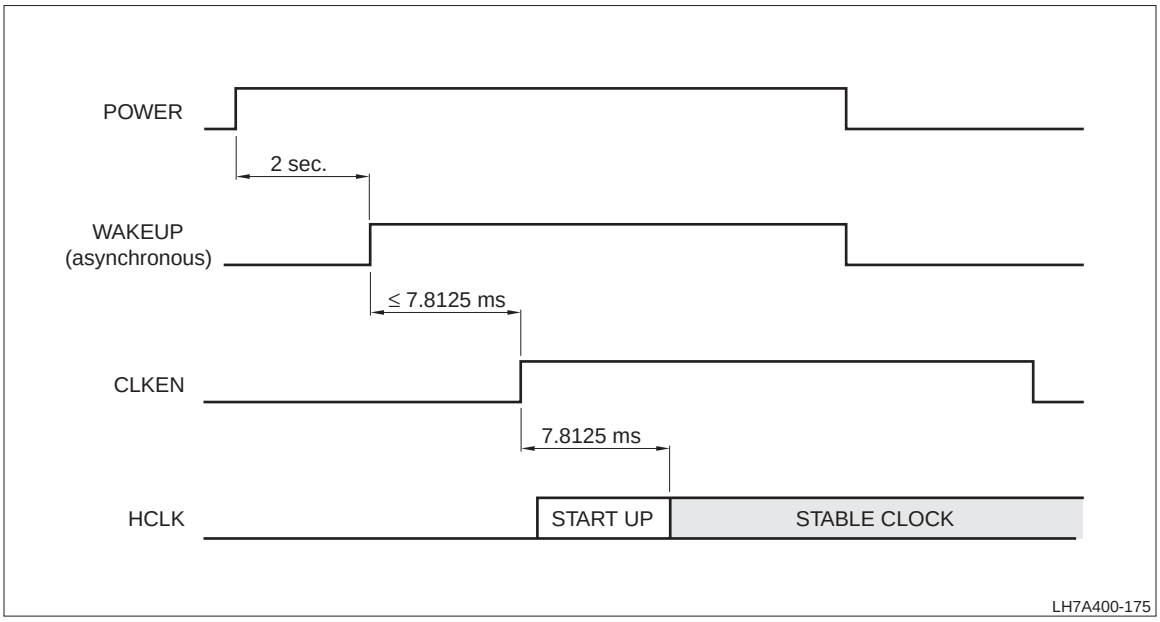
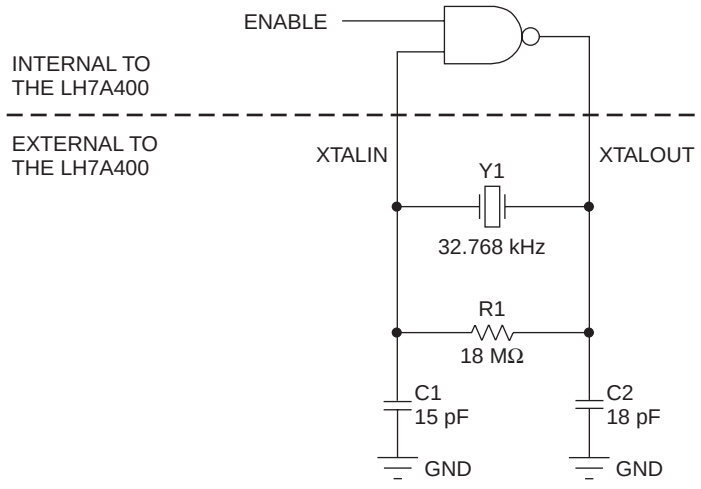


Figure 23. Signal Timing After Reset



NOTES:
1. Y1 is a parallel-resonant type crystal. (See table)
2. The nominal values for C1 and C2 shown are for a crystal specified at 12.5 pF load capacitance (CL).
3. The values for C1 and C2 are dependent upon the cystal's specified load capacitance and PCB stray capacitance.
4. R1 must be in the circuit.
5. Ground connections should be short and return to the ground plane which is connected to the processor's core ground pins.
6. Tolerance for R1, C1, C2 is ≤ 5%.

RECOMMENDED CRYSTAL SPECIFICATIONS

PARAMETER	DESCRIPTION
32.768 kHz Crystal	Parallel Mode
Tolerance	±30 ppm
Aging	±3 ppm
Load Capacitance	12.5 pF
ESR (MAX.)	50 kΩ
Drive Level	1.0 µW (MAX.)
Recommended Part	MTRON SX1555 or equivalent

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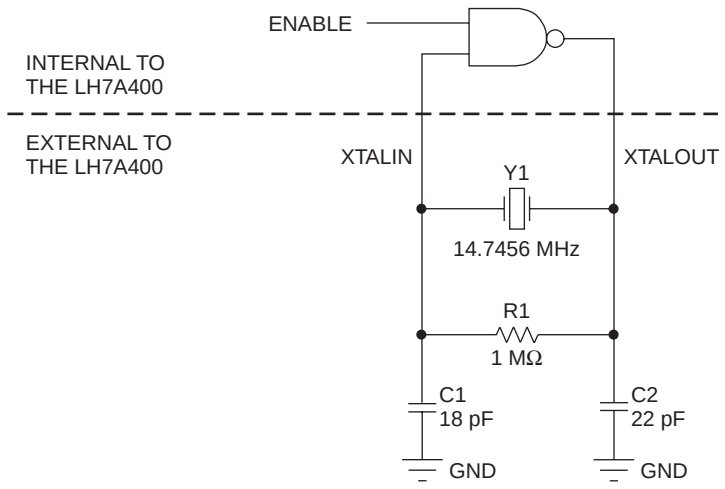
Figure 24. 32.768 kHz External Oscillator Components and Schematic



NOTES:
1. Y1 is a parallel-resonant type crystal. (See table)
2. The nominal values for C1 and C2 shown are for a crystal specified at 18 pF load capacitance (CL).
3. The values for C1 and C2 are dependent upon the cystal's specified load capacitance and PCB stray capacitance.
4. R1 must be in the circuit.
5. Ground connections should be short and return to the ground plane which is connected to the processor's core ground pins.
6. Tolerance for R1, C1, C2 is ≤ 5%.

RECOMMENDED CRYSTAL SPECIFICATIONS

PARAMETER	DESCRIPTION
14.7456 MHz Crystal	(AT-Cut) Parallel Mode
Tolerance	±50 ppm
Stability	±100 ppm
Aging	±5 ppm
Load Capacitance	18 pF
ESR (MAX.)	40 Ω
Drive Level	100 µW (MAX.)
Recommended Part	MTRON SX2050 or equivalent

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Figure 25. 14.7456 MHz External Oscillator Components and Schematic

CONTENT REVISIONS

This document contains the following changes to content, causing it to differ from previous versions.

Table 12. Record of Revisions

DATE	PAGE NO.	PARAGRAPH OR ILLUSTRATION	SUMMARY OF CHANGES
8-19-2003	1	Features	256-ball CABGA package added
	3-11	Table 1	CABGA Pins added; VDDA1/VDDA2 combined to VDDA; VSSA1/VSSA2 combined to VSSA
	12	Table 3	Signal ordering corrected
	12-18	Table 4	Table title added to differentiate between PBGA and CABGA packages
	18-24	Table 5	CABGA numerical pin list table added
	39	Figure 7 and Figure 8	'CSx' added to figures
	41-42	Figures 11 and 12	PCDIR signal corrected in PCMCIA timing diagrams
	44	Table 10 and Figure 16	tOSC14 added to both table and figure; XTAL14 added to figure; tPLLL added to table
	45-47	Figures 19-21 and Printed Circuit Board Layout Practices	Figures and text added
	49	Figure 23	Figure added for CABGA package
11-15-03	1	Text	Corrected minor text errors; added separate Commercial and Industrial temperature specification.
	2	Figure 1	Updated to show ALI Interface
	34	'Recommended Operating Conditions'	Broke out "Commercial" and "Industrial" speed ranges.
	39	Table 10	Minor corrections to type.
	39	Table 10	Added ACI timing.
	54	Figure 27	PBGA package drawing added.
6-21-04	11	Table 1	Changed names of BOOTWIDTH0 and BOOTWIDTH1 to WIDTH0 and WIDTH1 for consistency with other Sharp SoCs.
	53	Figure 26; text	Revised text and drawing to indicate that the VSSA pin must be grounded
	50	Table 11	Added table.
12-07-04	ALL		Rolled revision to Version 1.0
	1	Text	Run current corrected to 125 mA and Halt to 25 mA
	34	Table 7, Figure 6	Added table and accompanying graph for speed/temperature/voltage
	36	'DC Specifications'	Added IRUN, IHALT, and ISTANDBY; corrected IIN.
	37	Table 8	Corrected values in Table 8.
	39	Table 10	Changed Asynchronous Memory timing to match SRAM datasheet parameter naming conventions. Corrected Synchronous Memory times; added synchronous memory Address Hold time.
	41-44	Figure 8 - Figure 11	Changed Asynchronous Memory timing diagrams to match renamed parameters.
	51	Text and Figure 23	Clarification made to timing for cold boot power-on sequence.
12-13-04	36	'DC Specifications'	Added IIN without pullup resistors.