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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | ARM9® |
| Core Size | 32-Bit Single-Core |
| Speed | 200MHz |
| Connectivity | Audio Codec, EBI/EMI, IrDA, Memory Card, SmartCard, SSP, UART/USART, USB |
| Peripherals | AC'97, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 60 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 80K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 256-LFBGA |
| Supplier Device Package | 256-CABGA (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/socle/lh7a400n0f000b5 |

**Table 1. Functional Pin List (Cont'd)**

| PBGA PIN | CABGA PIN | SIGNAL | DESCRIPTION | RESET STATE | STANDBY STATE | OUTPUT DRIVE |
|---|---|---|---|---|---|---|
| R11 | P12 | VDDA | Analog Power for PLL | | | |
| N12 | M10 | | | | | |
| P12 | R13 | VSSA | Analog Ground for PLL | | | |
| T11 | N11 | | | | | |
| D3 | E4 | nPOR | Power On Reset | Input | Input | |
| H6 | D1 | nURESET | User Reset; should be pulled HIGH for normal or JTAG operation. | Input (Schmitt) | Input | |
| D4 | E2 | WAKEUP | Wake Up | Input (Schmitt) | Input | |
| E4 | F2 | nPWRFL | Power Fail Signal | Input (Schmitt) | Input | |
| C2 | D2 | nEXTPWR | External Power | Input (Schmitt) | Input | |
| R13 | R14 | XTALIN | 14.7456 MHz Crystal Oscillator pins. An external clock source can be connected to XTALIN leaving XTALOUT open. | Input | Input | |
| T13 | R15 | XTALOUT | | LOW | LOW | |
| P16 | N14 | XTAL32IN | 32.768 kHz Real Time Clock Crystal Oscillator pins. An external clock source can be connected to XTAL32IN leaving XTAL32OUT open. | Input | Input | |
| P15 | M13 | XTAL32OUT | | Output | Output | |
| P14 | M12 | CLKEN | External Oscillator Clock Enable Output | LOW | LOW | 8 mA |
| J6 | J5 | PGMCLK | Programmable Clock (14.7456 MHz MAX.) | LOW | LOW | 8 mA |
| K11 | P14 | nCS0 | Asynchronous Memory Chip Select 0 | HIGH | HIGH | 12 mA |
| K10 | P16 | nCS1 | Asynchronous Memory Chip Select 1 | HIGH | HIGH | 12 mA |
| P13 | N15 | nCS2 | Asynchronous Memory Chip Select 2 | HIGH | HIGH | 12 mA |
| M12 | N16 | nCS3/ nMMSPICS | • Asynchronous Memory Chip Select 3<br>• MultiMediaCard SPI Mode Chip Select | HIGH: nCS3 | HIGH | 12 mA |

**Table 1. Functional Pin List (Cont'd)**

| PBGA PIN | CABGA PIN | SIGNAL | DESCRIPTION | RESET STATE | STANDBY STATE | OUTPUT DRIVE |
|---|---|---|---|---|---|---|
| M13 | L15 | A2/SA0 | • Asynchronous Address Bus<br>• Synchronous Address Bus | LOW | LOW | 12 mA |
| K16 | K12 | A3/SA1 | | LOW | LOW | 12 mA |
| K15 | K13 | A4/SA2 | | LOW | LOW | 12 mA |
| K14 | K16 | A5/SA3 | | LOW | LOW | 12 mA |
| J8 | J13 | A6/SA4 | | LOW | LOW | 12 mA |
| J16 | J11 | A7/SA5 | | LOW | LOW | 12 mA |
| J14 | J16 | A8/SA6 | | LOW | LOW | 12 mA |
| J9 | H15 | A9/SA7 | | LOW | LOW | 12 mA |
| H16 | H10 | A10/SA8 | | LOW | LOW | 12 mA |
| H14 | H12 | A11/SA9 | | LOW | LOW | 12 mA |
| G16 | G15 | A12/SA10 | | LOW | LOW | 12 mA |
| G14 | G10 | A13/SA11 | | LOW | LOW | 12 mA |
| G13 | G11 | A14/SA12 | | LOW | LOW | 12 mA |
| F16 | F16 | A15/SA13 | | LOW | LOW | 12 mA |
| F14 | E16 | A16/SB0 | • Asynchronous Address Bus<br>• Synchronous Device Bank Address 0 | LOW | LOW | 12 mA |
| E16 | F13 | A17/SB1 | • Asynchronous Address Bus<br>• Synchronous Device Bank Address 1 | LOW | LOW | 12 mA |
| E13 | E14 | A18 | Asynchronous Address Bus | LOW | LOW | 12 mA |
| F11 | D15 | A19 | | | | |
| D15 | C16 | A20 | | | | |
| C16 | C15 | A21 | | | | |
| B16 | C14 | A22 | | | | |
| A15 | B15 | A23 | | | | |
| A13 | E11 | A24 | | | | |
| G8 | D8 | A25/SCIO | • Asynchronous Memory Address Bus<br>• Smart Card Interface I/O (Data) | LOW: A25 | LOW | 12 mA |
| F8 | B7 | A26/SCCLK | • Asynchronous Memory Address Bus<br>• Smart Card Interface Clock | LOW: A26 | LOW | 12 mA |
| A8 | A7 | A27/SCRST | • Asynchronous Memory Address Bus<br>• Smart Card Interface Reset | LOW: A27 | LOW | 12 mA |
| D8 | C8 | nOE | Asynchronous Memory Output Enable | HIGH | HIGH | 12 mA |
| C8 | F8 | nWE0 | Asynchronous Memory Write Byte Enable 0 | HIGH | HIGH | 12 mA |
| D10 | D9 | nWE3 | Asynchronous Memory Write Byte Enable 3 | HIGH | HIGH | 8 mA |
| B10 | E9 | CS6/SCKE1_2 | • Asynchronous Memory Chip Select 6<br>• Synchronous Memory Clock Enable 1 OR 2 | LOW: CS6 | LOW | 12 mA |
| C10 | A10 | CS7/SCKE0 | • Asynchronous Memory Chip Select 7<br>• Synchronous Memory Clock Enable 0 | LOW: CS7 | LOW | 12 mA |
| G9 | A11 | SCKE3 | Synchronous Memory Clock Enable 3 | LOW | LOW | 12 mA |
| A10 | B10 | SCLK | Synchronous Memory Clock | LOW | LOW | 20 mA (sink)<br>12 mA (source) |
| C14 | C13 | nSCS0 | Synchronous Memory Chip Select 0 | HIGH | HIGH | 12 mA |
| D13 | A15 | nSCS1 | Synchronous Memory Chip Select 1 | HIGH | HIGH | 12 mA |
| E11 | D11 | nSCS2 | Synchronous Memory Chip Select 2 | HIGH | HIGH | 12 mA |
| A12 | E10 | nSCS3 | Synchronous Memory Chip Select 3 | HIGH | HIGH | 12 mA |
| C12 | A13 | nSWE | Synchronous Memory Write Enable | HIGH | HIGH | 12 mA |
| C11 | B11 | nCAS | Synchronous Memory Column Address Strobe Signal | HIGH | HIGH | 12 mA |

**Table 1. Functional Pin List (Cont'd)**

| PBGA PIN | CABGA PIN | SIGNAL | DESCRIPTION | RESET STATE | STANDBY STATE | OUTPUT DRIVE |
|---|---|---|---|---|---|---|
| T2 | R2 | PC6/LCDHRLP | • GPIO Port C<br>• LCD Latch Pulse | LOW: PC6 | No Change | 12 mA |
| R2 | N5 | PC7/LCDSPL | • GPIO Port C<br>• LCD Start Pulse Left | LOW: PC7 | No Change | 12 mA |
| M11 | M9 | PD0/LCDVD8 | • GPIO Port D<br>• LCD Video Data Bus | LOW: PD0 | LOW if Dual-Panel LCD is Enabled; otherwise, No Change | 12 mA |
| L11 | K10 | PD1/LCDVD9 | | LOW: PD1 | | |
| K8 | P10 | PD2/LCDVD10 | | LOW: PD2 | | |
| N11 | T11 | PD3/LCDVD11 | | LOW: PD3 | | |
| R9 | T12 | PD4/LCDVD12 | | LOW: PD4 | | |
| T9 | R11 | PD5/LCDVD13 | | LOW: PD5 | | |
| P10 | R12 | PD6/LCDVD14 | | LOW: PD6 | | |
| R10 | T13 | PD7/LCDVD15 | | LOW: PD7 | | |
| L10 | T9 | PE0/LCDVD4 | • GPIO Port E<br>• LCD Video Data Bus | Input: PE0 | LOW if 8-bit LCD is Enabled, otherwise No Change | 12 mA |
| N10 | K9 | PE1/LCDVD5 | | Input: PE1 | | |
| M9 | T10 | PE2/LCDVD6 | | Input: PE2 | | |
| M10 | R10 | PE3/LCDVD7 | | Input: PE3 | | |
| A6 | A5 | PF0/INT0 | • GPIO Port F<br>• External FIQ Interrupt. Interrupts can be level or edge triggered and are internally debounced. | Input: PF0 (Schmitt) | No Change | 8 mA |
| B6 | B4 | PF1/INT1 | • GPIO Port F<br>• External IRQ Interrupts. Interrupts can be level or edge triggered and are internally debounced. | Input: PF1 (Schmitt) | No Change | 8 mA |
| C6 | E7 | PF2/INT2 | | Input: PF2 (Schmitt) | No Change | 8 mA |
| H8 | B3 | PF3/INT3 | • GPIO Port F<br>• External IRQ Interrupt. Interrupts can be level or edge triggered and are internally debounced. | Input: PF3 (Schmitt) | No Change | 8 mA |
| B5 | C5 | PF4/INT4/ SCVCCEN | • GPIO Port F<br>• External IRQ Interrupt. Interrupts can be level or edge triggered and are internally debounced.<br>• Smart Card Supply Voltage Enable | Input: PF4 (Schmitt) | LOW if SCI is Enabled; otherwise, No Change | 8 mA |
| D6 | D6 | PF5/INT5/ SCDETECT | • GPIO Port F<br>• External IRQ Interrupt. Interrupts can be level or edge triggered and are internally debounced.<br>• Smart Card Detection | Input: PF5 (Schmitt) | No Change | 8 mA |
| E6 | A4 | PF6/INT6/ PCRDY1 | • GPIO Port F<br>• External IRQ Interrupt. Interrupts can be level or edge triggered and are internally debounced.<br>• Ready for Card 1 for PC Card (PCMCIA or CompactFlash) in single or dual card mode | Input: PF6 (Schmitt) | No Change | 8 mA |
| C5 | A3 | PF7/INT7/ PCRDY2 | • GPIO Port F<br>• External IRQ Interrupt. Interrupts can be level or edge triggered and are internally debounced.<br>• Ready for Card 2 for PC Card (PCMCIA or CompactFlash) in single or dual card mode | Input: PF7 (Schmitt) | No Change | 8 mA |
| R3 | M6 | PG0/nPCOE | • GPIO Port G<br>• Output Enable for PC Card (PCMCIA or CompactFlash) in single or dual card mode | LOW: PG0 | No Change | 8 mA |
| T3 | T1 | PG1/nPCWE | • GPIO Port G<br>• Write Enable for PC Card (PCMCIA or CompactFlash) in single or dual card mode | LOW: PG1 | No Change | 8 mA |

**Table 1. Functional Pin List (Cont'd)**

| PBGA PIN | CABGA PIN | SIGNAL | DESCRIPTION | RESET STATE | STANDBY STATE | OUTPUT DRIVE |
|---|---|---|---|---|---|---|
| L6 | P4 | PG2/nPCIOR | • GPIO Port G<br>• I/O Read Strobe for PC Card (PCMCIA or CompactFlash) in single or dual card mode | LOW: PG2 | No Change | 8 mA |
| M6 | R3 | PG3/nPCIOW | • GPIO Port G<br>• I/O Write Strobe for PC Card (PCMCIA or CompactFlash) in single or dual card mode | LOW: PG3 | No Change | 8 mA |
| N6 | T2 | PG4/nPCREG | • GPIO Port G<br>• Register Memory Access for PC Card (PCMCIA or CompactFlash) in single or dual card mode | LOW: PG4 | No Change | 8 mA |
| M7 | P5 | PG5/nPCCE1 | • GPIO Port G<br>• Card Enable 1 for PC Card (PCMCIA or CompactFlash) in single or dual card mode. This signal and nPCCE2 are used by the PC Card for decoding low and high byte accesses. | LOW: PG5 | No Change | 8 mA |
| M8 | R4 | PG6/nPCCE2 | • GPIO Port G<br>• Card Enable 2 for PC Card (PCMCIA or CompactFlash) in single or dual card mode. This signal and nPCCE1 are used by the PC Card for decoding low and high byte accesses. | LOW: PG6 | No Change | 8 mA |
| N4 | T3 | PG7/PCDIR | • GPIO Port G<br>• Direction for PC Card (PCMCIA or CompactFlash) in single or dual card mode | LOW: PG7 | No Change | 8 mA |
| P4 | P6 | PH0/ PCRESET1 | • GPIO Port H<br>• Reset Card 1 for PC Card (PCMCIA or CompactFlash) in single or dual card mode | Input: PH0 | No Change | 8 mA |
| R4 | T4 | PH1/CFA8/ PCRESET2 | • GPIO Port H<br>• Address Bit 8 for PC Card (CompactFlash) in single card mode<br>• Reset Card 2 for PC Card (PCMCIA or CompactFlash) in dual card mode | Input: PH1 | No Change | 8 mA |
| T4 | M7 | PH2/ nPCSLOTE1 | • GPIO Port H<br>• Enable Card 1 for PC Card (PCMCIA or CompactFlash) in single or dual card mode. This signal is used for gating other control signals to the appropriate PC Card. | Input: PH2 | No Change | 8 mA |
| N7 | T5 | PH3/CFA9/ PCMCIAA25/ nPCSLOTE2 | • GPIO Port H<br>• Address Bit 9 for PC Card (CompactFlash) in single card mode<br>• Address Bit 25 for PC Card (PCMCIA) in single card mode<br>• Enable Card 2 for PC Card (PCMCIA or CompactFlash) in dual card mode. This signal is used for gating other control signals to the appropriate PC Card. | Input: PH3 | No Change | 8 mA |
| P8 | R6 | PH4/ nPCWAIT1 | • GPIO Port H<br>• WAIT Signal for Card 1 for PC Card (PCMCIA or CompactFlash) in single or dual card mode | Input: PH4 | No Change | 8 mA |
| P5 | R7 | PH5/CFA10/ PCMCIAA24/ nPCWAIT2 | • GPIO Port H<br>• Address Bit 10 for PC Card (CompactFlash) in single card mode<br>• Address Bit 24 for PC Card (PCMCIA) in single card mode<br>• WAIT Signal for Card 2 for PC Card (PCMCIA or CompactFlash) in dual card mode | Input: PH5 | No Change | 8 mA |

## Table 3. LCD Data Multiplexing

| PBGA PIN | CABGA PIN | LCD DATA SIGNAL | STN | | | | | | TFT | AD-TFT/ HR-TFT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MONO 4-BIT | | MONO 8-BIT | | COLOR | | | |
| | | | SINGLE PANEL | DUAL PANEL | SINGLE PANEL | DUAL PANEL | SINGLE PANEL | DUAL PANEL | | |
| K1 | K2 | LCDVD17 | | | | | | | | LOW |
| J5 | K1 | LCDVD16 | | | | | | | | LOW |
| R10 | T13 | LCDVD15 | | | | MLSTN7 | | CLSTN7 | Intensity | Intensity |
| P10 | R12 | LCDVD14 | | | | MLSTN6 | | CLSTN6 | BLUE4 | BLUE4 |
| T9 | R11 | LCDVD13 | | | | MLSTN5 | | CLSTN5 | BLUE3 | BLUE3 |
| R9 | T12 | LCDVD12 | | | | MLSTN4 | | CLSTN4 | BLUE2 | BLUE2 |
| N11 | T11 | LCDVD11 | | | | MLSTN3 | | CLSTN3 | BLUE1 | BLUE1 |
| K8 | P10 | LCDVD10 | | | | MLSTN2 | | CLSTN2 | BLUE0 | BLUE0 |
| L11 | K10 | LCDVD9 | | | | MLSTN1 | | CLSTN1 | GREEN4 | GREEN4 |
| M11 | M9 | LCDVD8 | | | | MLSTN0 | | CLSTN0 | GREEN3 | GREEN3 |
| M10 | R10 | LCDVD7 | | MLSTN3 | MUSTN7 | MUSTN7 | CUSTN7 | CUSTN7 | GREEN2 | GREEN2 |
| M9 | T10 | LCDVD6 | | MLSTN2 | MUSTN6 | MUSTN6 | CUSTN6 | CUSTN6 | GREEN1 | GREEN1 |
| N10 | K9 | LCDVD5 | | MLSTN1 | MUSTN5 | MUSTN5 | CUSTN5 | CUSTN5 | GREEN0 | GREEN0 |
| L10 | T9 | LCDVD4 | | MLSTN0 | MUSTN4 | MUSTN4 | CUSTN4 | CUSTN4 | RED4 | RED4 |
| N8 | T8 | LCDVD3 | MUSTN3 | MUSTN3 | MUSTN3 | MUSTN3 | CUSTN3 | CUSTN3 | RED3 | RED3 |
| T7 | R8 | LCDVD2 | MUSTN2 | MUSTN2 | MUSTN2 | MUSTN2 | CUSTN2 | CUSTN2 | RED2 | RED2 |
| R7 | P8 | LCDVD1 | MUSTN1 | MUSTN1 | MUSTN1 | MUSTN1 | CUSTN1 | CUSTN1 | RED1 | RED1 |
| P7 | M8 | LCDVD0 | MUSTN0 | MUSTN0 | MUSTN0 | MUSTN0 | CUSTN0 | CUSTN0 | RED0 | RED0 |

**NOTES:**
1. The Intensity bit is identically generated for all three colors.
2. MU = Monochrome Upper
3. CU = Color Upper
4. CL = Color Lower

**Table 4. 256-Ball PBGA Package Numerical Pin List (Cont'd)**

| BGA PIN | SIGNAL | RESET STATE | STANDBY STATE |
|---|---|---|---|
| F11 | A19 | LOW | LOW |
| F12 | D17 | LOW | LOW |
| F13 | VDD | | |
| F14 | A16/SB0 | LOW: SBANK0 | LOW |
| F15 | D16 | LOW | LOW |
| F16 | A15/SA13 | LOW: SA13 | LOW |
| G1 | COL2 | HIGH | HIGH |
| G2 | COL3 | HIGH | HIGH |
| G3 | VSS | | |
| G4 | COL4 | HIGH | HIGH |
| G5 | COL5 | HIGH | HIGH |
| G6 | VSSC | | |
| G7 | VDD | | |
| G8 | A25/SCIO | LOW: A25 | LOW |
| G9 | SCKE3 | LOW | LOW |
| G10 | D28 | LOW | LOW |
| G11 | D14 | LOW | LOW |
| G12 | D15 | LOW | LOW |
| G13 | A14/SA12 | LOW: SA12 | LOW |
| G14 | A13/SA11 | LOW: SA11 | LOW |
| G15 | D13 | LOW | LOW |
| G16 | A12/SA10 | LOW: SA10 | LOW |
| H1 | COL6 | HIGH | HIGH |
| H2 | COL7 | HIGH | HIGH |
| H3 | TBUZ | LOW | LOW |
| H4 | SSPCLK | LOW | LOW |
| H5 | VSSC | | |
| H6 | nURESET | Input | Input |
| H7 | VSS | | |
| H8 | PF3/INT3 | Input: PF3 | No Change |
| H9 | VSS | | |
| H10 | D20 | LOW | LOW |
| H11 | D6 | LOW | LOW |
| H12 | VSSC | | |
| H13 | D12 | LOW | LOW |
| H14 | A11/SA9 | LOW: SA9 | LOW |
| H15 | D11 | LOW | LOW |
| H16 | A10/SA8 | LOW: SA8 | LOW |
| J1 | SSPRX | Input | Input |
| J2 | SSPTX | LOW | LOW |
| J3 | SSPFRM/nSSPFRM | Input: nSSPFRM | Input |
| J4 | VDDC | | |
| J5 | PA0/LCDVD16 | Input: PA0 | No Change |
| J6 | PGMCLK | LOW | LOW |
| J7 | UARTRX2 | Input | Input |

**Table 5. 256-Ball CABGA Package Numerical Pin List**

| CABGA PIN | SIGNAL | RESET STATE | STANDBY STATE |
|---|---|---|---|
| L13 | D1 | LOW | LOW |
| L14 | D2 | LOW | LOW |
| L15 | A2/SA0 | LOW | LOW |
| L16 | D4 | LOW | LOW |
| M1 | PB1/UARTTX3 | Input: PB1 | LOW if UART3 is Enabled, otherwise No Change |
| M2 | PB2/UARTRX3 | Input: PB2 | No Change |
| M3 | PB3/UARTCTS3 | Input: PB3 | No Change |
| M4 | PB7/SMBCLK | Input: PB7 | Input if SMB is Enabled, otherwise No Change |
| M5 | PC3/LCDREV | LOW: PC3 | No Change |
| M6 | PG0/nPCOE | LOW: PG0 | No Change |
| M7 | PH2/nPCSLOTE1 | Input: PH2 | No Change |
| M8 | LCDVD0 | LOW | LOW |
| M9 | PD0/LCDVD8 | LOW: PD0 | LOW if Dual-Panel LCD is Enabled; otherwise, No Change |
| M10 | VDDA | | |
| M11 | VSS | | |
| M12 | CLKEN | LOW | LOW |
| M13 | XTAL32OUT | Output | Output |
| M14 | VSS | | |
| M15 | A0/nWE1 | HIGH: nWE1 | HIGH |
| M16 | A1/nWE2 | HIGH: nWE2 | HIGH |
| N1 | PB5/UARTDSR3 | Input: PB5 | No Change |
| N2 | PB6/SWID/SMBD | Input: PB6 | Input if SMB is Enabled, otherwise No Change |
| N3 | VSSC | | |
| N4 | PC5/LCDCLS | LOW: PC5 | No Change |
| N5 | PC7/LCDSPL | LOW: PC7 | No Change |
| N6 | VDD | | |
| N7 | VSSC | | |
| N8 | VDD | | |
| N9 | LCDDCLK | LOW | LOW |
| N10 | VSSC | | |
| N11 | VSSA | | |
| N12 | VDD | | |
| N13 | VDD | | |
| N14 | XTAL32IN | Input | Input |
| N15 | nCS2 | HIGH | HIGH |
| N16 | nCS3/nMMSPICS | HIGH: nCS3 | HIGH |
| P1 | PC0/UARTTX1 | LOW: PC0 | No Change |
| P2 | PC1/LCDPS | LOW: PC1 | No Change |
| P3 | PC4/LCDSPS | LOW: PC4 | No Change |
| P4 | PG2/nPCIOR | LOW: PG2 | No Change |
| P5 | PG5/nPCCE1 | LOW: PG5 | No Change |
| P6 | PH0/PCRESET1 | Input: PH0 | No Change |

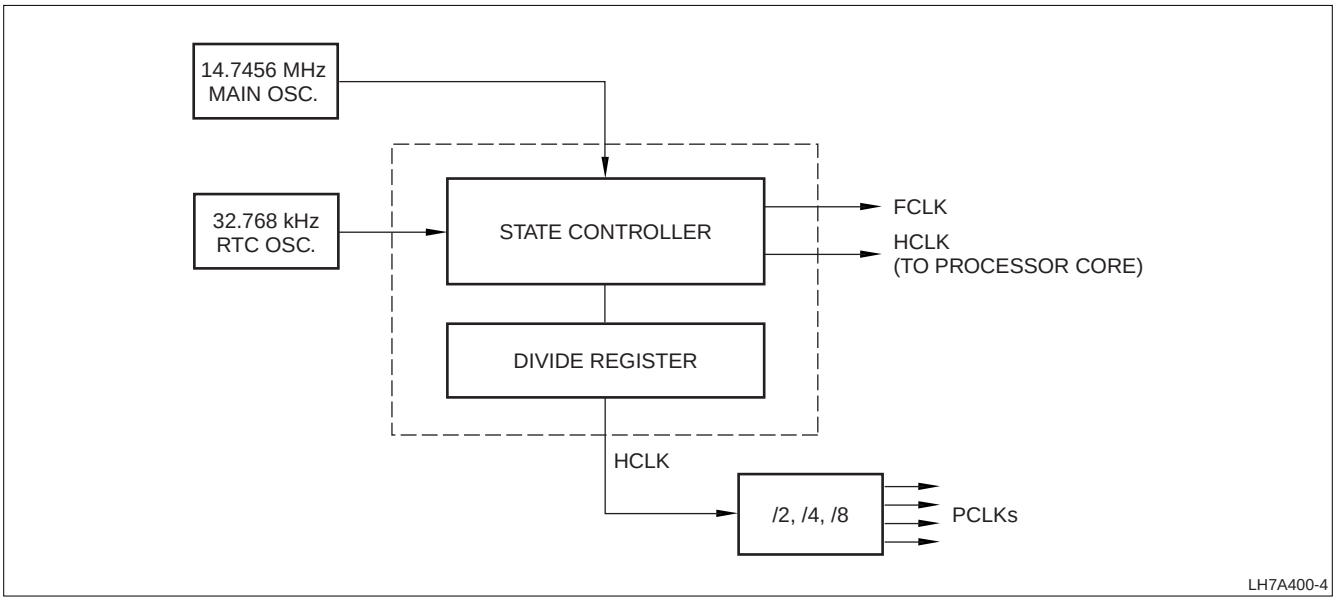



**Figure 3. Clock and State Controller Block Diagram**

## Power Modes

The LH7A400 has three operational states: Run, Halt, and Standby. In Run mode, all clocks are hardware-enabled and the processor is clocked. Halt mode stops the processor clock while waiting for an event such as a key press, but the device continues to function. Finally, Standby equates to the computer being switched 'off', i.e. no display (LCD disabled) and the main oscillator is shut down. The 32.768 kHz oscillator operates in all three modes.

## Reset Modes

There are three external signals that can generate resets to the LH7A400; these are nPOR (power on reset), nPWRFL (power failure) and nURESET (user reset). If any of these are active, a system reset is generated internally. A nPOR reset performs a full system reset. The nPWRFL and nURESET resets will perform a full system reset except for the SDRAM refresh control, SDRAM Global Configuration, SDRAM Device Configuration and the RTC peripheral registers. The SDRAM controller will issue a self-refresh command to external SDRAM before the system enters this reset (the nPWRFL and nURESET resets only, not so for the nPOR reset). This allows the system to maintain its Real Time Clock and SDRAM contents. On coming out of reset, the chip enters Standby mode. Once in Run mode the PWRSR register can be interrogated to determine the nature of the reset, and the trigger source, after which software can then take appropriate actions.

## Data Paths

The data paths in the LH7A400 are:

- The AMBA AHB bus
- The AMBA APB bus
- The External Bus Interface
- The LCD AHB bus
- The DMA busses.

### AMBA AHB BUS

The Advanced Microprocessor Bus Architecture Advanced High-performance Bus (AMBA AHB) bus is a high speed 32-bit-wide data bus. The AMBA AHB is for high-performance, high clock frequency system modules.

Peripherals that have high bandwidth requirements are connected to the LH7A400 core processor using the AHB bus. These include the external and internal memory interfaces, the LCD registers, palette RAM and the bridge to the Advanced Peripheral Bus (APB) interface. The APB Bridge transparently converts the AHB access into the slower speed APB accesses. All of the control registers for the APB peripherals are programmed using the AHB - APB bridge interface. The main AHB data and address lines are configured using a multiplexed bus. This removes the need for tri-state buffers and bus holders, and simplifies bus arbitration.

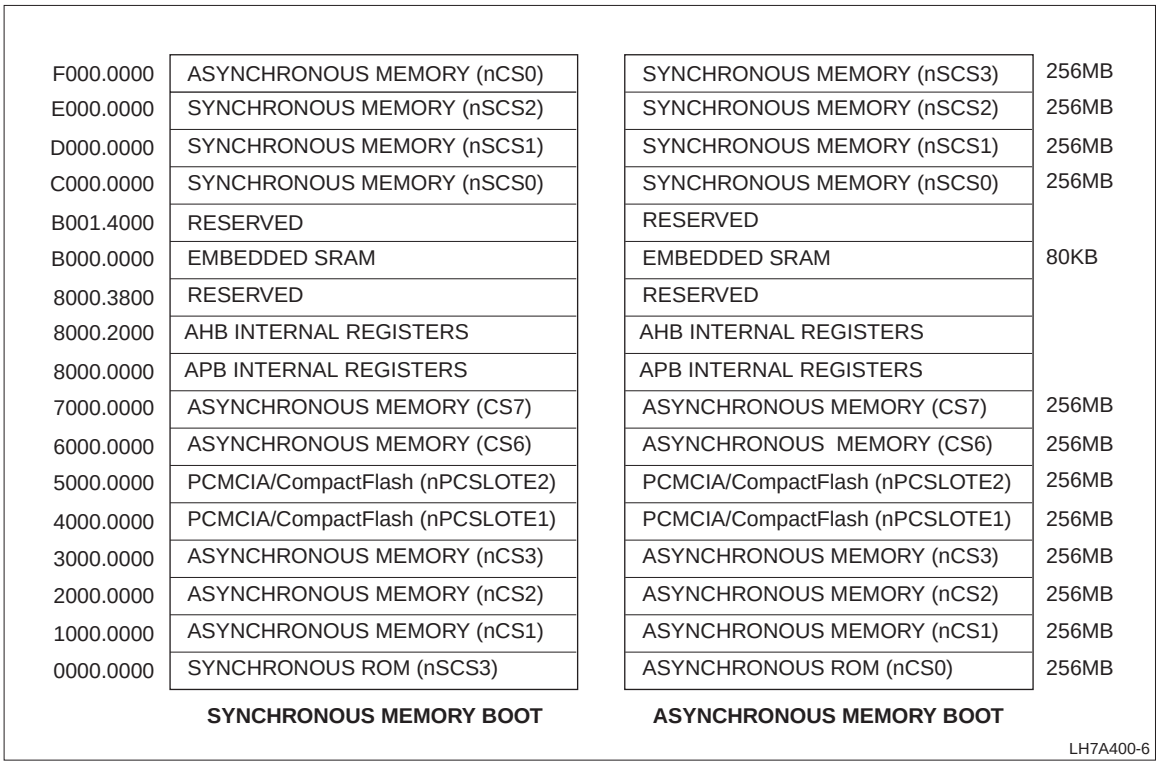



**Figure 4. Memory Mapping for Each Boot Mode**

## External Bus Interface

The external bus interface allows the ARM922T, LCD controller and DMA engine access to an external memory system. The LCD controller has access to an internal frame buffer in embedded SRAM and an extension buffer in Synchronous Memory for large displays. The processor and DMA engine share the main system bus, providing access to all external memory devices and the embedded SRAM frame buffer.

An arbitration unit ensures that control over the External Bus Interface (EBI) is only granted when an existing access has been completed. See Figure 5.

## Embedded SRAM

The amount of Embedded SRAM contained in the LH7A400 is 80KB. This Embedded memory is designed to be used for storing code, data, or LCD frame data and to be contiguous with external SDRAM. The 80KB is large enough to store a QVGA panel (320 × 240) at 8 bits per pixel, equivalent to 70KB of information.

Containing the frame buffer on chip reduces the overall power consumed in any application that uses the LH7A400. Normally, the system has to perform external accesses to acquire this data. The LCD controller is designed to automatically use an overflow frame buffer in SDRAM if a larger screen size is required. This overflow buffer can be located on any 4KB page boundary in SDRAM, allowing software to set the MMU (in the LCD controller) page tables such that the two memory areas appear contiguous. Byte, Half-Word and Word accesses are permissible.

## Asynchronous Memory Controller

The Asynchronous memory controller is incorporated as part of the memory controller to provide an interface between the AMBA AHB system bus and external (off-chip) memory devices.

The Asynchronous Memory Controller provides support for up to eight independently configurable memory banks simultaneously. Each memory bank is capable of supporting:

- SRAM
- ROM
- Flash EPROM
- Burst ROM memory.

Each memory bank may use devices using either 8-, 16-, or 32-bit external memory data paths. The memory controller can be configured to support either little-endian or big-endian operation.

The memory banks can be configured to support:

- Non-burst read and write accesses only to high-speed CMOS static RAM.
- Non-burst write accesses, nonburst read accesses and asynchronous page mode read accesses to fast-boot block flash memory.

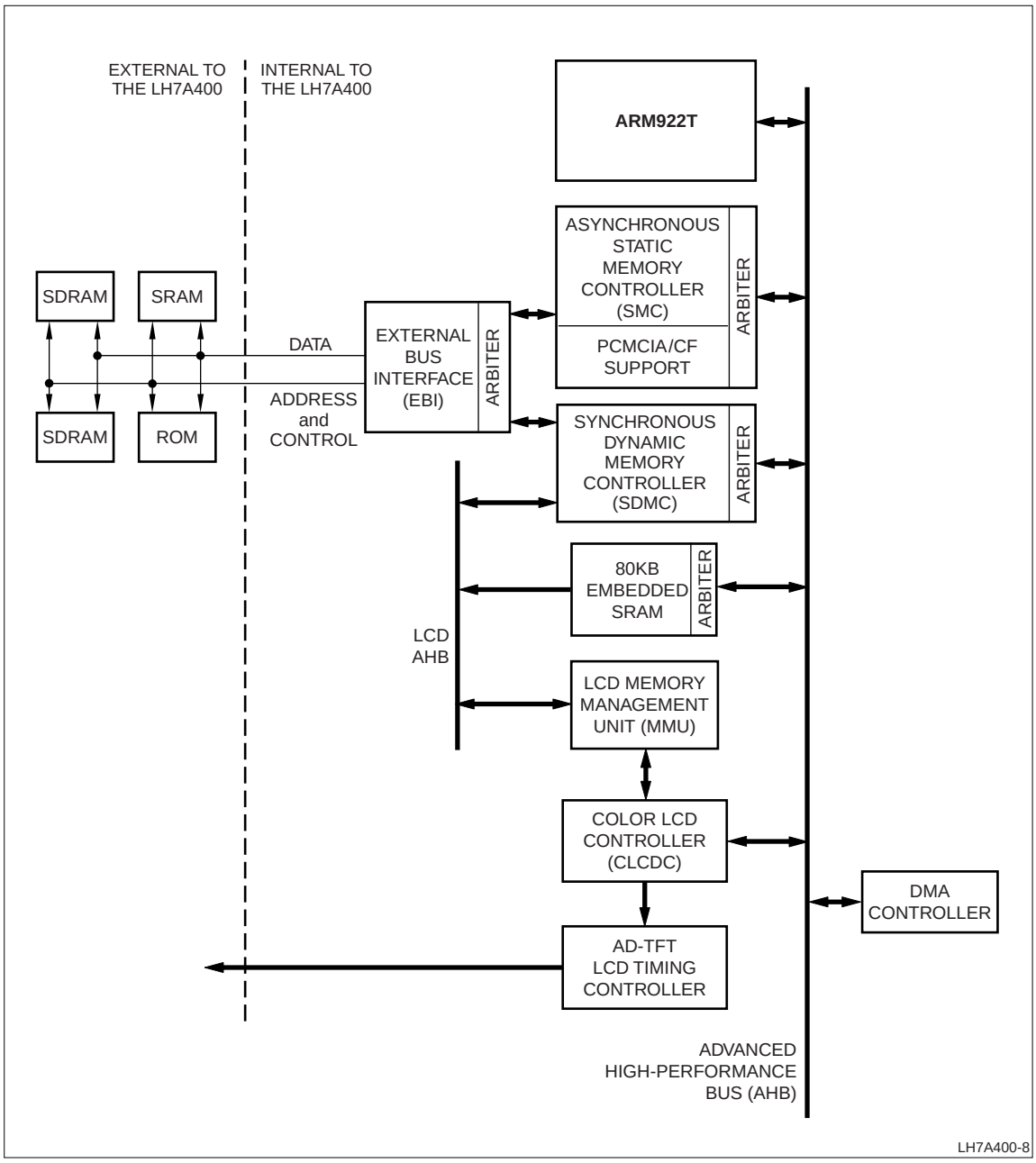



**Figure 5. External Bus Interface Block Diagram**

The Asynchronous Memory Controller has six main functions:

- Memory bank select
- Access sequencing
- Wait states generation
- Byte lane write control
- External bus interface
- CompactFlash or PCMCIA interfacing.

## Synchronous Memory Controller

The Synchronous memory controller provides a high speed memory interface to a wide variety of Synchronous memory devices, including SDRAM, Synchronous Flash and Synchronous ROMs.

The key features of the controller are:

- LCD DMA port for high bandwidth
- Up to four Synchronous Memory banks that can be independently set up
- Special configuration bits for Synchronous ROM operation
- Ability to program Synchronous Flash devices using write and erase commands
- On booting from Synchronous ROM, (and optionally with Synchronous Flash), a configuration sequence is performed before releasing the processor from reset
- Data is transferred between the controller and the SDRAM in quad-word bursts. Longer transfers within the same page are concatenated, forming a seamless burst
- Programmable for 16- or 32-bit data bus size
- Two reset domains are provided to enable SDRAM contents to be preserved over a ‘soft’ reset
- Power saving Synchronous Memory SCKE and external clock modes provided.

## MultiMediaCard (MMC)

The MMC adapter combines all of the requirements and functions of an MMC host. The adapter supports the full MMC bus protocol, defined by the MMC Definition Group’s specification v.2.11. The controller can also implement the SPI interface to the cards.

### INTERFACE DESCRIPTION AND MMC OVERVIEW

The MMC controller uses the three-wire serial data bus (clock, command, and data) to transfer data to and from the MMC card, and to configure and acquire status information from the card’s registers.

MMC bus lines can be divided into three groups:

- Power supply: VDD and VSS
- Data Transfer: MMCCMD, MMCDATA
- Clock: MMCLK.

### MULTIMEDIACARD ADAPTER

The MultiMediaCard Adapter implements MultiMediaCard specific functions, serves as the bus master for the MultiMediacard Bus and implements the standard interface to the MultiMediaCard Cards (card initialization, CRC generation and validation, command/response transactions, etc.).

## Smart Card Interface (SCI)

The SCI (ISO7816) interfaces to an external Smart Card reader. The SCI can autonomously control data transfer to and from the smart card. Transmit and receive data FIFOs are provided to reduce the required interaction between the CPU core and the peripheral.

### SCI FEATURES

- Supports asynchronous T0 and T1 transmission protocols
- Supports clock rate conversion factor F = 372, with bit rate adjustment factors D = 1, 2, or 4 supported
- Eight-character-deep buffered Tx and Rx paths
- Direct interrupts for Tx and Rx FIFO level monitoring
- Interrupt status register
- Hardware-initiated card deactivation sequence on detection of card removal
- Software-initiated card deactivation sequence on transaction complete
- Limited support for synchronous Smart Cards via registered input/output.

### PROGRAMMABLE PARAMETERS

- Smart Card clock frequency
- Communication baud rate
- Protocol convention
- Card activation/deactivation time
- Check for maximum time for first character of Answer to Reset - ATR reception
- Check for maximum duration of ATR character stream
- Check for maximum time of receipt of first character of data stream
- Check for maximum time allowed between characters
- Character guard time
- Block guard time
- Transmit/receive character retry.

## Audio Codec Interface (ACI)

The ACI provides:

- A digital serial interface to an off-chip 8-bit CODEC
- All the necessary clocks and timing pulses to perform serialization or de-serialization of the data stream to or from the CODEC device.

The interface supports full duplex operation and the transmit and receive paths are buffered with internal FIFO memories allowing up to 16 bytes to be stored independently in both transmit and receive modes.

The ACI includes a programmable frequency divider that generates a common transmit and receive bit clock output from the on-chip ACI clock input (ACICLK). Transmit data values are output synchronous with the rising edge of the bit clock output. Receive data values are sampled on the falling edge of the bit clock output. The start of a data frame is indicated by a synchronization output signal that is synchronous with the bit clock.

## Synchronous Serial Port (SSP)

The LH7A400 SSP is a master-only interface for synchronous serial communication with device peripheral devices that has either Motorola SPI, National Semiconductor MICROWIRE or Texas Instruments Synchronous Serial Interfaces.

The LH7A400 SSP performs serial-to-parallel conversion on data received from a peripheral device. The transmit and receive paths are buffered with internal FIFO memories allowing up to eight 16-bit values to be stored independently in both transmit and receive modes. Serial data is transmitted on SSPTXD and received on SSPRXD.

The LH7A400 SSP includes a programmable bit rate clock divider and prescaler to generate the serial output clock SCLK from the input clock SSPCLK. Bit rates are supported to 2 MHz and beyond, subject to choice of frequency for SSPCLK; the maximum bit rate will usually be determined by peripheral devices.

## UART/IrDA

The LH7A400 contains three UARTs, UART1, UART2, and UART3.

The UART performs:

- Serial-to-Parallel conversion on data received from the peripheral device
- Parallel-to-Serial conversion on data transmitted to the peripheral device.

The transmit and receive paths are buffered with internal FIFO memories allowing up to 16 bytes to be stored independently in both transmit and receive modes.

The UART can generate:

- Four individually maskable interrupts from the receive, transmit and modem status logic blocks
- A single combined interrupt so that the output is asserted if any of the individual interrupts are asserted and unmasked.

If a framing, parity or break error occurs during reception, the appropriate error bit is set, and is stored in the FIFO. If an overrun condition occurs, the overrun register bit is set immediately and the FIFO data is prevented from being overwritten. UART1 also supports IrDA 1.0 (15.2 kbit/s).

The modem status input signals Clear to Send (CTS), Data Carrier Detect (DCD) and Data Set Ready (DSR) are supported on UART2 and UART3.

## Timers

Two identical timers are integrated in the LH7A400. Each of these timers has an associated 16-bit read/write data register and a control register. Each timer is loaded with the value written to the data register immediately, this value will then be decremented on the next active clock edge to arrive after the write. When the timer underflows, it will immediately assert its appropriate interrupt. The timers can be read at any time. The clock source and mode is selectable by writing to various bits in the system control register. Clock sources are 508 kHz and 2 kHz.

Timer 3 (TC3) has the same basic operation, but is clocked from a single 7.3728 MHz source. It has the same register arrangement as Timer 1 and Timer 2, providing a load, value, control and clear register. Once the timer has been enabled and is written to, unlike the Timer 1 and Timer 2, will decrement the timer on the next rising edge of the 7.3728 MHz clock after the data register has been updated. All the timers can operate in two modes, free running mode or pre-scale mode.

### FREE-RUNNING MODE

In free-running mode, the timer will wrap around to 0xFFFF when it underflows and continue counting down.

### PRE-SCALE MODE

In pre-scale (periodic) mode, the value written to each timer is automatically re-loaded when the timer underflows. This mode can be used to produce a programmable frequency to drive the buzzer or generate a periodic interrupt.

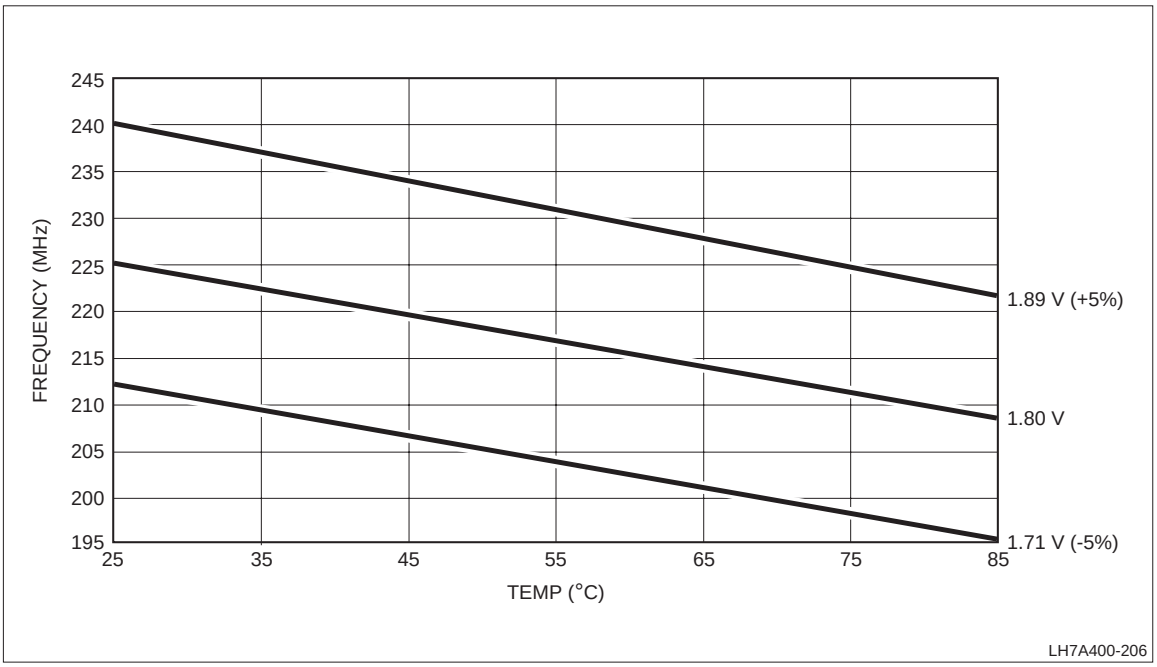



**Figure 6. Temperature/Voltage/Speed Chart**

## AC Specifications

All signals described in Table 10 relate to transitions after a reference clock signal. The illustration in Figure 7 represents all cases of these sets of measurement parameters.

The reference clock signals in this design are:

- HCLK, internal System Bus clock ('C' in timing data)
- PCLK, Peripheral Bus clock
- SSPCLK, Synchronous Serial Port clock
- UARTCLK, UART Interface clock
- LCDDCLK, LCD Data clock from the LCD Controller
- ACBITCLK, AC97 clock
- SCLK, Synchronous Memory clock.

All signal transitions are measured from the 50% point of the clock to the 50% point of the signal.

For outputs from the LH7A400, tOVXXX (e.g. tOVA) represents the amount of time for the output to become valid from a valid address bus, or rising edge of the peripheral clock. Maximum requirements for tOVXXX are shown in Table 10.

The signal tOHXXX (e.g. tOHA) represents the amount of time the output will be held valid from the valid address bus, or rising edge of the peripheral clock. Minimum requirements for tOHXXX are listed in Table 10.

For Inputs, tISXXX (e.g. tISD) represents the amount of time the input signal must be valid after a valid address bus, or rising edge of the peripheral clock. Maximum requirements for tISXXX are shown in Table 10.

The signal tIHXXX (e.g. tIHD) represents the amount of time the output must be held valid from the valid address bus, or rising edge of the peripheral clock. Minimum requirements are shown in Table 10.

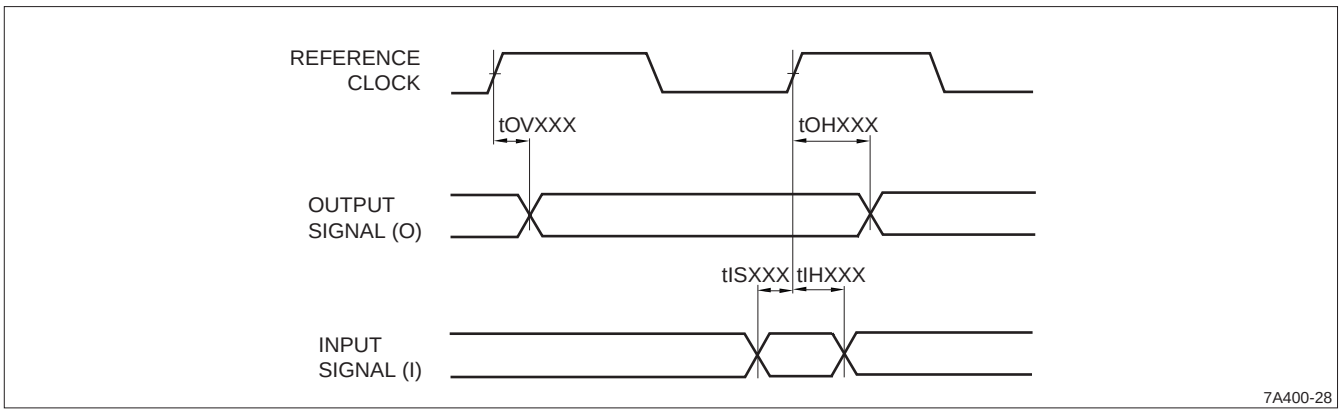



**Figure 7. LH7A400 Signal Timing**

## Table 10. AC Signal Characteristics

| SIGNAL | TYPE | LOAD | SYMBOL | MIN. | MAX. | DESCRIPTION |
|---|---|---|---|---|---|---|
| **ASYNCHRONOUS MEMORY INTERFACE SIGNALS (+ wait states × C)[1]** | | | | | | |
| A[27:0] | Output | 50 pF | tRC | 4C ns | | Read Cycle Time |
| | Output | 50 pF | tWC | 4C ns | | Write Cycle Time |
| | Output | 50 pF | tAW | 2C – 10 ns | | Address Valid to Write Edge |
| | NA | | None | 1C ns | 1C ns | Wait State Width |
| D[31:0] | Output | 50 pF | tDW | 1C – 9 ns | | Data Valid to Write Edge |
| | | | tDH | 1C + 3 ns | | Data Hold after Write Edge |
| | Input | | tAA | 3C – 20 ns | | Address Valid to Data Valid |
| | | | tOH | 0 ns | | Data Output Hold |
| nCS[3:0]/CS[7:6] | Output | 30 pF | tCO | 3C – 20 ns | | Chip Select Valid to Data Valid (Read) |
| | | | tCW | | 1C – 10 ns | Chip Select Valid to Write edge |
| | | | tAS (Write) | 1C ns | | Address Valid to Chip Select Valid (Address setup time) |
| | | | tAS (Read) | 0 | | Address Valid to Chip Select Valid (Address setup time) |
| nWE[3:0] | Output | 30 pF | tWP | 1C – 10 ns | | Write Pulse Width |
| | | | tWHZ | 0 ns | | Write Edge to High Z on SRAM |
| nOE | Output | 30 pF | tOE | | 2C – 20 ns | Output Enable Valid to Data Valid |
| | | | tOHZ | 0 ns | | Output Enable invalid to High Z on SRAM |
| **SYNCHRONOUS MEMORY INTERFACE SIGNALS** | | | | | | |
| SA[13:0] | Output | 50 pF | tOVA | | 7.5 ns | Address Valid |
| | | | tOHA | 1.5 ns | | Address Hold |
| SA[17:16]/SB[1:0] | Output | 50 pF | tOVB | | 7.5 ns | Bank Select Valid |
| D[31:0] | Output | 50 pF | tOVD | 2 ns | 7.5 ns | Data Valid |
| | Input | | tISD | 2.5 ns | | Data Setup |
| | | | tIHD | 1.5 ns | | Data Hold |
| nCAS | Output | 30 pF | tOVCA | 2 ns | 7.5 ns | CAS Valid |
| | | | tOHCA | 2 ns | | CAS Hold |
| nRAS | Output | 30 pF | tOVRA | 2 ns | 7.5 ns | RAS Valid |
| | | | tOHRA | 2 ns | | RAS Hold |
| nSWE | Output | 30 pF | tOVSDW | 2 ns | 7.5 ns | Write Enable Valid |
| | | | tOHSDW | 2 ns | | Write Enable Hold |
| SCKE[1:0] | Output | 30 pF | tOVC | 2 ns | 7.5 ns | Clock Enable Valid |
| DQM[3:0] | Output | 30 pF | tOVDQ | 2 ns | 7.5 ns | Data Mask Valid |
| nSCS[3:0] | Output | 30 pF | tOVSC | 2 ns | 7.5 ns | Synchronous Chip Select Valid |
| | | | tOHSC | 2 ns | | Synchronous Chip Select Hold |
| **PCMCIA INTERFACE SIGNALS (+ wait states × C)[1]** | | | | | | |
| nPCREG | Output | 30 pF | tOVDREG | | 1C | nREG Valid |
| | | | tOHDREG | 4C – 5 ns | | nREG Hold |
| D[31:0] | Output | 50 pF | tOVD | | 1C | Data Valid |
| | | | tOHD | 4C – 5 ns | | Data Hold |
| | Input | | tISD | | 1C - 10 ns | Data Setup Time |
| | | | tIHD | 4C – 5 ns | | Data Hold Time |
| nPCCE1 | Output | 30 pF | tOVCE1 | | 1C | Chip Enable 1 Valid |
| | | | tOHCE1 | 4C – 5 ns | | Chip Enable 1 Hold |
| nPCCE2 | Output | 30 pF | tOVCE2 | | 1C | Chip Enable 2 Valid |
| | | | tOHCE2 | 4C – 5 ns | | Chip Enable 2 Hold |
| nPCOE | Output | 30 pF | tOVOE | | 1C + 1 ns | Output Enable Valid |
| | | | tOHOE | 3C – 5 ns | | Output Enable Hold |
| nPCWE | Output | 30 pF | tOVWE | | 1C + 1 ns | Write Enable Valid |
| | | | tOHWE | 3C – 5 ns | | Write Enable Hold |
| PCDIR | Output | 30 pF | tOVPCD | | 1C | Card Direction Valid |
| | | | tOHPCD | 4C – 5 ns | | Card Direction Hold |

## SMC Waveforms

Figure 8 and Figure 9 show the waveform and timing for an External Asynchronous Memory Write. Note that the deassertion of nWE can precede the deassertion of nCS by a maximum of one HCLK, or at minimum, can coincide (see Table 10). Figure 10 and Figure 11 show the waveform and timing for an External Asynchronous Memory Read.

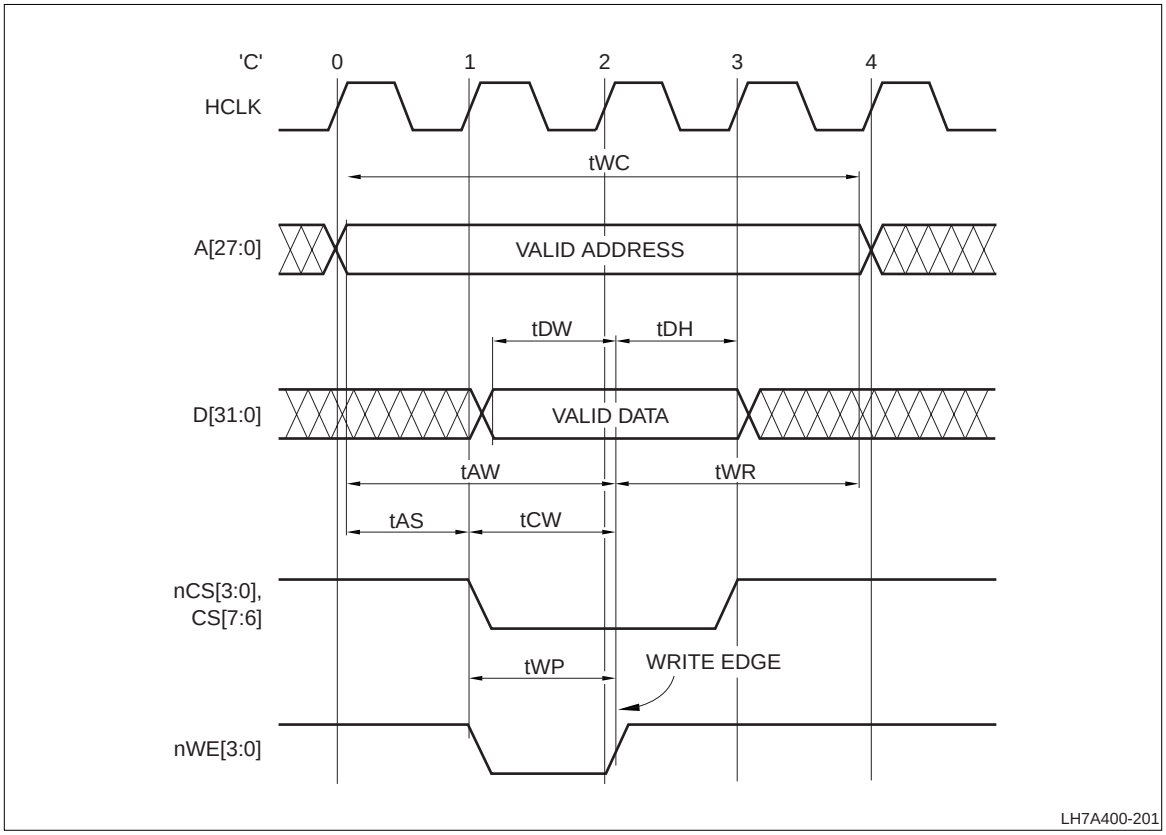



**Figure 8. External Asynchronous Memory Write with 0 Wait States (BCRx:WST1 = 0b000)**

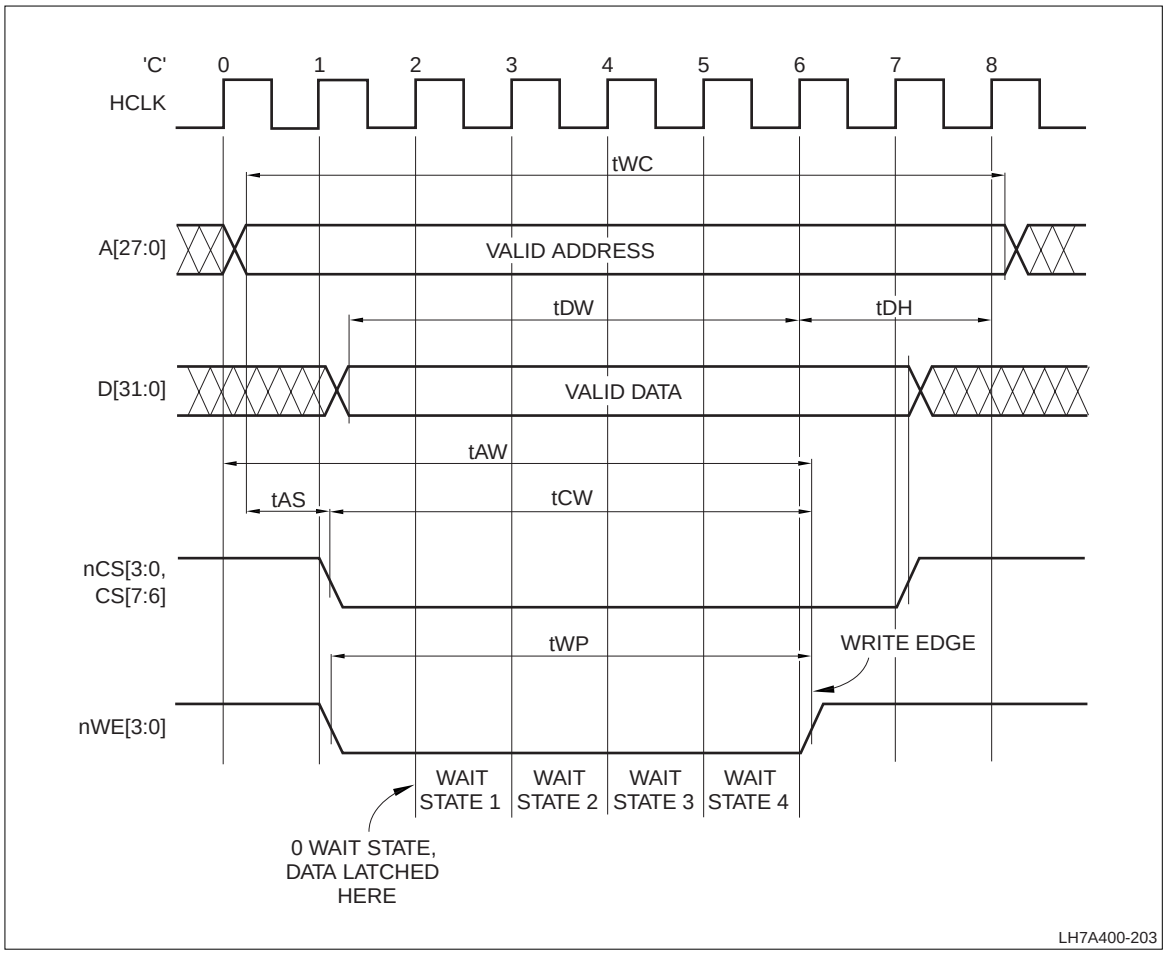



**Figure 9. External Asynchronous Memory Write with 4 Wait States (BCRx:WST1 = 0b100)**

## Clock and State Controller (CSC) Waveforms

Figure 21 shows the behavior of the LH7A400 when coming out of Reset or Power On. Figure 22 shows external reset timing, and Table 11 gives the timing parameters. Figure 23 depicts signal timing following a Reset. On transition from Standby to Run (including a Cold Boot), the Wakeup pin must not be asserted for 2 seconds after assertion of nPOR to allow time for sampling BATOK and nEXTPWR. The delay prevents a false 'battery good' indication caused by alkaline battery recovery that can immediately follow a battery-low switch off. The battery sampling takes place on the rising edge of the 1 Hz clock. This clock is derived from the 32.768 kHz oscillator. The WAKEUP pin can be pulsed, but at least one edge must follow the 2 second delay to be recognized. For more information, see the application note "Implementing Auto-Wakeup on the LH7A4xx Series Devices" at www.sharpsma.com.

Figure 24 shows the recommended components for the SHARP LH7A400 32.768 kHz external oscillator circuit. Figure 25 shows the same for the 14.7456 MHz external oscillator circuit. In both figures, the NAND gate represents the internal logic of the chip.

**Table 11. Reset AC Timing**

| PARAMETER | DESCRIPTION | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| tOSC32 | 32.768 kHz Oscillator Stabilization Time after Power On* | | 550 | ms |
| tPORH | nPOR Hold Time after tOSC32 | 0 | | ms |
| tOSC14 | 14.7456 MHz Oscillator Stabilization Time after Wake UP | | 4 | ms |
| tPLLL | Phase Locked Loop Lockup Time | | 250 | µs |
| tURESET/tPWRFL | nURESET/nPWRFL Pulse Width (once sampled LOW) | 2 | | System Clock Cycles |

**NOTE:** *VDDC = VDDCmin

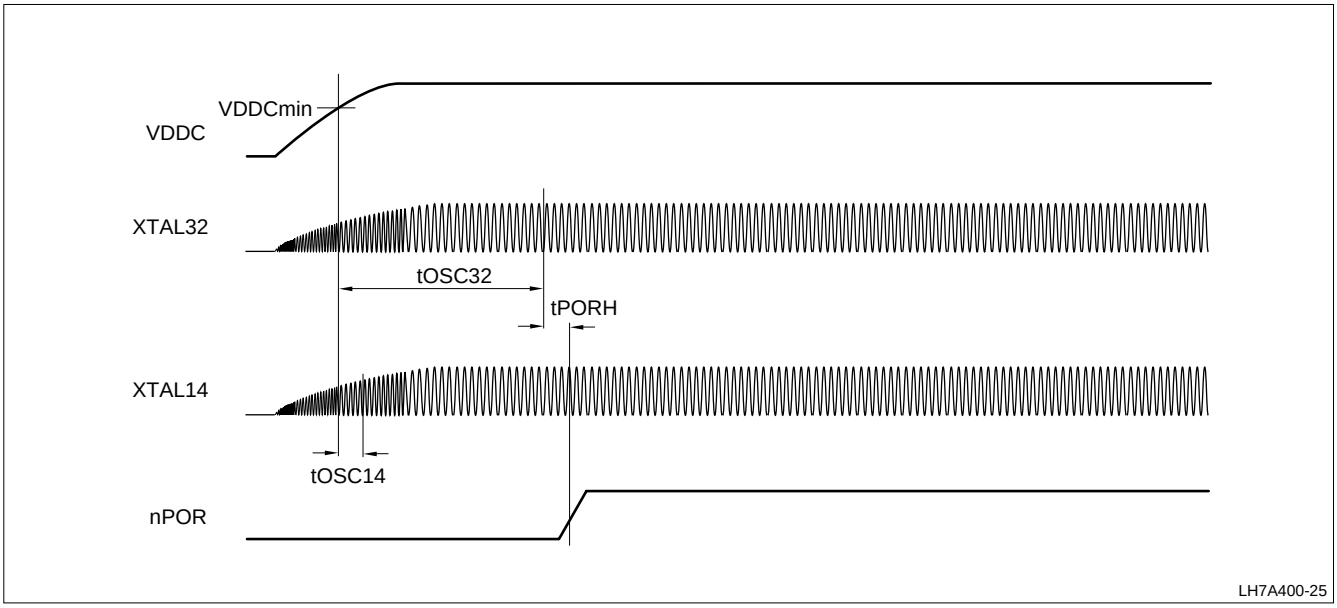



**Figure 21. Oscillator Start-up**

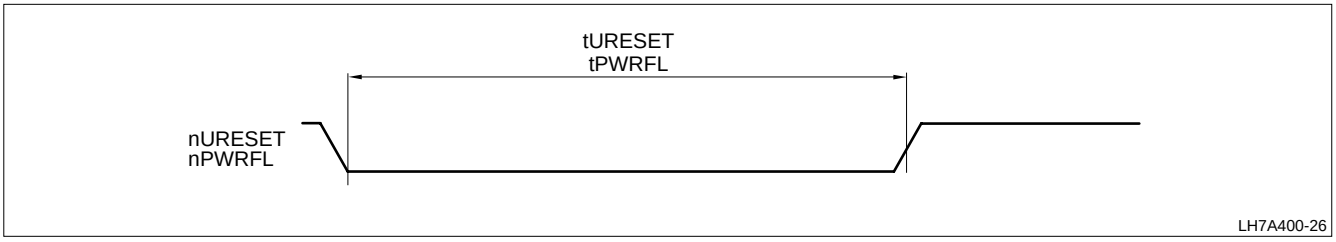
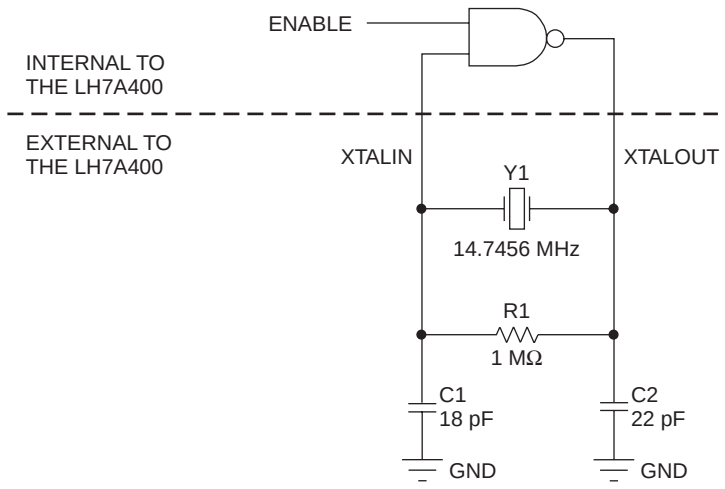



**Figure 22. External Reset**




**NOTES:**
1. Y1 is a parallel-resonant type crystal. (See table)
2. The nominal values for C1 and C2 shown are for a crystal specified at 18 pF load capacitance (CL).
3. The values for C1 and C2 are dependent upon the cystal's specified load capacitance and PCB stray capacitance.
4. R1 must be in the circuit.
5. Ground connections should be short and return to the ground plane which is connected to the processor's core ground pins.
6. Tolerance for R1, C1, C2 is ≤ 5%.

**RECOMMENDED CRYSTAL SPECIFICATIONS**

| PARAMETER | DESCRIPTION |
|---|---|
| 14.7456 MHz Crystal | (AT-Cut) Parallel Mode |
| Tolerance | ±50 ppm |
| Stability | ±100 ppm |
| Aging | ±5 ppm |
| Load Capacitance | 18 pF |
| ESR (MAX.) | 40 Ω |
| Drive Level | 100 µW (MAX.) |
| Recommended Part | MTRON SX2050 or equivalent |

LH7A400-188

**Figure 25. 14.7456 MHz External Oscillator Components and Schematic**

## CONTENT REVISIONS

This document contains the following changes to content, causing it to differ from previous versions.

**Table 12. Record of Revisions**

| DATE | PAGE NO. | PARAGRAPH OR ILLUSTRATION | SUMMARY OF CHANGES |
|---|---|---|---|
| 8-19-2003 | 1 | Features | 256-ball CABGA package added |
| | 3-11 | Table 1 | CABGA Pins added; VDDA1/VDDA2 combined to VDDA; VSSA1/VSSA2 combined to VSSA |
| | 12 | Table 3 | Signal ordering corrected |
| | 12-18 | Table 4 | Table title added to differentiate between PBGA and CABGA packages |
| | 18-24 | Table 5 | CABGA numerical pin list table added |
| | 39 | Figure 7 and Figure 8 | 'CSx' added to figures |
| | 41-42 | Figures 11 and 12 | PCDIR signal corrected in PCMCIA timing diagrams |
| | 44 | Table 10 and Figure 16 | tOSC14 added to both table and figure; XTAL14 added to figure; tPLLL added to table |
| | 45-47 | Figures 19-21 and Printed Circuit Board Layout Practices | Figures and text added |
| | 49 | Figure 23 | Figure added for CABGA package |
| 11-15-03 | 1 | Text | Corrected minor text errors; added separate Commercial and Industrial temperature specification. |
| | 2 | Figure 1 | Updated to show ALI Interface |
| | 34 | 'Recommended Operating Conditions' | Broke out "Commercial" and "Industrial" speed ranges. |
| | 39 | Table 10 | Minor corrections to type. |
| | 39 | Table 10 | Added ACI timing. |
| | 54 | Figure 27 | PBGA package drawing added. |
| 6-21-04 | 11 | Table 1 | Changed names of BOOTWIDTH0 and BOOTWIDTH1 to WIDTH0 and WIDTH1 for consistency with other Sharp SoCs. |
| | 53 | Figure 26; text | Revised text and drawing to indicate that the VSSA pin must be grounded |
| | 50 | Table 11 | Added table. |
| 12-07-04 | ALL | | Rolled revision to Version 1.0 |
| | 1 | Text | Run current corrected to 125 mA and Halt to 25 mA |
| | 34 | Table 7, Figure 6 | Added table and accompanying graph for speed/temperature/voltage |
| | 36 | 'DC Specifications' | Added IRUN, IHALT, and ISTANDBY; corrected IIN. |
| | 37 | Table 8 | Corrected values in Table 8. |
| | 39 | Table 10 | Changed Asynchronous Memory timing to match SRAM datasheet parameter naming conventions. Corrected Synchronous Memory times; added synchronous memory Address Hold time. |
| | 41-44 | Figure 8 - Figure 11 | Changed Asynchronous Memory timing diagrams to match renamed parameters. |
| | 51 | Text and Figure 23 | Clarification made to timing for cold boot power-on sequence. |
| 12-13-04 | 36 | 'DC Specifications' | Added IIN without pullup resistors. |