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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	CANbus, CSI, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	128
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3.3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3378m2gja-gae-ax

Notes for CMOS Devices

1. **Precaution against ESD for semiconductors**
   Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

2. **Handling of unused input pins for CMOS**
   No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

3. **Status before initialization of MOS devices**
   Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

1. Pin Group Information

1.1 Device package information

The V850ES/Fx3 device series comprises several members. An overview with the pin and package information is given in the following table:

Series Member	# Pins	Device package information
μPD70F3370A μPD70F3371	64	FE3
μPD70F3372 μPD70F3373	80	FF3
μPD70F3374 μPD70F3375 μPD70F3376A μPD70F3377A	100	FG3
μPD70F3378 μPD70F3379 μPD70F3380 μPD70F3381 μPD70F3382	144	FJ3
μPD70F3383 μPD70F3384 μPD70F3385	176	FK3

This document describes the specification for the V850ES/FJ3.

1.2 Pin Groups 1x: Pins supplied by EVDD

1B: (SHMT1)
- P04, P30-31, P34; P40, P91, P913-915 (FE3)
- P04, P30-31, P34; P38-39, P40, P91, P913-915 (FF3)
- P04, P30-31, P34; P36-39, P40, P91, P911, P913-915 (FG3)
- P04, P30-31, P34; P36-39, P40, P63-69, P614-615, P80-81, P91, P911, P913-915 (FJ3)
- P04, P30-31, P34; P36-39, P40, P63-69, P614-615, P80-81, P91, P911, P913-915, P156-157 (FK3)

1D: (SHMT3)
- P00-03, P05-P06, P32-33, P35, P41-42, P50-55, P90, P96-99 (FE3)
- P00-03, P05-P06, P32-33, P35, P41-42, P50-55, P90, P96-99 (FF3)
- P00-03, P05-P06, P10-11, P32-33, P35, P41-42, P50-55, P90, P92-910, P912 (FG3)
- P00-03, P05-P06, P10-11, P32-33, P35, P41-42, P50-55, P60-62, P610-613, P90, P92-910, P912 (FJ3)
- P00-03, P05-P06, P10-11, P32-33, P35, P41-42, P50-55, P60-62, P610-613, P90, P92-910, P912, P150-155 (FK3)

1.3 Pin Groups 2x: Pins supplied by EVDD

2A: (CMOS)
- PCM0-1 (FE3)
- PCM0-3, PCS0-1, PCT0-1, PCT4, PCT6 (FF3)

2D: (SHMT3)
- PDL0-7 (FE3)
- PDL0-11 (FF3)

2.6.3 Power supply current (A-grade)

2.6.3.1 µPD70F3378

(a) Absolute values

(Ta = -40 to +85°C, C=4.7uF,
VDD = EVDD = BVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V[Note1])

Mode	Symbol	Condition				TYP.	MAX.	Unit
Operating mode Note2,8	IDD1	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_x=5MHz	28	38	mA
					f_{xx}=32MHz f_x=16MHz	40	53	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	14	21	mA
					f_{xx}=16MHz f_x=16MHz	22	30	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=32MHz f_x=16MHz	36	48	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_x=5MHz	22		mA
					f_{xx}=32MHz f_x=16MHz	32		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	12		mA
					f_{xx}=16MHz f_x=16MHz	19		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=32MHz f_x=16MHz	31		mA
HALT mode Note8	IDD2	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_x=5MHz	18	26	mA
					f_{xx}=32MHz f_x=16MHz	27	39	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	8	12	mA
					f_{xx}=16MHz f_x=16MHz	13	20	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=32MHz f_x=16MHz	21	29	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_x=5MHz	12		mA
					f_{xx}=32MHz f_x=16MHz	18		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	5		mA
					f_{xx}=16MHz f_x=16MHz	9		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=32MHz f_x=16MHz	18		mA

Mode	Symbol	Condition			TYP.	MAX.	Unit
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_x=5MHz	1.7	2.4	mA
				f_{xx}=12MHz f_x=12MHz	2.7	3.9	mA
				f_{xx}=16MHz f_x=16MHz	3.3	4.7	mA
			fxx=8MHz, 8MHz Internal-OSC Note3		1.5	2.3	mA
		All peripherals stopped	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_x=5MHz	1.2		mA
				f_{xx}=12MHz f_x=12MHz	1.4		mA
				f_{xx}=16MHz f_x=16MHz	1.6		mA
			fxx=8MHz, 8MHz Internal-OSC Note3		1.1		mA
IDLE2 mode	IDD4	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7		f_{xx}=5MHz f_x=5MHz	0.4	0.7	mA
				f_{xx}=12MHz f_x=12MHz	0.7	1.0	mA
				f_{xx}=16MHz f_x=16MHz	0.8	1.2	mA
		fxx=8MHz, 8MHz Internal-OSC Note3			0.2	0.5	mA
SUB operating mode Note5	IDD5	Crystal resonator (fxt = 32,768kHz)			80	400	μA
		RC resonator (fxt=20kHz) Note6			80	400	μA
		240 kHz Internal-OSC (SubOSC stopped)			220	1000	μA
SubIDLE mode Note3,5	IDD6	Crystal resonator (fxt = 32,768kHz)			20	190	μA
		RC resonator (fxt=20kHz) Note6			40	220	μA
		240kHz Internal-OSC (SubOSC stopped)			25	180	μA
STOP mode Note3,4	IDD7	POC stop	240kHz Internal-OSC stop		7.5	80	μA
			240kHz Internal-OSC working		15.5	95	μA
		POC work	240kHz Internal-OSC stop		10.5	85	μA
			240kHz Internal-OSC working		18.5	100	μA

2.6.3.3 µPD70F3381, µPD70F3382

(a) Absolute values

(Ta = -40 to +85°C, C=4.7uF,
VDD = EVDD = BVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V[Note1])

Mode	Symbol	Condition				TYP.	MAX.	Unit
Operating mode Note2,8	IDD1	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_x=5MHz	30	41	mA
					f_{xx}=32MHz f_x=16MHz	43	57	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	15	21	mA
					f_{xx}=16MHz f_x=16MHz	24	32	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤48MHz	f_{xx}=48MHz f_x=12MHz	53	68	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_x=5MHz	23		mA
					f_{xx}=32MHz f_x=16MHz	33		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	13		mA
					f_{xx}=16MHz f_x=16MHz	19		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤48MHz	f_{xx}=48MHz f_x=12MHz	46		mA
HALT mode Note8	IDD2	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_x=5MHz	19	28	mA
					f_{xx}=32MHz f_x=16MHz	28	40	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	9	14	mA
					f_{xx}=16MHz f_x=16MHz	15	22	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤48MHz	f_{xx}=48MHz f_x=12MHz	31	42	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_x=5MHz	13		mA
					f_{xx}=32MHz f_x=16MHz	18		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	6		mA
					f_{xx}=16MHz f_x=16MHz	10		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤48MHz	f_{xx}=48MHz f_x=12MHz	25		mA

Mode	Symbol	Condition			TYP.	MAX.	Unit
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_x=5MHz	2.6	3.3	mA
				f_{xx}=12MHz f_x=12MHz	4.1	5.3	mA
				f_{xx}=16MHz f_x=16MHz	4.9	6.5	mA
			fxx=8MHz, 8MHz Internal-OSC Note3		3.0	3.9	mA
		All peripherals stopped	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_x=5MHz	1.4		mA
				f_{xx}=12MHz f_x=12MHz	1.8		mA
				f_{xx}=16MHz f_x=16MHz	2.0		mA
			fxx=8MHz, 8MHz Internal-OSC Note3		1.3		mA
IDLE2 mode	IDD4	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7		f_{xx}=5MHz f_x=5MHz	0.4	0.7	mA
				f_{xx}=12MHz f_x=12MHz	0.7	1.0	mA
				f_{xx}=16MHz f_x=16MHz	0.8	1.2	mA
		fxx=8MHz, 8MHz Internal-OSC Note3			0.2	0.5	mA
SUB operating mode Note5	IDD5	Crystal resonator (fxt = 32,768kHz)			90	400	μA
		RC resonator (fxt=20kHz) Note6			90	400	μA
		240 kHz Internal-OSC (SubOSC stopped)			330	1310	μA
SubIDLE mode Note3,5	IDD6	Crystal resonator (fxt = 32,768kHz)			20	190	μA
		RC resonator (fxt=20kHz) Note6			40	220	μA
		240kHz Internal-OSC (SubOSC stopped)			25	180	μA
STOP mode Note3,4	IDD7	POC stop	240kHz Internal-OSC stop		7.5	100	μA
			240kHz Internal-OSC working		15.5	115	μA
		POC work	240kHz Internal-OSC stop		10.5	105	μA
			240kHz Internal-OSC working		18.5	120	μA

(b) Calculation formulas

(Ta = -40 to +85°C, C=4.7uF,
VDD = EVDD = BVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V[Note1])

Mode	Symbol	Condition			TYP. [Note9]	MAX. [Note9]	Unit
Operating mode [Note2,8]	IDD1	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	1.12·f_{xx}+7.1	1.35·f_{xx}+13.6	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	1.13·f_{xx}+5.5	1.35·f_{xx}+10.6	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤32MHz	0.97·f_{xx}+6.0	1.17·f_{xx}+12.2	mA
		All peripherals stopped	Peripheral: ff_{xx}- PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	0.85·f_{xx}+6.2		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.86·f_{xx}+5.7		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤32MHz	0.82·f_{xx}+6.2		mA
HALT mode [Note8]	IDD2	All peripherals running	Peripheral: ff_{xx}- PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤32MHz	0.75·f_{xx}+3.0	1.04*f_{xx}+6.9	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.72·f_{xx}+3.0	1.00*f_{xx}+5.5	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 16MHz≤f_{xx}≤32MHz	0.56·f_{xx}+4.0	0.69*f_{xx}+8.5	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤32MHz	0.46·f_{xx}+3.6		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.46·f_{xx}+2.6		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 16MHz≤f_{xx}≤32MHz	0.46·f_{xx}+2.8		mA
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running		PLL: OFF 4MHz≤f_{xx}≤16MHz [Note7]	0.211·f_{xx}+1.54	0.295·f_{xx}+ 1.80	mA
		All peripherals stopped			0.054·f_{xx}+1.15		mA
IDLE2 mode	IDD4	PLL: OFF 4MHz ≤f_{xx}≤16MHz [Note7]			0.037·f_{xx}+0.21	0.049·f_{xx}+ 0.43	mA

Notes: 1. VDD, EVDD and BVDD total current. (Ports are stopped).
AVREF0 current, port buffer current (including a current flowing in the on-chip pull-up/pull-down resistor) are not included.

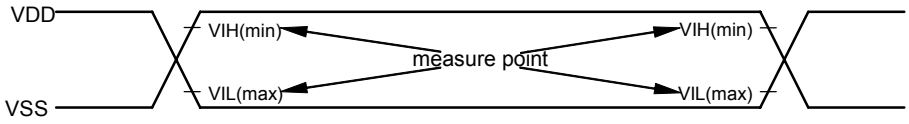
2. The code flash and the data flash are in read mode.
When the device is in programming mode (Self-programming mode or data flash programming mode), the current value (MAX. value) adds by the following value:

- Self-programming mode:
  + In case of PLL OFF: 7-(0.33*fxx+0.1) [mA]
  + In case of PLL ON: 7-(0.18*fxx+3.0) [mA]
- Data flash programming mode:
  + 7-(0.18*fxx/4+3.0) [mA]

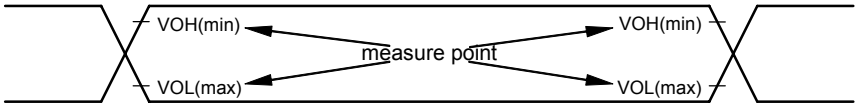
3. Main OSC is stopped.
4. Do not use SubOSC.
5. POC is working. 240kHz Internal-OSC is working. 8MHz Internal-OSC is stopped.
6. RC Oscillation frequency is typ.40kHz. This clock is divided by 2 internally.
7. 8MHz Internal-OSC is stopped
8. When the SSCG is running, the current value adds typ +2.5mA, max +4mA.
9. The formulas are for reference only. Not all possible values for f_{xx} are tested in the outgoing device inspection.

2.7 AC Characteristics

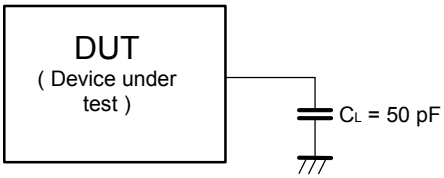
AC test Input measurement points (VDD, AVREF0, EVDD, BVDD)



AC test output measurement points



Load conditions



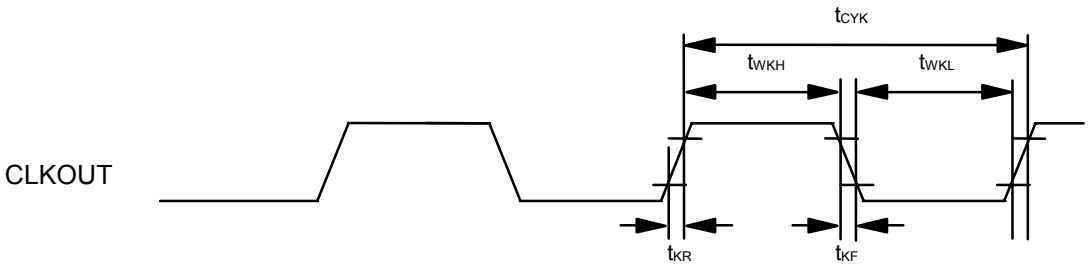
Caution: If the load capacitance exceeds 50pF due to the circuit configuration, reduce the load capacitance of the device to 50pF or less by inserting a buffer or by some other means.

2.7.1 CLKOUT Output Timing

(Ta = -40 to +85°C, VDD = EVDD = BVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output cycle	tCYK	VDD = EVDD = BVDD = 4.0V ~ 5.5V	31.25ns	80μs	
		VDD = EVDD = BVDD = 3.5V ~ 5.5V	50ns		
High level width	tWKH	VDD = EVDD = BVDD = 4.0V ~ 5.5V	tCYK/2-13		ns
		VDD = EVDD = BVDD = 3.5V ~ 5.5V	tCYK/2-15		
Low level width	tWKL	VDD = EVDD = BVDD = 4.0V ~ 5.5V	tCYK/2-13		ns
		VDD = EVDD = BVDD = 3.5V ~ 5.5V	tCYK/2-15		
Rise time	tKR	VDD = EVDD = BVDD = 4.0V ~ 5.5V		13	ns
		VDD = EVDD = BVDD = 3.5V ~ 5.5V		15	
Fall time	tKF	VDD = EVDD = BVDD = 4.0V ~ 5.5V		13	ns
		VDD = EVDD = BVDD = 3.5V ~ 5.5V		15	

CLKOUT output timing



(b) CLKOUT synchronous: In multiplexed bus mode

(Ta = -40 to +85°C, VDD = EVDD = BVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	tDKA	<43>		0	24	ns
Delay time from CLKOUT↑ to address float	tFKA	<44>		0	24	ns
Delay time from CLKOUT↓ to ASTB	tDKST	<45>		-7	18	ns
Delay time fromCLKOUT↑ to _RD, _WRm	tDKRDWR	<46>		-2	18	ns
Data Input setup time (from CLKOUT↑)	tSIDK	<47>		20		ns
Data Input hold time (from CLKOUT↑)	tHKID	<48>		5		ns
Data output delay time (from CLKOUT↑)	tDKOD	<49>			27	ns
_WAIT setup time (to CLKOUT↓)	tSWTK	<50>		30		ns
_WAIT hold time (from CLKOUT↓)	tHKWT	<51>		5		ns
HLDRQ setup time (to CLKOUT↓)	tSHQK	<52>		30		ns
_HLDRQ hold time (from CLKOUT↓)	tHKHQ	<53>		5		ns
Delay time from CLKOUT↑ to _HLDAK	tDKHA	<54>			24	ns
Delay time from CLKOUT↑ to address float	tDKF	<55>			25	ns

Remarks: 1. T=1/fcpu (fcpu: CPU operation clock frequency)

2. n: Number of wait clocks Inserted In the bus cycle.
The sampling timing changes when a programmable wait is Inserted.

3. i: Number of Idle states Inserted after the read cycle (0 or 1).

4. The values In the above specifications are values for when clocks with a 1: 1 duty ratio are Input from X1

5. m=0,1

6. t_{ASW}=Number of address setup wait clocks (0 or 1)
t_{AHW}=Number of address hold wait clocks (0 or 1)

7. When the operation frequency is high, it is not possible to access by no wait bus cycle. Please insert wait clock (data wait (n)) / address setup wait (tASW) / address hold wait (tAHW)).
Example: Set the following in accordance to the CPU operating clock frequency (k=0 to 3).

- In case of Flash ≤ 256KB product
  - 31.25ns≤1/fcpu<40ns: Set an address setup wait (AWC.ASWk bit=1).
- In case of Flash ≥ 384KB product
  - 30ns≤1/fcpu<40ns: Set an address setup wait (AWC.ASWk bit=1).
  - 20.8ns≤1/fcpu<30ns: Set an address setup wait (AWC.ASWk bit=1) and address hold wait (AWC.AHWk bit=1).
  - 20.8ns≤1/fcpu≤25ns: Set a data wait (minimum 1 wait)

2.7.3 RESET, Interrupt, ADTRG Timing

(Ta = -40 to +85°C, VDD = EVDD = BVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
_RESET input low level width	tWRSL	analog filter	250			ns
NMI input high level width	tWNIH	analog filter	250			ns
NMI input low level width	tWNIL	analog filter	250			ns
INTPn[Note1] input high level width	tWITH	analog filter ,n=0-14	250			ns
		digital filter ,n=3	Note2			ns
INTPn [Note1] input low level width	tWITL	analog filter ,n=0-14	250			ns
		digital filter ,n=3	Note2			ns

Notes: 1. ADTRG is same spec (P03/INTP0/ADTRG). $\overline{\text{DRST}}$ is same spec (P05/INTP2/$\overline{\text{DRST}}$)

2. 2Tsamp+20 or 3Tsamp+20 ("Tsamp" is Noise reject sampling clock (NF macro))

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. $\overline{\text{RESET}}$, NMI, INTPn, ADTRG and $\overline{\text{DRST}}$ have analog noise filter. The typical filter time is typ=60ns.

2.7.4 Key Return Timing

(Ta = -40 to +85°C, VDD = EVDD = BVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
KRn input high level width	tWKRH	analog filter ,n=0-7	250			ns
KRn input low level width	tWKRL	analog filter ,n=0-7	250			ns

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. KRn inputs have analog noise filter. The typical filter time is typ=60ns.

2.7.5 Timer Timing

(Ta = -40 to +85°C, VDD = EVDD = BVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V, CL=50pF)

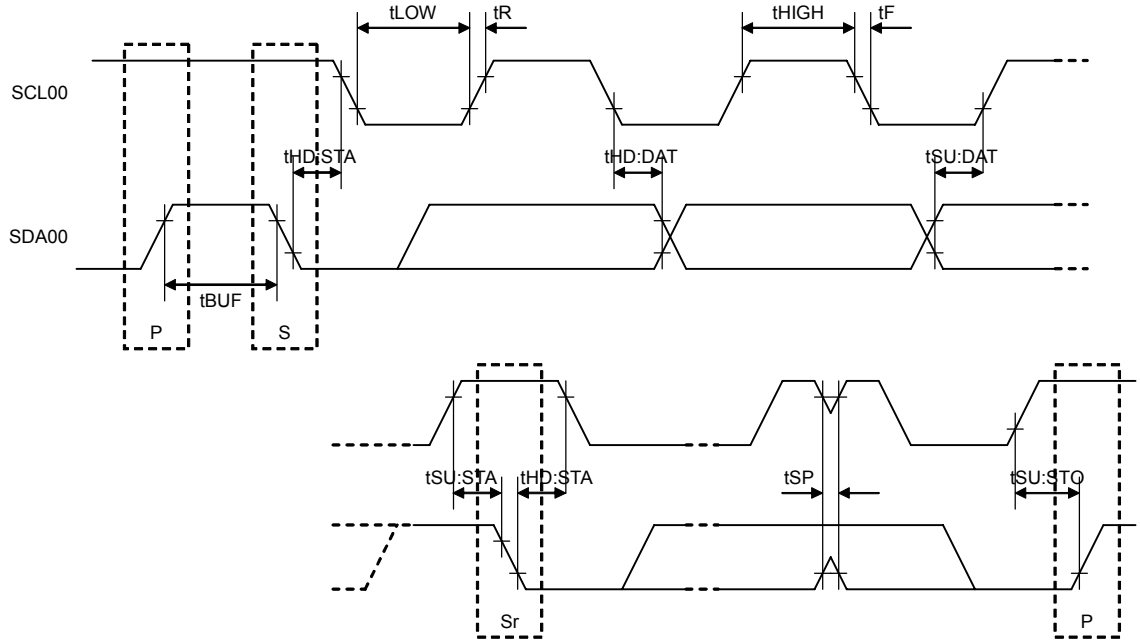
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
TI input high level width	tTIH	TIAA00-01,10-11,20-21,30-31,40-41 [Note1] TIAB00-03,10-13,20-23 [Note1]		250			ns
TI input low level width	tTIL	TIAA00-01,10-11,20-21,30-31,40-41 [Note1] TIAB00-03,10-13,20-23 [Note1]		250			ns
TO output cycle	tTCYK	TIAA00-01,10-11,20-21,30-31, 40-41 [Note1] TIAB00-03,10-13,20-23 [Note1]	4.0V≤VDD≤5.5V			16	MHz
			3.5V≤VDD<4.0V			10	MHz

Notes: 1. Except for the external trigger and external event function.

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. TIAAn and TIABn inputs have analog noise filter. The typical filter time is typ=60ns.

IIC bus interface timing

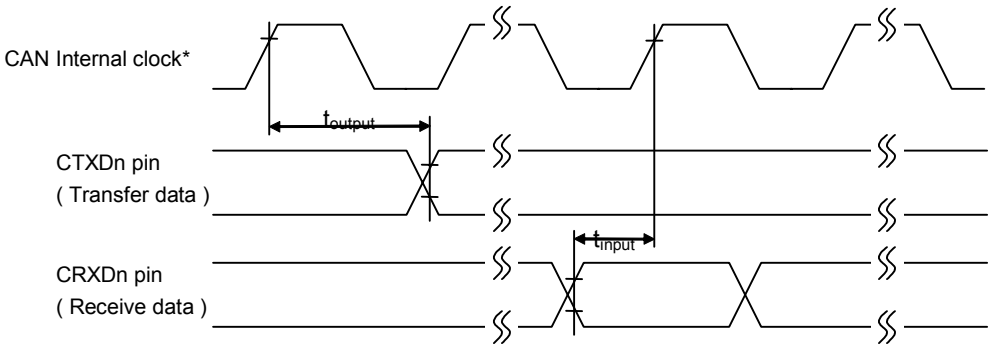


Remark: P: Stop condition
S: Start condition
Sr: Restart condition

2.7.9 CAN Timing

(Ta = -40 to +85°C, VDD = EVDD = BVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					1	Mbps
Internal delay time					100	ns



Internal delay time (tNODE)= Internal Transfer Delay(t_{output}) + Internal Receive Delay(t_{input})

*) CAN Internal clock (f_{CAN}) :CAN baud rate clock

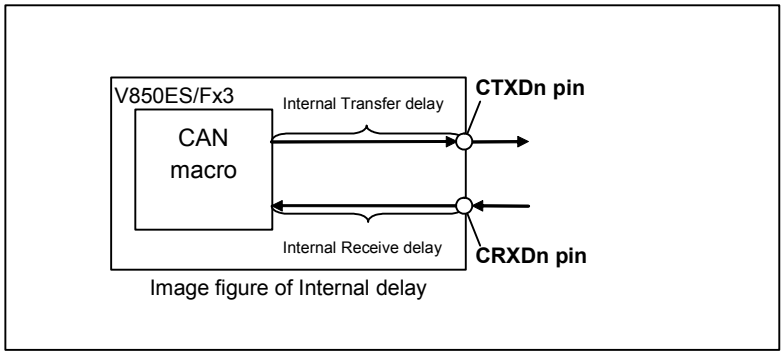


Image figure of Internal delay

3.5 Clock Generator Circuit

3.5.1 Main System Clock Oscillation Circuit Characteristics

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.5.2 Sub System Clock Oscillation Circuit Characteristics

(Ta = -40 to +110°C, C=4.7uF, VDD = EVDD = BVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V)

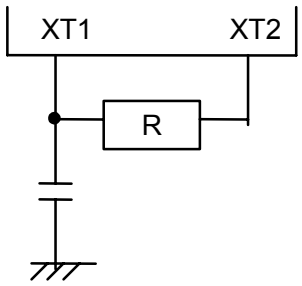
Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC resonator	Refer to Figure 2	Oscillator frequency Note1,4	R=390KΩ ±5% Note3, C=47pF±10% Note3	25	40	55	kHz
		Oscillation stabilization time Note2				100	μs

Notes: 1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristic" for cpu operation clock.

2. Time required to stabilize oscillation after VDD reaches oscillator voltage range min. 3.3V

3. In order to avoid the influence of wiring capacity, shorten wiring as much as possible.

4. RC Oscillation frequency is typ. 40kHz. This clock is divided by 2 internally. In case of RC Oscillator, internal system clock frequency(fxt) is min. 12.5kHz, typ. 20kHz, max. 27.5kHz.



3.5.3 Internal-OSC Characteristics

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.5.4 PLL Characteristics

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.5.5 SSCG Characteristics

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.6 DC Characteristics

3.6.1 Input/Output Level

(Ta = -40 to +110°C, C=4.7uF, VDD = EVDD = BVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V)

Parameter	Sym-bol	Conditions		MIN.	TYP.	MAX.	Unit
High level input voltage	VIH1	Pin Group 1B		0.7·EVDD		EVDD	V
	VIH2	Pin Group 1D		0.8·EVDD		EVDD	V
		Pin Group 3D		0.8·BVDD		BVDD	V
	VIH3	Pin Group 3A		0.7·BVDD		BVDD	V
	VIH4	Pin Group 4		0.7·AVREF0		AVREF0	V
	VIH5	Pin Group 6		0.8·EVDD		EVDD	V
Low level input voltage	VIL1	Pin Group 1B		EVSS		0.3·EVDD	V
	VIL2	Pin Group 1D		EVSS		0.4·EVDD	V
		Pin Group 3D		BVSS		0.4·BVDD	V
	VIL3	Pin Group 3A		BVSS		0.3·BVDD	V
	VIL4	Pin Group 4		AVSS		0.3·AVREF0	V
	VIL5	Pin Group 6		EVSS		0.2·EVDD	V
Input hysteresis	VHYS1	Pin Group 1B	Center point at 0.5 x EVDD Note3		0.267 x EVDD - 0.51V		V
	VHYS2	Pin Group 1D	Center point at 0.6 x EVDD Note3		0.192 x EVDD - 0.31V		V
		Pin Group 3D	Center point at 0.6 x BVDD Note3		0.192 x BVDD - 0.31V		V
	VHYS5	Pin Group 6	Center point at 0.5 x EVDD Note3		0.535 x EVDD - 0.9V		V
High level output voltage Note2	VOH1	Pin Group 1x	IOH=-1.0mA	EVDD-1.0		EVDD	V
			IOH=-100uA	EVDD-0.5		EVDD	V
	VOH2	Pin Group 3x	IOH=-1.0mA	BVDD-1.0		BVDD	
			IOH=-100uA	BVDD-0.5		BVDD	V
	VOH3	Pin Group 4	IOH=-1.0mA	AVREF0-1.0		AVREF0	V
			IOH=-100uA	AVREF0-0.5		AVREF0	V
Low level output voltage Note2	VOL1	Pin Group 1x	IOL=1.0mA	0		0.4	V
		P914, 915	IOL=3.0mA				
	VOL2	Pin Group 3x	IOL=1.0mA	0		0.4	V
	VOL3	Pin Group 4	IOL=1.0mA	0		0.4	V
Software pull-up resistor	R1	VI=0V		10	30	100	kΩ
Software Note1 pull-down resistor	R2	VI=VDD		10	30	100	kΩ

Remark: The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified.

Notes: 1. $\overline{\text{DRST}}$ terminal only. (Control register is OCDM)

2. Total IOH/IOL max is 20mA/-20mA for the power supply lines EVDD and BVDD.
Total IOH/IOL max is 10mA/-10mA for the power supply line AVREF0.
AVREF0 IOH/IOL current is excluding ADC current IAREF0.

3. Typical value. Not tested and guaranteed

3.6.3.2 µPD70F3379, µPD70F3380

(a) Absolute values

(Ta = -40 to +110°C, C=4.7uF,
VDD = EVDD = BVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V[Note1])

Mode	Symbol	Condition				TYP.	MAX.	Unit
Operating mode Note2,8	IDD1	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_x=5MHz	28	39	mA
					f_{xx}=32MHz f_x=16MHz	41	54	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	14	21	mA
					f_{xx}=16MHz f_x=16MHz	23	31	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤48MHz	f_{xx}=48MHz f_x=12MHz	51	66	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_x=5MHz	22		mA
					f_{xx}=32MHz f_x=16MHz	32		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	12		mA
					f_{xx}=16MHz f_x=16MHz	19		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤48MHz	f_{xx}=48MHz f_x=12MHz	44		mA
HALT mode Note8	IDD2	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_x=5MHz	18	26	mA
					f_{xx}=32MHz f_x=16MHz	27	39	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	8	12	mA
					f_{xx}=16MHz f_x=16MHz	13	20	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤48MHz	f_{xx}=48MHz f_x=12MHz	30	40	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_x=5MHz	12		mA
					f_{xx}=32MHz f_x=16MHz	18		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	5		mA
					f_{xx}=16MHz f_x=16MHz	9		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤48MHz	f_{xx}=48MHz f_x=12MHz	24		mA

4. Electrical Specifications of (A2)-Grade

This product has to be used only under the conditions of VDD=EVDD=BVDD. Operation is not ensured at the time of using this product except this condition.

4.1 Absolute Maximum Ratings

Specification is identical to that from (A1)-Grade except

- Operating ambient temperature Ta = -40 to +125°C
- Note2: AVREF0 IOH/IOL current is including ADC max. current IAREF0.

4.2 Capacities

Specification is identical to that from (A)-Grade except Ta=-40 to +125°C.

4.5.2 Sub System Clock Oscillation Circuit Characteristics

Specification is identical to that from (A1)-Grade except Ta=-40 to +125°C.

4.5.3 Internal-OSC Characteristics

Specification is identical to that from (A)-Grade except Ta=-40 to +125°C.

4.5.4 PLL Characteristics

(Ta = -40 to +125°C, C=4.7uF, VDD = EVDD = BVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	fx		4		16	MHz
	f_{PLLI}	Note	3		6	MHz
Output frequency	fxx	≤256KB product	12		24	MHz
		≥384KB product	12		32	
Lock time	tPLL	After VDD reaches voltage range min. 3.3V			800	μs
Output period jitter Note2	tpj	Peak to peak			2.0	ns

Notes: 1. The input of the PLL (f_{PLLI}) can be set to f_X, $f_X/2$, or $f_X/4$. The divider is set through an option byte in the code flash memory.

2. Not tested in production.

4.5.5 SSCG Characteristics

(Ta = -40 to +125°C, C=4.7uF, VDD = EVDD = BVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	fx		4		16	MHz
Output frequency	fxx	≤256KB product	12		24	MHz
		≥384KB product	12		32	
Lock time	t_{SSCG}	After VDD reaches voltage range min. 3.3V			1000	μs

Remark: The SSCG MAX output frequency indicates the case without modulation. If modulation is enabled the average SSCG frequency has to be set lower. The maximum achievable average operating frequency with modulation is as follows:

SSCG input clock divider selector SFC1[6:4]	Percent modulation		Maximum average operating frequency		Unit
	TYP	MAX	≤256KB product	≥384KB product	
000B	± 0.5%	± 2.0%	23.5	31.4	MHz
001B	± 1.0%	± 2.5%	23.4	31.2	
010B	± 2.0%	± 4.0%	23.0	30.7	
011B	± 3.0%	± 6.0%	22.6	30.1	
100B	± 4.0%	± 8.0%	22.1	29.4	
101B	± 5.0%	± 10.0%	21.6	28.8	

Mode	Symbol	Condition			TYP.	MAX.	Unit
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_x=5MHz	2.6	3.9	mA
				f_{xx}=12MHz f_x=12MHz	4.1	5.9	mA
				f_{xx}=16MHz f_x=16MHz	4.9	7.1	mA
			fxx=8MHz, 8MHz Internal-OSC Note3		3.0	4.5	mA
		All peripherals stopped	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_x=5MHz	1.4		mA
				f_{xx}=12MHz f_x=12MHz	1.8		mA
				f_{xx}=16MHz f_x=16MHz	2.0		mA
			fxx=8MHz, 8MHz Internal-OSC Note3		1.3		mA
IDLE2 mode	IDD4	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7		f_{xx}=5MHz f_x=5MHz	0.4	1.1	mA
				f_{xx}=12MHz f_x=12MHz	0.7	1.5	mA
				f_{xx}=16MHz f_x=16MHz	0.8	1.7	mA
		fxx=8MHz, 8MHz Internal-OSC Note3			0.2	1.0	mA
SUB operating mode Note5	IDD5	RC resonator (fxt=20kHz) Note6			90	850	μA
		240 kHz Internal-OSC (SubOSC stopped)			330	1760	μA
SubIDLE mode Note3,5	IDD6	RC resonator (fxt=20kHz) Note6			40	670	μA
		240kHz Internal-OSC (SubOSC stopped)			25	630	μA
STOP mode Note3,4	IDD7	POC stop	240kHz Internal-OSC stop		7.5	550	μA
			240kHz Internal-OSC working		15.5	565	μA
		POC work	240kHz Internal-OSC stop		10.5	555	μA
			240kHz Internal-OSC working		18.5	570	μA

(b) Calculation formulas

(Ta = -40 to +125°C, C=4.7uF,
VDD = EVDD = BVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V[Note1])

Mode	Symbol	Condition			TYP. [Note9]	MAX. [Note3]	Unit
Operating mode Note2,8	IDD1	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	1.06·f_{xx}+7.1	1.27·f_{xx}+13.6	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	1.06·f_{xx}+5.5	1.28·f_{xx}+10.6	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤32MHz	0.94·f_{xx}+6.0	1.13·f_{xx}+12.2	mA
		All peripherals stopped	Peripheral: ff_{xx}- PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	0.81·f_{xx}+6.2		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.83·f_{xx}+5.7		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤32MHz	0.79·f_{xx}+6.2		mA
HALT mode Note8	IDD2	All peripherals running	Peripheral: ff_{xx}- PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤32MHz	0.75·f_{xx}+3.0	1.04*f_{xx}+5.4	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.70·f_{xx}+1.9	1.00*f_{xx}+4.0	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 16MHz≤f_{xx}≤32MHz	0.56·f_{xx}+2.8	0.69*f_{xx}+7.0	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤32MHz	0.46·f_{xx}+2.8		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.44·f_{xx}+1.6		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 16MHz≤f_{xx}≤32MHz	0.46·f_{xx}+1.8		mA
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running		PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	0.151·f_{xx}+0.90	0.209·f_{xx}+ 1.93	mA
		All peripherals stopped			0.035·f_{xx}+1.01		mA
IDLE2 mode	IDD4	PLL: OFF 4MHz ≤f_{xx}≤16MHz Note7			0.037·f_{xx}+0.21	0.049·f_{xx}+ 0.88	mA

Notes: 1. VDD, EVDD and BVDD total current. (Ports are stopped).
AVREF0 current, port buffer current (including a current flowing in the on-chip pull-up/pull-down resistor) are not included.

2. The code flash and the data flash are in read mode.
When the device is in programming mode (Self-programming mode or data flash programming mode), the current value (MAX. value) adds by the following value:

- Self-programming mode:
  + In case of PLL OFF: 7-(0.33*fxx+0.1) [mA]
  + In case of PLL ON: 7-(0.18*fxx+3.0) [mA]
- Data flash programming mode:
  + 7-(0.18*fxx/4+3.0) [mA]

3. Main OSC is stopped.
4. Do not use SubOSC.
5. POC is working. 240kHz Internal-OSC is working. 8MHz Internal-OSC is stopped.
6. RC Oscillation frequency is typ.40kHz. This clock is divided by 2 internally.
7. 8MHz Internal-OSC is stopped
8. When the SSCG is running, the current value adds typ +2.5mA, max +4mA.

The formulas are for reference only. Not all possible values for f_{xx} are tested in the outgoing device inspection.