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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	CANbus, CSI, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	128
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3.3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3382m2gja-gae-ax

Table of Contents

1. Pin Group Information

1.1 Device package information

The V850ES/Fx3 device series comprises several members. An overview with the pin and package information is given in the following table:

Series Member	# Pins	Device package information
μPD70F3370A μPD70F3371	64	FE3
μPD70F3372 μPD70F3373	80	FF3
μPD70F3374 μPD70F3375 μPD70F3376A μPD70F3377A	100	FG3
μPD70F3378 μPD70F3379 μPD70F3380 μPD70F3381 μPD70F3382	144	FJ3
μPD70F3383 μPD70F3384 μPD70F3385	176	FK3

This document describes the specification for the V850ES/FJ3.

1.2 Pin Groups 1x: Pins supplied by EVDD

1B: (SHMT1)
- P04, P30-31, P34; P40, P91, P913-915 (FE3)
- P04, P30-31, P34; P38-39, P40, P91, P913-915 (FF3)
- P04, P30-31, P34; P36-39, P40, P91, P911, P913-915 (FG3)
- P04, P30-31, P34; P36-39, P40, P63-69, P614-615, P80-81, P91, P911, P913-915 (FJ3)
- P04, P30-31, P34; P36-39, P40, P63-69, P614-615, P80-81, P91, P911, P913-915, P156-157 (FK3)

1D: (SHMT3)
- P00-03, P05-P06, P32-33, P35, P41-42, P50-55, P90, P96-99 (FE3)
- P00-03, P05-P06, P32-33, P35, P41-42, P50-55, P90, P96-99 (FF3)
- P00-03, P05-P06, P10-11, P32-33, P35, P41-42, P50-55, P90, P92-910, P912 (FG3)
- P00-03, P05-P06, P10-11, P32-33, P35, P41-42, P50-55, P60-62, P610-613, P90, P92-910, P912 (FJ3)
- P00-03, P05-P06, P10-11, P32-33, P35, P41-42, P50-55, P60-62, P610-613, P90, P92-910, P912, P150-155 (FK3)

1.3 Pin Groups 2x: Pins supplied by EVDD

2A: (CMOS)
- PCM0-1 (FE3)
- PCM0-3, PCS0-1, PCT0-1, PCT4, PCT6 (FF3)

2D: (SHMT3)
- PDL0-7 (FE3)
- PDL0-11 (FF3)

2.6 DC Characteristics

2.6.1 Input/Output Level

(Ta = -40 to +85°C, C=4.7uF, VDD = EVDD = BVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High level input voltage	VIH1	Pin Group 1B		0.7·EVDD		EVDD	V
	VIH2	Pin Group 1D		0.8·EVDD		EVDD	V
		Pin Group 3D		0.8·BVDD		BVDD	V
	VIH3	Pin Group 3A		0.7·BVDD		BVDD	V
	VIH4	Pin Group 4		0.7·AVREF0		AVREF0	V
	VIH5	Pin Group 6		0.8·EVDD		EVDD	V
Low level input voltage	VIL1	Pin Group 1B		EVSS		0.3·EVDD	V
	VIL2	Pin Group 1D		EVSS		0.4·EVDD	V
		Pin Group 3D		BVSS		0.4·BVDD	V
	VIL3	Pin Group 3A		BVSS		0.3·BVDD	V
	VIL4	Pin Group 4		AVSS		0.3·AVREF0	V
	VIL5	Pin Group 6		EVSS		0.2·EVDD	V
Input hysteresis	VHYS1	Pin Group 1B	Center point at 0.5 x EVDD Note3		0.267 x EVDD - 0.51V		V
	VHYS2	Pin Group 1D	Center point at 0.6 x EVDD Note3		0.192 x EVDD - 0.31V		V
		Pin Group 3D	Center point at 0.6 x BVDD Note3		0.192 x BVDD - 0.31V		V
	VHYS5	Pin Group 6	Center point at 0.5 x EVDD Note3		0.535 x EVDD - 0.9V		V
High level output voltage Note2	VOH1	Pin Group 1x	IOH=-1.0mA	EVDD-1.0		EVDD	V
			IOH=-100uA	EVDD-0.5		EVDD	V
	VOH2	Pin Group 3x	IOH=-1.0mA	BVDD-1.0		BVDD	
			IOH=-100uA	BVDD-0.5		BVDD	V
	VOH3	Pin Group 4	IOH=-1.0mA	AVREF0-1.0		AVREF0	V
			IOH=-100uA	AVREF0-0.5		AVREF0	V
Low level output voltage Note2	VOL1	Pin Group 1x	IOL=1.0mA	0		0.4	V
		P914, 915	IOL=3.0mA				
	VOL2	Pin Group 3x	IOL=1.0mA	0		0.4	V
	VOL3	Pin Group 4	IOL=1.0mA	0		0.4	V
Software pull-up resistor	R1	VI=0V		10	30	100	kΩ
Software Note1 pull-down resistor	R2	VI=VDD		10	30	100	kΩ

Remark: The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified.

Notes: 1. $\overline{\text{DRST}}$ terminal only. (Control register is OCDM)

2. Total IOH/IOL max is 20mA/-20mA each power supply line (EVDD,BVDD and AVREF0). AVREF0 IOH/IOL current is excluding ADC current IAREF0.

3. Typical value. Not tested and guaranteed

(b) Calculation formulas

(Ta = -40 to +85°C, C=4.7uF,
VDD = EVDD = BVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V[Note1])

Mode	Symbol	Condition			TYP. [Note9]	MAX. [Note9]	Unit
Operating mode [Note2,8]	IDD1	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	1.06·f_{xx}+7.1	1.27·f_{xx}+13.6	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	1.06·f_{xx}+5.5	1.28·f_{xx}+10.6	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤48MHz	0.94·f_{xx}+6.0	1.13·f_{xx}+12.2	mA
		All peripherals stopped	Peripheral: ff_{xx}- PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	0.81·f_{xx}+6.2		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.83·f_{xx}+5.7		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤48MHz	0.79·f_{xx}+6.2		mA
HALT mode [Note8]	IDD2	All peripherals running	Peripheral: ff_{xx}- PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤32MHz	0.75·f_{xx}+3.0	1.04*f_{xx}+5.4	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.70·f_{xx}+1.9	1.00*f_{xx}+4.0	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 16MHz≤f_{xx}≤48MHz	0.56·f_{xx}+2.8	0.69*f_{xx}+7.0	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤32MHz	0.46·f_{xx}+2.8		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.44·f_{xx}+1.6		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 16MHz≤f_{xx}≤48MHz	0.46·f_{xx}+1.8		mA
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running		PLL: OFF 4MHz≤f_{xx}≤16MHz [Note7]	0.151·f_{xx}+0.90	0.210·f_{xx}+ 1.35	mA
		All peripherals stopped			0.035·f_{xx}+1.01		mA
IDLE2 mode	IDD4	PLL: OFF 4MHz ≤f_{xx}≤16MHz [Note7]			0.037·f_{xx}+0.21	0.049·f_{xx}+ 0.43	mA

Notes: 1. VDD, EVDD and BVDD total current. (Ports are stopped).
AVREF0 current, port buffer current (including a current flowing in the on-chip pull-up/pull-down resistor) are not included.

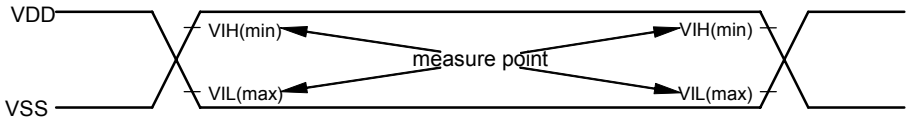
2. The code flash and the data flash are in read mode.
When the device is in programming mode (Self-programming mode or data flash programming mode), the current value (MAX. value) adds by the following value:

- Self-programming mode:
  + In case of PLL OFF: 7-(0.33*fxx+0.1) [mA]
  + In case of PLL ON: 7-(0.18*fxx+3.0) [mA]
- Data flash programming mode:
  + 7-(0.18*fxx/4+3.0) [mA]

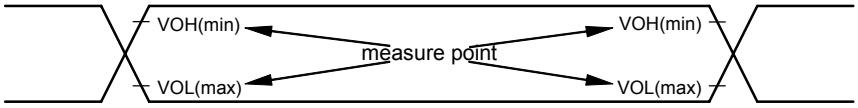
3. Main OSC is stopped.
4. Do not use SubOSC.
5. POC is working. 240kHz Internal-OSC is working. 8MHz Internal-OSC is stopped.
6. RC Oscillation frequency is typ.40kHz. This clock is divided by 2 internally.
7. 8MHz Internal-OSC is stopped
8. When the SSCG is running, the current value adds typ +2.5mA, max +4mA.
9. The formulas are for reference only. Not all possible values for f_{xx} are tested in the outgoing device inspection.

2.7 AC Characteristics

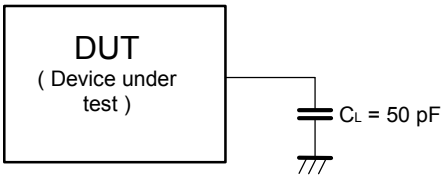
AC test Input measurement points (VDD, AVREF0, EVDD, BVDD)



AC test output measurement points



Load conditions



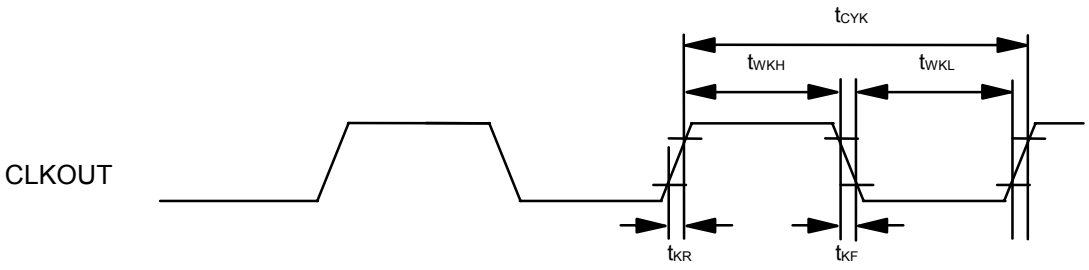
Caution: If the load capacitance exceeds 50pF due to the circuit configuration, reduce the load capacitance of the device to 50pF or less by inserting a buffer or by some other means.

2.7.1 CLKOUT Output Timing

(Ta = -40 to +85°C, VDD = EVDD = BVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output cycle	tCYK	VDD = EVDD = BVDD = 4.0V ~ 5.5V	31.25ns	80μs	
		VDD = EVDD = BVDD = 3.5V ~ 5.5V	50ns		
High level width	tWKH	VDD = EVDD = BVDD = 4.0V ~ 5.5V	tCYK/2-13		ns
		VDD = EVDD = BVDD = 3.5V ~ 5.5V	tCYK/2-15		
Low level width	tWKL	VDD = EVDD = BVDD = 4.0V ~ 5.5V	tCYK/2-13		ns
		VDD = EVDD = BVDD = 3.5V ~ 5.5V	tCYK/2-15		
Rise time	tKR	VDD = EVDD = BVDD = 4.0V ~ 5.5V		13	ns
		VDD = EVDD = BVDD = 3.5V ~ 5.5V		15	
Fall time	tKF	VDD = EVDD = BVDD = 4.0V ~ 5.5V		13	ns
		VDD = EVDD = BVDD = 3.5V ~ 5.5V		15	

CLKOUT output timing



2.7.3 RESET, Interrupt, ADTRG Timing

(Ta = -40 to +85°C, VDD = EVDD = BVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
_RESET input low level width	tWRSL	analog filter	250			ns
NMI input high level width	tWNIH	analog filter	250			ns
NMI input low level width	tWNIL	analog filter	250			ns
INTPn[Note1] input high level width	tWITH	analog filter ,n=0-14	250			ns
		digital filter ,n=3	Note2			ns
INTPn [Note1] input low level width	tWITL	analog filter ,n=0-14	250			ns
		digital filter ,n=3	Note2			ns

Notes: 1. ADTRG is same spec (P03/INTP0/ADTRG). $\overline{\text{DRST}}$ is same spec (P05/INTP2/$\overline{\text{DRST}}$)

2. 2Tsamp+20 or 3Tsamp+20 ("Tsamp" is Noise reject sampling clock (NF macro))

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. $\overline{\text{RESET}}$, NMI, INTPn, ADTRG and $\overline{\text{DRST}}$ have analog noise filter. The typical filter time is typ=60ns.

2.7.4 Key Return Timing

(Ta = -40 to +85°C, VDD = EVDD = BVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
KRn input high level width	tWKRH	analog filter ,n=0-7	250			ns
KRn input low level width	tWKRL	analog filter ,n=0-7	250			ns

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. KRn inputs have analog noise filter. The typical filter time is typ=60ns.

2.7.5 Timer Timing

(Ta = -40 to +85°C, VDD = EVDD = BVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
TI input high level width	tTIH	TIAA00-01,10-11,20-21,30-31,40-41 [Note1] TIAB00-03,10-13,20-23 [Note1]		250			ns
TI input low level width	tTIL	TIAA00-01,10-11,20-21,30-31,40-41 [Note1] TIAB00-03,10-13,20-23 [Note1]		250			ns
TO output cycle	tTCYK	TIAA00-01,10-11,20-21,30-31, 40-41 [Note1] TIAB00-03,10-13,20-23 [Note1]	4.0V≤VDD≤5.5V			16	MHz
			3.5V≤VDD<4.0V			10	MHz

Notes: 1. Except for the external trigger and external event function.

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. TIAAn and TIABn inputs have analog noise filter. The typical filter time is typ=60ns.

2.7.6 CSI Timing

(a) Master mode

(Ta = -40 to +85°C, VDD = EVDD = BVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V, CL=50pF)

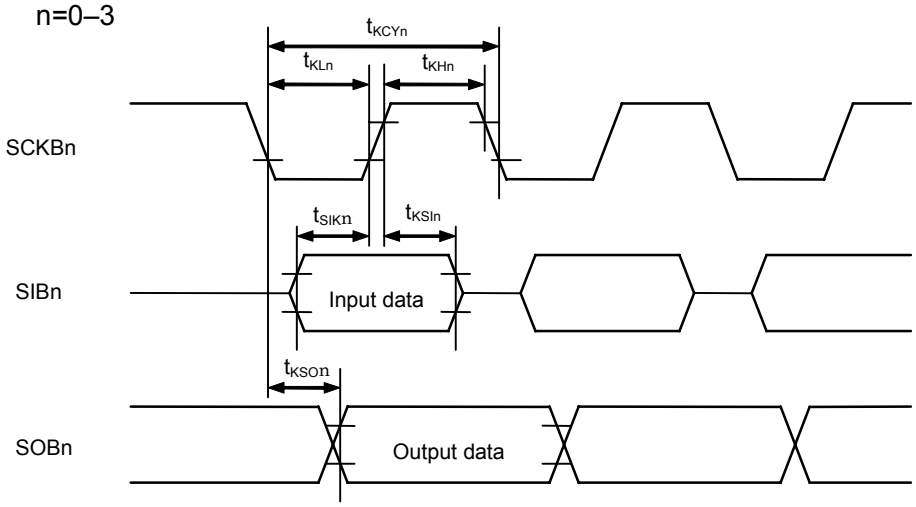
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCKBn cycle time	tKCY1		125		ns
SCKBn high level width	tKH1		tKCY1/2-15		ns
SCKBn low level width	tKL1		tKCY1/2-15		ns
SIBn setup time (to SCKBn)	tSIK1		30		ns
SIBn hold time (from SCKBn)	tKSI1		25		ns
Delay time from SCKBn to SOBn	tKSO1			25	ns

(b) Slave mode

(Ta = -40 to +85°C, VDD = EVDD = BVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCKBn cycle time	tKCY1		200		ns
SCKBn high level width	tKH1		90		ns
SCKBn low level width	tKL1		90		ns
SIBn setup time (to SCKBn)	tSIK1		50		ns
SIBn hold time (from SCKBn)	tKSI1		50		ns
Delay time from SCKBn to SOBn	tKSO1			50	ns

CSIBn n=0–3



2.7.7 UART Timing

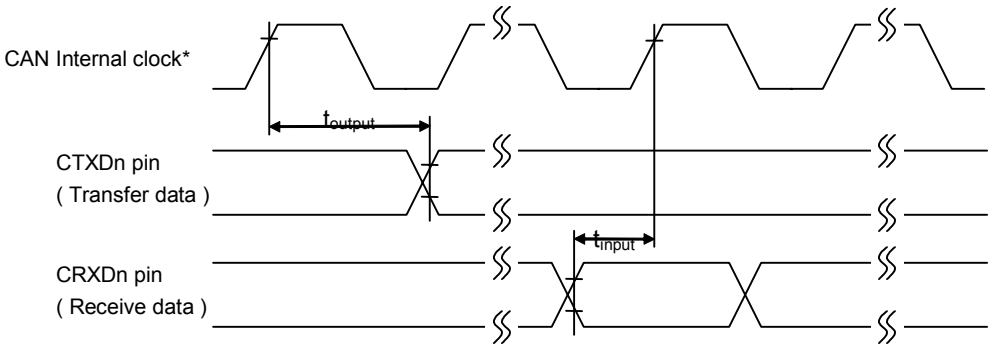
(Ta = -40 to +85°C, VDD = EVDD = BVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					1.5	Mbps
ASCK0 frequency					10	MHz

2.7.9 CAN Timing

(Ta = -40 to +85°C, VDD = EVDD = BVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					1	Mbps
Internal delay time					100	ns



Internal delay time (tNODE)= Internal Transfer Delay(t_{output}) + Internal Receive Delay(t_{input})

*) CAN Internal clock (f_{CAN}) :CAN baud rate clock

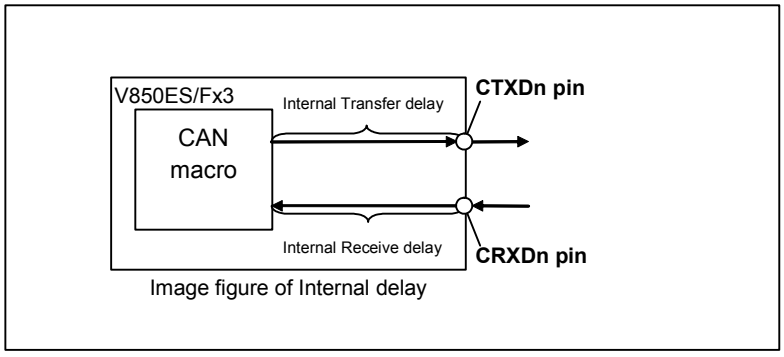


Image figure of Internal delay

3. Electrical Specifications of (A1)-Grade

This product has to be used only under the conditions of VDD=EVDD=BVDD. Operation is not ensured at the time of using this product except this condition.

3.1 Absolute Maximum Ratings

AbsAbsolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	VDD	VDD=EVDD=BVDD,		-0.5 to +6.5	V
	EVDD	VDD=EVDD=BVDD		-0.5 to +6.5	V
	BVDD	VDD=EVDD=BVDD		-0.5 to +6.5	V
	AVREF0			-0.5 to +6.5	V
	VSS	VSS=EVSS=BVSS=AVSS		-0.5 to +0.5	V
	EVSS	VSS=EVSS=BVSS=AVSS		-0.5 to +0.5	V
	BVSS	VSS=EVSS=BVSS=AVSS		-0.5 to +0.5	V
	AVSS	VSS=EVSS=BVSS=AVSS		-0.5 to +0.5	V
Input voltage	VI1	Pin Group 1x, 6		-0.5 to EVDD+0.5 Note1	V
	VI2	Pin Group 3x		-0.5 to BVDD+0.5 Note1	V
	VI3	Pin Group 7		-0.5 to VRO+0.5 Note1	V
Analog input voltage	VIAN	Pin Group 4		-0.5 to AVREF0+0.5 Note1	V
High level output current	IOH	Pin Group 1x	1 pin	-4	mA
			Total	-20	mA
		Pin Group 3x	1 pin	-4	mA
			Total	-20	mA
		Pin Group 4	1 pin	-4	mA
			Total	-10 Note2	mA
Low level output current	IOL	Pin Group 1x	1 pin	4	mA
			Total	20	mA
		Pin Group 3x	1 pin	4	mA
			Total	20	mA
		Pin Group 4	1 pin	4	mA
			Total	10 Note2	mA
Operating ambient temperature	Ta	Normal operating mode		-40 to +110	°C
		Flash programming mode		-40 to +110	
Storage temperature	Tstg			-40 to +125	°C

Remarks: 1. The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified

Notes: 1. Be sure not to exceed the absolute maximum ratings (Max. value) of each supply voltage.
2. Excluding ADC IAREF0 current.

3.2 Capacities

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.3 Operating condition

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.4 Voltage Regulator Characteristics

Specification is identical to that from (A)-Grade except Ta=-40 to +110°C.

3.6 DC Characteristics

3.6.1 Input/Output Level

(Ta = -40 to +110°C, C=4.7uF, VDD = EVDD = BVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V)

Parameter	Sym-bol	Conditions		MIN.	TYP.	MAX.	Unit
High level input voltage	VIH1	Pin Group 1B		0.7·EVDD		EVDD	V
	VIH2	Pin Group 1D		0.8·EVDD		EVDD	V
		Pin Group 3D		0.8·BVDD		BVDD	V
	VIH3	Pin Group 3A		0.7·BVDD		BVDD	V
	VIH4	Pin Group 4		0.7·AVREF0		AVREF0	V
	VIH5	Pin Group 6		0.8·EVDD		EVDD	V
Low level input voltage	VIL1	Pin Group 1B		EVSS		0.3·EVDD	V
	VIL2	Pin Group 1D		EVSS		0.4·EVDD	V
		Pin Group 3D		BVSS		0.4·BVDD	V
	VIL3	Pin Group 3A		BVSS		0.3·BVDD	V
	VIL4	Pin Group 4		AVSS		0.3·AVREF0	V
	VIL5	Pin Group 6		EVSS		0.2·EVDD	V
Input hysteresis	VHYS1	Pin Group 1B	Center point at 0.5 x EVDD Note3		0.267 x EVDD - 0.51V		V
	VHYS2	Pin Group 1D	Center point at 0.6 x EVDD Note3		0.192 x EVDD - 0.31V		V
		Pin Group 3D	Center point at 0.6 x BVDD Note3		0.192 x BVDD - 0.31V		V
	VHYS5	Pin Group 6	Center point at 0.5 x EVDD Note3		0.535 x EVDD - 0.9V		V
High level output voltage Note2	VOH1	Pin Group 1x	IOH=-1.0mA	EVDD-1.0		EVDD	V
			IOH=-100uA	EVDD-0.5		EVDD	V
	VOH2	Pin Group 3x	IOH=-1.0mA	BVDD-1.0		BVDD	
			IOH=-100uA	BVDD-0.5		BVDD	V
	VOH3	Pin Group 4	IOH=-1.0mA	AVREF0-1.0		AVREF0	V
			IOH=-100uA	AVREF0-0.5		AVREF0	V
Low level output voltage Note2	VOL1	Pin Group 1x	IOL=1.0mA	0		0.4	V
		P914, 915	IOL=3.0mA				
	VOL2	Pin Group 3x	IOL=1.0mA	0		0.4	V
	VOL3	Pin Group 4	IOL=1.0mA	0		0.4	V
Software pull-up resistor	R1	VI=0V		10	30	100	kΩ
Software Note1 pull-down resistor	R2	VI=VDD		10	30	100	kΩ

Remark: The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified.

Notes: 1. $\overline{\text{DRST}}$ terminal only. (Control register is OCDM)

2. Total IOH/IOL max is 20mA/-20mA for the power supply lines EVDD and BVDD.
Total IOH/IOL max is 10mA/-10mA for the power supply line AVREF0.
AVREF0 IOH/IOL current is excluding ADC current IAREF0.

3. Typical value. Not tested and guaranteed

3.6.3.3 µPD70F3381, µPD70F3382

(a) Absolute values

(Ta = -40 to +110°C, C=4.7uF,
VDD = EVDD = BVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V[Note1])

Mode	Symbol	Condition				TYP.	MAX.	Unit
Operating mode Note2,8	IDD1	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_x=5MHz	30	41	mA
					f_{xx}=32MHz f_x=16MHz	43	57	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	15	22	mA
					f_{xx}=16MHz f_x=16MHz	24	32	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤48MHz	f_{xx}=48MHz f_x=12MHz	53	68	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_x=5MHz	23		mA
					f_{xx}=32MHz f_x=16MHz	33		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	13		mA
					f_{xx}=16MHz f_x=16MHz	19		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤48MHz	f_{xx}=48MHz f_x=12MHz	46		mA
HALT mode Note8	IDD2	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_x=5MHz	19	28	mA
					f_{xx}=32MHz f_x=16MHz	28	40	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	9	14	mA
					f_{xx}=16MHz f_x=16MHz	15	22	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤48MHz	f_{xx}=48MHz f_x=12MHz	31	42	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_x=5MHz	13		mA
					f_{xx}=32MHz f_x=16MHz	18		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	6		mA
					f_{xx}=16MHz f_x=16MHz	10		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤48MHz	f_{xx}=48MHz f_x=12MHz	25		mA

4. Electrical Specifications of (A2)-Grade

This product has to be used only under the conditions of VDD=EVDD=BVDD. Operation is not ensured at the time of using this product except this condition.

4.1 Absolute Maximum Ratings

Specification is identical to that from (A1)-Grade except

- Operating ambient temperature Ta = -40 to +125°C
- Note2: AVREF0 IOH/IOL current is including ADC max. current IAREF0.

4.2 Capacities

Specification is identical to that from (A)-Grade except Ta=-40 to +125°C.

4.3 Operating condition

(Ta = -40 to +125°C, C=4.7uF, VDD = EVDD = BVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V)

Internal System clock frequency (f_{VBCLK})	Supply voltage	Operating Condition

4.0≤f_{XX}≤24MHz (≤256KB product)
4.0≤f_{XX}≤32MHz (≥384KB product)
Note1
	4.0V≤VDD≤5.5V Note2	Operation of functions is usable under following conditions:
		• Peripheral clock frequency
		  • $f_{XP1} \leq f_{XX}$
		  • $f_{XP2} \leq f_{XX}$
		• AC characteristics:
		  • Refer to chapter '4.7 AC Characteristics' for details.

	3.5V≤VDD<4.0V Note2	Operation of functions is usable under following conditions:
		• Peripheral clock frequency
		  • $f_{XP1} \leq$ 20MHz
		  • $f_{XP2} \leq$ 20MHz
		• AC characteristics:
		  • Refer to chapter '4.7 AC Characteristics' for details.

	3.3V≤VDD<3.5V Note2	Only operation of the following functions is assured: • CPU • Flash (include programming) • RAM • IO Buffer • Port • WT • WDT • INT • CLM • POC • LVI

	3.3V≤AVREF0≤5.5V	• A/D Converter
		  • Refer to chapter '4.8 A/D Converter' for details.
		  • stop ADC for AVREF0 < 4.0V (ADA0CE bit =0)

12.5kHz≤f_{XT}≤27.5kHz Note3(RC)	3.3V≤VDD<5.5V Note2	-
f_{RL} (240kHz Internal-OSC)	3.3V≤VDD<5.5V Note2	-

Notes: 1. For using SSCG please refer to '4.5.5 SSCG Characteristics' for details
2. VDD = EVDD = BVDD
3. RC Oscillation frequency is min. 25kHz max. 55kHz. This clock is divided by 2 internally.

4.4 Voltage Regulator Characteristics

Specification is identical to that from (A)-Grade except Ta=-40 to +125°C.

4.5 Clock Generator Circuit

4.5.1 Main System Clock Oscillation Circuit Characteristics

Specification is identical to that from (A)-Grade except Ta=-40 to +125°C.

Mode	Symbol	Condition		TYP.	MAX.	Unit
IDLE2 mode	IDD4	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_X=5MHz	0.4	1.1	mA
			f_{xx}=12MHz f_X=12MHz	0.7	1.5	mA
			f_{xx}=16MHz f_X=16MHz	0.8	1.7	mA
		fxx=8MHz, 8MHz Internal-OSC Note3		0.2	1.0	mA
SUB operating mode Note5	IDD5	RC resonator (fxt=20kHz) Note6		80	850	μA
		240 kHz Internal-OSC (SubOSC stopped)		220	1450	μA
SubIDLE mode Note3,5	IDD6	RC resonator (fxt=20kHz) Note6		40	670	μA
		240kHz Internal-OSC (SubOSC stopped)		25	630	μA
STOP mode Note3,4	IDD7	POC stop	240kHz Internal-OSC stop	7.5	530	μA
			240kHz Internal-OSC working	15.5	545	μA
		POC work	240kHz Internal-OSC stop	10.5	535	μA
			240kHz Internal-OSC working	18.5	550	μA

(b) Calculation formulas

(Ta = -40 to +125°C, C=4.7uF,
VDD = EVDD = BVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V[Note1])

Mode	Symbol	Condition			TYP. [Note9]	MAX. [Note3]	Unit
Operating mode Note2,8	IDD1	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤24MHz	1.03·f_{xx}+7.1	1.24·f_{xx}+13.6	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	1.03·f_{xx}+5.5	1.24·f_{xx}+10.6	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤24MHz	0.92·f_{xx}+6.0	1.11·f_{xx}+12.2	mA
		All peripherals stopped	Peripheral: ff$_{xx}$- PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤24MHz	0.81·f_{xx}+6.2		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.83·f_{xx}+5.7		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 12MHz≤f_{xx}≤24MHz	0.79·f_{xx}+6.2		mA
HALT mode Note8	IDD2	All peripherals running	Peripheral: ff$_{xx}$- PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤24MHz	0.75·f_{xx}+3.0	1.04*f_{xx}+5.4	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.70·f_{xx}+1.9	1.00*f_{xx}+4.0	mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 16MHz≤f_{xx}≤24MHz	0.56·f_{xx}+2.8	0.69*f_{xx}+7.0	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤24MHz	0.46·f_{xx}+2.8		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.44·f_{xx}+1.6		mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 16MHz≤f_{xx}≤24MHz	0.46·f_{xx}+1.8		mA
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running		PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	0.151·f_{xx}+0.90	0.209·f_{xx}+ 1.93	mA
		All peripherals stopped			0.035·f_{xx}+1.01		mA
IDLE2 mode	IDD4	PLL: OFF 4MHz ≤f_{xx}≤16MHz Note7			0.037·f_{xx}+0.21	0.049·f_{xx}+ 0.88	mA

Notes: 1. VDD, EVDD and BVDD total current. (Ports are stopped).
AVREF0 current, port buffer current (including a current flowing in the on-chip pull-up/pull-down resistor) are not included.

2. The code flash and the data flash are in read mode.
When the device is in programming mode (Self-programming mode or data flash programming mode), the current value (MAX. value) adds by the following value:

- Self-programming mode:
  + In case of PLL OFF: 7-(0.33*fxx+0.1) [mA]
  + In case of PLL ON: 7-(0.18*fxx+3.0) [mA]
- Data flash programming mode:
  + 7-(0.18*fxx/4+3.0) [mA]

3. Main OSC is stopped.
4. Do not use SubOSC.
5. POC is working. 240kHz Internal-OSC is working. 8MHz Internal-OSC is stopped.
6. RC Oscillation frequency is typ.40kHz. This clock is divided by 2 internally.
7. 8MHz Internal-OSC is stopped
8. When the SSCG is running, the current value adds typ +2.5mA, max +4mA.
9. The formulas are for reference only. Not all possible values for f_{xx} are tested in the outgoing device inspection.

4.6.3.3 µPD70F3381, µPD70F3382

(a) Absolute values

(Ta = -40 to +125°C, C=4.7uF,
VDD = EVDD = BVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V[Note1])

Mode	Symbol	Condition				TYP.	MAX.	Unit
Operating mode Note2,8	IDD1	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_X=5MHz	30	41	mA
					f_{xx}=32MHz f_X=16MHz	43	57	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	15	22	mA
					f_{xx}=16MHz f_X=16MHz	24	32	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_X=5MHz	23		mA
					f_{xx}=32MHz f_X=16MHz	33		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	13		mA
					f_{xx}=16MHz f_X=16MHz	19		mA
HALT mode Note8	IDD2	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_X=5MHz	19	28	mA
					f_{xx}=32MHz f_X=16MHz	28	40	mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	9	14	mA
					f_{xx}=16MHz f_X=16MHz	15	22	mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 12MHz≤f_{xx}≤32MHz	f_{xx}=20MHz f_X=5MHz	13		mA
					f_{xx}=32MHz f_X=16MHz	18		mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	6		mA
					f_{xx}=16MHz f_X=16MHz	10		mA

4.13 Flash Memory Programming Characteristics

(a) Basic Characteristics

(C=4.7uF, VDD = EVDD = BVDD, AVREF0 = 3.5 to 5.5V, VSS = EVSS = BVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operation frequency	fCPU	≤256KB product	4		24	MHz
		≥384KB product	4		32	
Supply voltage	VDD		3.3		5.5	V
Number of rewrites	CWRT1	Code Flash	1000			count
		Data Flash				
	CWRT2		10000			
High level input voltage	VIH	FLMD0	0.8EVDD		EVDD	V
Low level input voltage	VIL	FLMD0	EVSS		0.2EVDD	V
Programming temperature	tPRG		-40		+125	°C
Data retention		Code Flash			15[Note1]	year
		Data Flash				
					5[Note2]	

Notes: 1. Under the condition of CWRT1
2. Under the condition of CWRT2

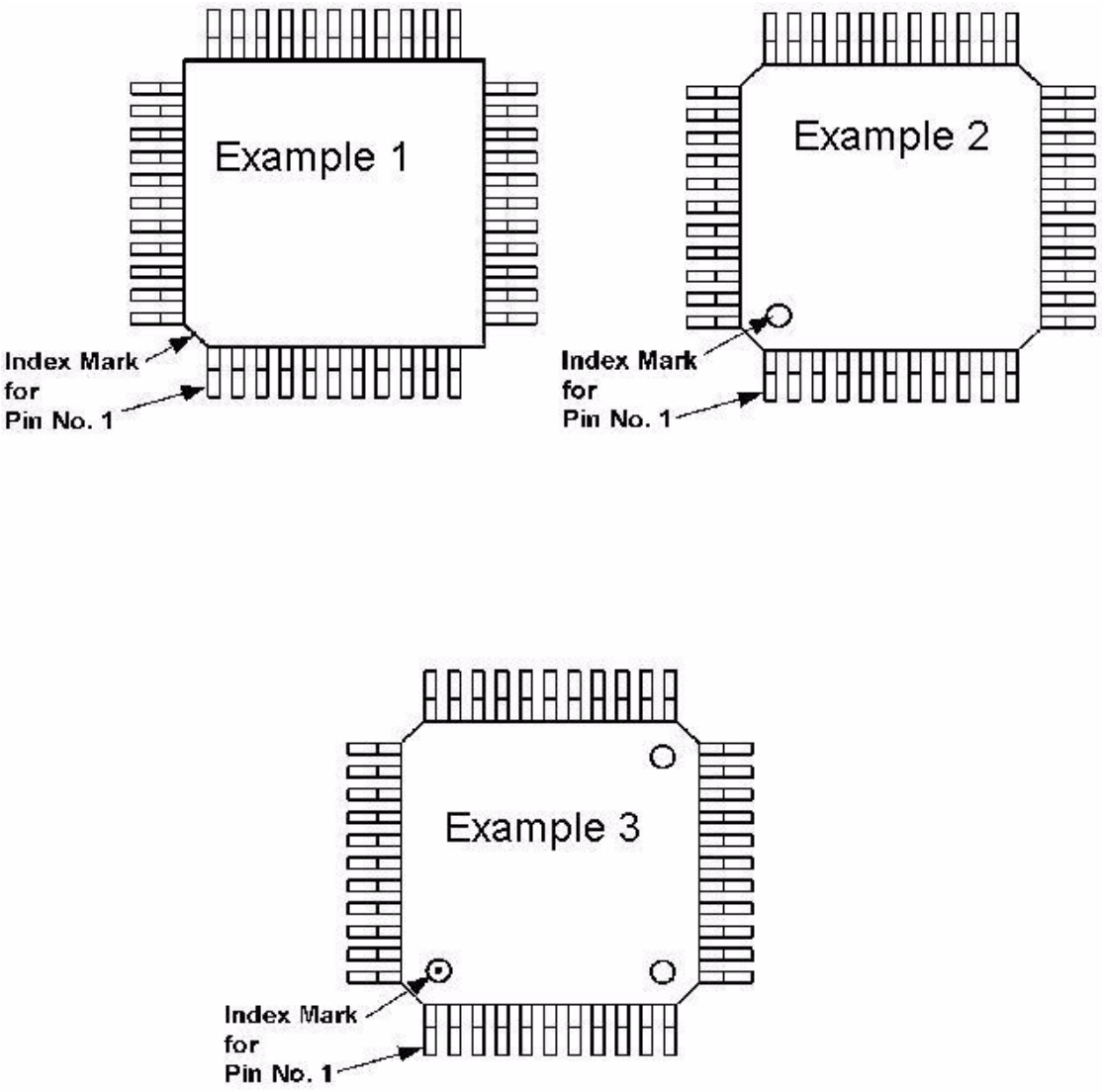
Remark: The initial write when the product is shipped, any erase → write set of operations, or any programming operation is counted as one rewrite.
Example: P: Program(write) E: Erase
Product is shipped → P → E → P → E → P : Rewrite count: 3
Product is shipped → E → P → E → P → E → P : Rewrite count: 3

(b) Serial Writing Operation Characteristics

Specification is identical to that from (A)-Grade except Ta=-40 to +125°C.

5.2 Product Marking

5.2.1 Marking of pin 1 at a QFP (Quad Flat Package)



Example 1: The index mark for pin 1 is the beveled edge of the package

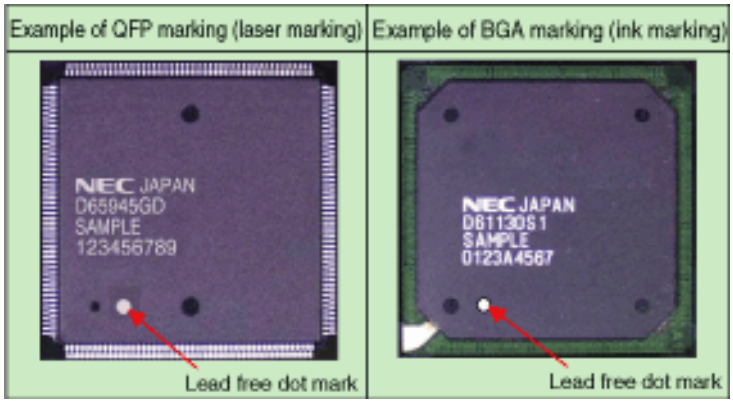
Example 2: The index mark for pin 1 is a round notch at one of the 4 edges. In this case, the shape of all edges is identical (usually beveled).

Example 3: For production reasons, two or more similar notches may be located at the top of the package. In such a case the index marker for pin 1 is a round notch with an additional mark in it.

Note: RoHS compliant devices have an additional dot at the top side. Do not mix it up with the marking for pin 1. For details see 5.2.2 "Identification of Lead-Free Products" on page 79.

5.2.2 Identification of Lead-Free Products

Lead-Free products are marked with a dot "•". The marking methods are the paint or the laser (It doesn't sink in). The shape of lead-free marks is a circle.
Example:



[MEMO]