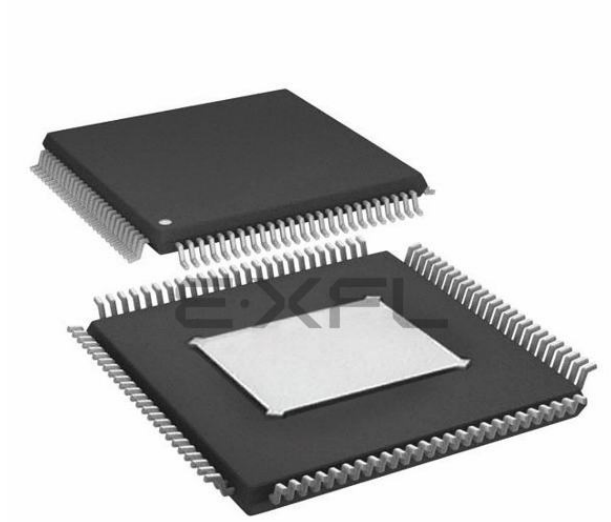

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Sigma
Interface	I²C, SPI
Clock Rate	172MHz
Non-Volatile Memory	-
On-Chip RAM	46kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP Exposed Pad
Supplier Device Package	100-TQFP-EP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adau1442ysvz-3a-rl

GENERAL DESCRIPTION

The ADAU1442/ADAU1445/ADAU1446 are enhanced audio processors that allow full flexibility in routing all input and output signals. The SigmaDSP® core features full 28-bit processing (56-bit in double-precision mode), synchronous parameter loading for ensuring filter stability, and 100% code efficiency with the SigmaStudio™ tools. This DSP allows system designers to compensate for the real-world limitations of speakers, amplifiers, and listening environments, resulting in a dramatic improvement of the perceived audio quality through speaker equalization, multiband compression, limiting, and third-party branded algorithms.

The flexible audio routing matrix (FARM) allows the user to multiplex inputs from multiple sources running at various sample rates to or from the SigmaDSP core. This drastically reduces the complexity of signal routing and clocking issues in the audio system. FARM includes up to eight stereo asynchronous sample rate converters (depending on the device model), Sony/Philips Digital Interconnect Format (S/PDIF) input and output, and serial (I^2S) and time division multiplexing (TDM) I/Os. Any of these inputs can be routed to the SigmaDSP core or to any of the asynchronous sample rate converters (ASRCs). Similarly, any one of the output signals can be taken from the SigmaDSP core or from any of the ASRC outputs. This routing scheme, which can be modified at any time via control registers, allows for maximum system flexibility.

The ADAU1442, ADAU1445, and ADAU1446 differ only in ASRC functionality and packaging. The ADAU1442/ADAU1445 contain 16 channels of ASRCs and are packaged in TQFP packages, whereas the ADAU1446 contains no ASRCs and is packaged in an LQFP. The ADAU1442 can handle nine clock domains, the ADAU1445 can handle three clock domains, and the ADAU1446 can handle one clock domain.

The ADAU1442/ADAU1445/ADAU1446 can be controlled in one of two operational modes: the settings of the chip can be loaded and dynamically updated through the SPI/I^2C® port, or the DSP can self-boot from an external EEPROM in a system with no microcontroller. There is also a bank of multipurpose (MP) pins that can be used as general-purpose digital I/Os or as inputs to the 4-channel auxiliary control ADC.

The ADAU1442/ADAU1445/ADAU1446 are supported by the SigmaStudio graphical development environment. This software includes audio processing blocks such as FIR and IIR filters, dynamics processors, mixers, low level DSP functions, and third-party algorithms for fast development of custom signal flows.

Table 1.

Device	ASRC Channels	ASRC Clock Domains	Package
ADAU1442	16	8	TQFP
ADAU1445	16	2	TQFP
ADAU1446	0	N/A	LQFP

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
I/O Sample Rate Ratio	1:8		7.75:1		
THD + N		−133	−120	dB	
CRYSTAL OSCILLATOR					
Transconductance		40		mS	
REGULATOR[2]					
DVDD Voltage	1.65	1.75	1.85	V	Maximum 500 mA load.

[1] To calculate the group delay, refer to the SRC Group Delay section.
[2] Regulator specifications are calculated using an NJT4030P transistor from On Semiconductor in the circuit.

AVDD = 3.3 V ± 10%, DVDD = 1.8 V ± 10%, PVDD = 3.3 V, IOVDD = 3.3 V ± 10%, T_A = −40°C to +105°C, master clock input = 12.288 MHz, core clock f_{CORE} = 172.032 MHz, I/O pins set to 2 mA drive setting, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG PERFORMANCE					AVDD = 3.3 V ± 10%.
Auxiliary Analog Inputs					
Resolution		10		Bits	
Full-Scale Analog Input		AVDD		V	
Integral Nonlinearity (INL)	−2.3		+2.3	LSB	
Differential Nonlinearity (DNL)	−2.0		+2.0	LSB	
Gain Error	−2.0		+2.0	LSB	
Input Impedance		200		kΩ	
Sample Rate		f_{CORE}/896		kHz	4:1 multiplexed input, each channel at f_{CORE}/3584. For f_{CORE} = 172.032 MHz, each channel is sampled at 48 kHz.
DIGITAL I/O					
Input Voltage, High (V_{IH})	0.7 × IOVDD			V	Digital input pins except SPDIFI.[1]
Input Voltage, Low (V_{IL})			0.3 × IOVDD	V	Digital input pins except SPDIFI.[1]
Input Leakage, High (I_{IH}) at 3.3 V	−2		+2	µA	Digital input pins except MCLK and SPDIFI.
	−2		+8	µA	MCLK.
	60		140	µA	SPDIFI.
Input Leakage, Low (I_{IL}) at 0 V	−85		−10	µA	All other pins.
	−2		+2	µA	CLKMODEx, RSVD, PLLx, RESET.
	−8		+2	µA	MCLK.
	−140		−60	µA	SPDIFI.
High Level Output Voltage (V_{OH})	0.85 × IOVDD			V	I_{OH} = 1 mA.
Low Level Output Voltage (V_{OL})			0.1 × IOVDD	V	I_{OL} = 1 mA.
Input Capacitance (C_I)		5		pF	Guaranteed by design.
Multipurpose Pins Output Drive		2		mA	These pins are not designed for static current draw and should not drive LEDs directly.
POWER					
Supply Voltage					
Analog Voltage (AVDD)	2.97	3.3	3.63	V	
Digital Voltage (DVDD)	1.62	1.8	1.98	V	
PLL Voltage (PVDD)	2.97	3.3	3.63	V	
IOVDD Voltage (IOVDD)	2.97	3.3	3.63	V	
Supply Current					
Analog Current (AVDD)		2		mA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PLL Current (PVDD)		10		mA	
I/O Current (IOVDD)		10		mA	Depends greatly on the number of active serial ports, clock pins, and characteristics of external loads.
Maximum Digital Current (DVDD)					
ADAU1442			460	mA	Test program includes 24 channels I/O, fully utilized program RAM.
ADAU1445			365	mA	Test program includes 24 channels I/O, fully utilized program RAM.
ADAU1446			315	mA	Test program includes 24 channels I/O, fully utilized program RAM.
Power Dissipation					
AVDD, DVDD, PVDD During Operation of ADAU1442			960	mW	All supplies at nominal +10%, IOVDD is not included in measurement.
AVDD, DVDD, PVDD During Operation of ADAU1445			780	mW	All supplies at nominal +10%, IOVDD is not included in measurement.
AVDD, DVDD, PVDD During Operation of ADAU1446			675	mW	All supplies at nominal +10%, IOVDD is not included in measurement.
Reset, All Supplies		94		mW	
ASYNCHRONOUS SAMPLE RATE CONVERTERS[2]					
Dynamic Range		139		dB	A-weighted, 20 Hz to 20 kHz.
I/O Sample Rate	6		192	kHz	
I/O Sample Rate Ratio	1:8		7.75:1		
THD + N		−133	−120	dB	
CRYSTAL OSCILLATOR					
Transconductance		40		mS	
REGULATOR[3]					
DVDD Voltage	1.65	1.75	1.85	V	Maximum 500 mA load.

[1] SPDIFI input voltage range exceeds the requirements of the S/PDIF specification.
[2] To calculate the group delay, refer to the SRC Group Delay section.
[3] Regulator specifications are calculated using an NJT4030P transistor from On Semiconductor in the circuit.

Digital Timing Diagrams

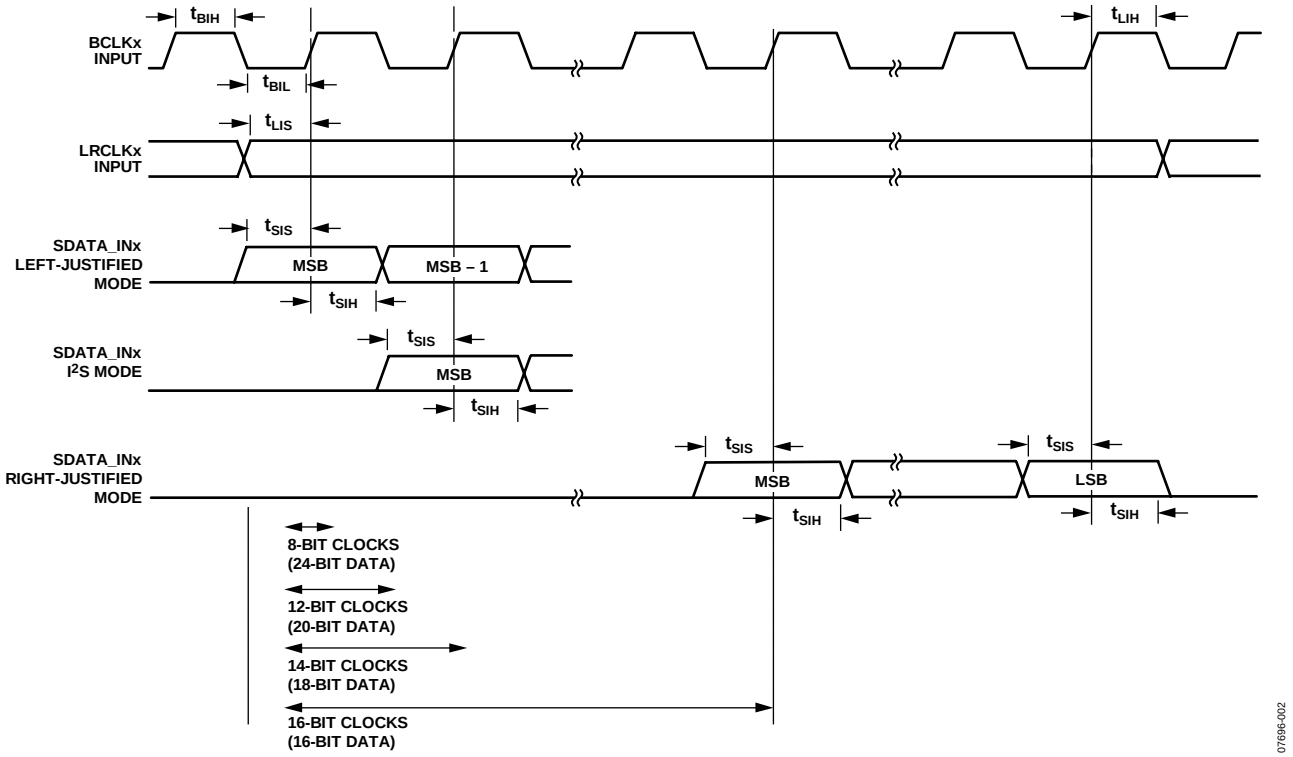


Figure 2. Serial Input Port Timing

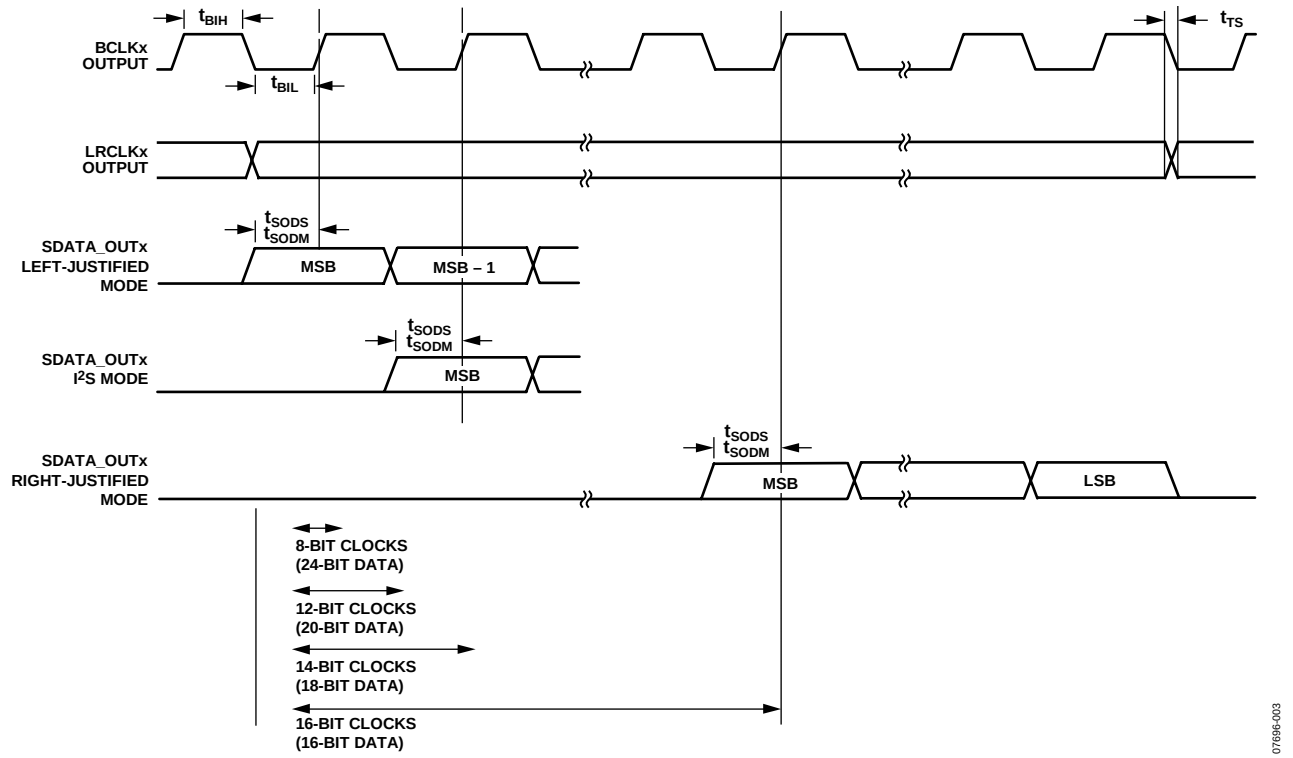
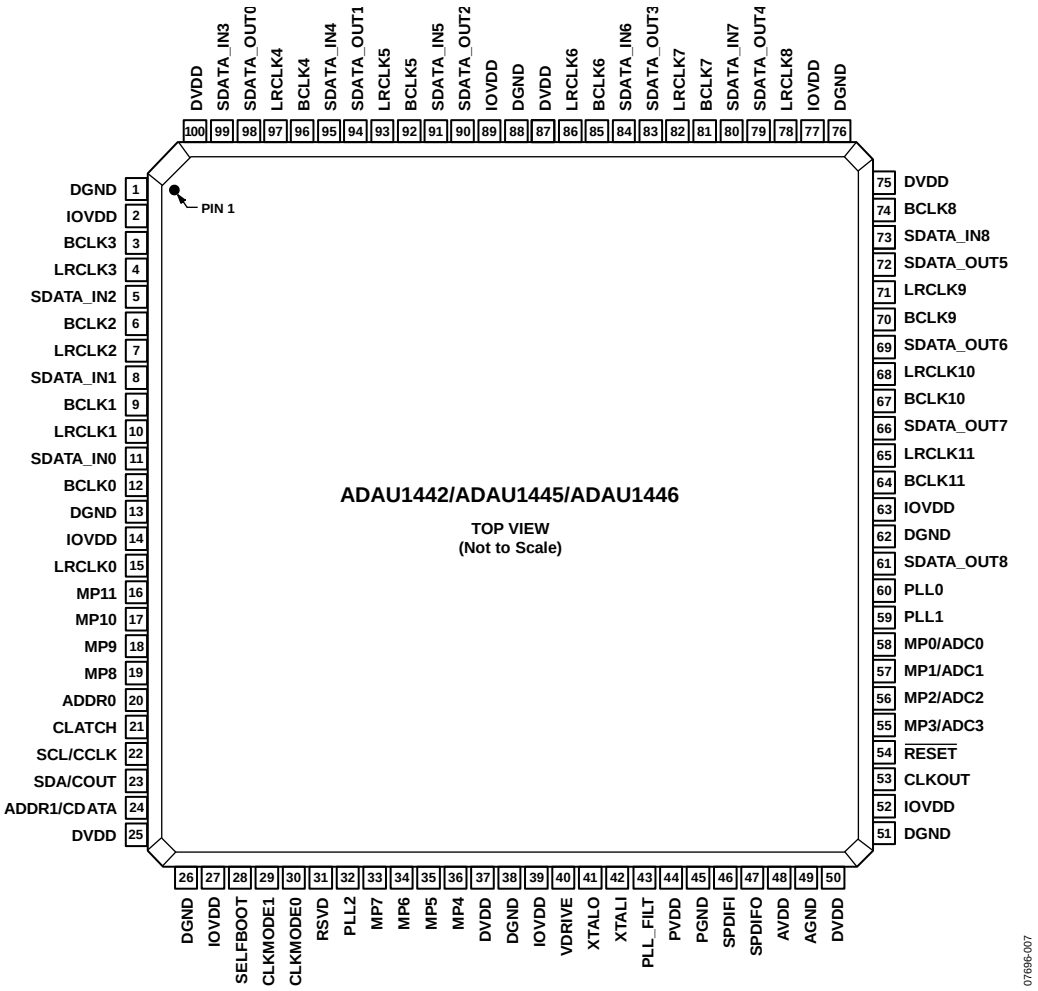


Figure 3. Serial Output Port Timing

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD DOES NOT HAVE AN INTERNAL ELECTRICAL CONNECTION TO THE INTEGRATED CIRCUIT, BUT SHOULD BE CONNECTED TO THE GROUND PLANE OF THE PCB FOR PROPER HEAT DISSIPATION.

Figure 7. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 13, 26, 38, 51, 62, 76, 88	DGND	PWR	Digital Ground. The AGND, DGND, and PGND pins should be tied directly together in a common ground plane. DGND pins should be decoupled to a DVDD pin with a 100 nF capacitor.
2, 14, 27, 39, 52, 63, 77, 89	IOVDD	PWR	Input and Output Supply. The voltage on this pin sets the highest input voltage that should be present on the digital input pins. This pin is also the supply for the digital output signals on the clock, data, control port, and MP pins. IOVDD should always be set to 3.3 V. The current draw of this pin is variable because it is dependent on the loads of the digital outputs.
3	BCLK3	D_IO	Bit Clock, Input/Output Clock Domain 3. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 3 is set up as a master or slave. When not used, this pin can be left disconnected.
4	LRCLK3	D_IO	Frame Clock, Input/Output Clock Domain 3. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 3 is set up as a master or slave. When not used, this pin can be left disconnected.
5	SDATA_IN2	D_IN	Serial Data Port 2 Input. When not used, this pin can be left disconnected.

Pin No.	Mnemonic	Type[1]	Description
96	BCLK4	D_IO	Bit Clock, Input/Output Clock Domain 4. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 4 is set up as a master or slave. When not used, this pin can be left disconnected.
97	LRCLK4	D_IO	Frame Clock, Input/Output Clock Domain 4. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 4 is set up as a master or slave. When not used, this pin can be left disconnected.
98	SDATA_OUT0	D_OUT	Serial Data Port 0 Output. When not used, this pin can be left disconnected.
99	SDATA_IN3	D_IN	Serial Data Port 3 Output. When not used, this pin can be left disconnected.

[1] PWR = power/ground, A_IN = analog input, D_IN = digital input, A_OUT = analog output, D_OUT = digital output, D_IO = digital input/output.

OVERVIEW

The ADAU1442/ADAU1445/ADAU1446 are each a 24-channel audio DSP with an integrated S/PDIF receiver and transmitter, flexible serial audio ports, up to 16 channels of asynchronous sample rate converters (ASRCs), flexible audio routing, and user interface capabilities. Signal processing capabilities include equalization, crossover, bass enhancement, multiband dynamics processing, delay compensation, speaker compensation, and stereo image widening. These algorithms can be used to compensate for the real-world limitations of speakers, amplifiers, and listening environments, resulting in an improvement in the perceived audio quality.

An on-board oscillator can be connected to an external crystal to generate the master clock. A phase-locked loop (PLL) allows the ADAU1442/ADAU1445/ADAU1446 to be clocked from a variety of clock frequencies. The PLL can accept inputs of 64 × f_S, 128 × f_S, 256 × f_S, 384 × f_S, or 512 × f_S to generate the internal master clock of the core, where f_S is the sampling rate of audio in normal-rate processing mode. In dual- or quad-rate mode, these multipliers are halved or quartered, respectively. System sample rates include, but are not limited to, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, and 192 kHz.

Each ADAU1442/ADAU1445/ADAU1446 operates from a 1.8 V digital power supply and a 3.3 V analog supply. An on-board voltage regulator can be used to operate the chip from a single 3.3 V supply.

The ADAU1442/ADAU1445/ADAU1446 have a sophisticated control port that supports complete read and write capability of all memory locations, excluding read-only addresses. Control registers are provided to offer complete control of the chip's configuration and serial modes. Handshaking is included for ease of memory uploads and downloads. The ADAU1442/ADAU1445/ADAU1446 can be configured for either SPI or I²C control. Program RAM, parameter RAM, and register contents can be saved in an external EEPROM, from which the ADAU1442/ADAU1445/ADAU1446 can self-boot on startup.

The ADAU1442/ADAU1445/ADAU1446 serial ports operate with digital audio I/Os in the I²S, left-justified, right-justified, or TDM-compatible mode. The flexible serial data ports allow for direct interconnection to a variety of ADCs, DACs, and general-purpose DSPs. The combination of an on-board S/PDIF transmitter and receiver and 16 channels of ASRCs allows for easy compatibility with an extensive number of external devices, and a system with up to nine sampling rates.

The flexible audio routing matrix (FARM) is a system of multiplexers used to distribute the audio signals in the ADAU1442/ADAU1445/ADAU1446 among the serial inputs and outputs, audio core, and ASRCs. FARM can easily be configured by setting the appropriate registers.

The ADAU1442, ADAU1445, and ADAU1446 are distinguished by the number of on-board ASRCs and maximum sample rates. The ADAU1442 contains eight 2-channel ASRCs, the ADAU1445 contains two 8-channel ASRCs, and the ADAU1446 has no ASRCs.

Two sets of serial ports at the input and output can operate in a special flexible TDM mode, which allows the user to independently assign byte-specific locations to audio streams at varying bit depths. This mode ensures compatibility with codecs using similar flexible TDM streams.

The core of the ADAU1442/ADAU1445/ADAU1446 is a 28-bit DSP (or a 56-bit DSP when using double-precision mode) optimized for audio processing, and it can process audio at sample rates of up to 192 kHz. The program and parameter RAMs can be loaded with a custom audio processing signal flow built with the SigmaStudio graphical programming software from Analog Devices, Inc. The values stored in the parameter RAM control individual signal processing blocks, such as IIR and FIR equalization filters, dynamics processors, audio delays, and mixer levels. A software safeload feature allows for transparent parameter updates and prevents clicks on the output signals.

Reliability features such as a CRC and program counter watchdog help ensure that the system can detect and recover from any errors related to memory corruption.

S/PDIF signals can be routed through an ASRC for processing in the DSP or can be sent directly to output on MP pins for recovery of the embedded audio signal. Other components of the embedded signal, including status and user bits, are not lost and can be output on the MP pins as well.

Multipurpose (MP) pins are available for providing a simple user interface without the need for an external microcontroller. Twelve pins are available to input external control signals and output flags or controls to other devices in the system. Four of these can alternatively be assigned to an auxiliary ADC for use with analog controls such as potentiometers or system voltages. As inputs, MP pins can be connected to push buttons, switches, rotary encoders, potentiometers, or other external control circuitry to control the internal signal processing program. When configured as outputs, these pins can be used to drive LEDs (with a buffer), to output flags to a microcontroller, to control other ICs, or to connect to other external circuitry in an application.

The SigmaStudio software is used to program and control the ADAU1442/ADAU1445/ADAU1446 through the control port. Along with designing and tuning a signal flow, the software can configure all of the DSP registers in real time and download a new program and parameter into the external self-boot EEPROM. SigmaStudio's easy-to-use graphical interface allows anyone with audio processing knowledge to easily design a DSP signal flow and port it to a target application without the need for writing line-level code. At the same time, the software provides enough flexibility and programmability for an experienced DSP programmer to have in-depth control of the design. In SigmaStudio, the user can add signal processing cells from the library by dragging and dropping cells, connect them together in a flow, compile the design, and load the program and parameter files into the ADAU1442/ADAU1445/ADAU1446 memory through the control port. The complicated tasks of linking, compiling, and downloading the project are all handled automatically by the software.

Table 9. PLL Modes

DSP Core Rate[1]	Input to MCLK (XTALI Pin)	PLL2	PLL1	PLL0	PLL Divider[2]	Core Clock Multiplier	Core Clock (f_{CORE})	Instructions per Sample
Normal	64 × $f_{S,NORMAL}$	0	0	0	1	56	3584 × $f_{S,NORMAL}$	3584
	128 × $f_{S,NORMAL}$	0	0	1	2	56	3584 × $f_{S,NORMAL}$	3584
	256 × $f_{S,NORMAL}$	0	1	0	4	56	3584 × $f_{S,NORMAL}$	3584
	384 × $f_{S,NORMAL}$	0	1	1	6	56	3584 × $f_{S,NORMAL}$	3584
	512 × $f_{S,NORMAL}$	1	0	0	8	56	3584 × $f_{S,NORMAL}$	3584
Dual	32 × $f_{S,DUAL}$	0	0	0	1	56	1792 × $f_{S,DUAL}$	1792
	64 × $f_{S,DUAL}$	0	0	1	2	56	1792 × $f_{S,DUAL}$	1792
	128 × $f_{S,DUAL}$	0	1	0	4	56	1792 × $f_{S,DUAL}$	1792
	192 × $f_{S,DUAL}$	0	1	1	6	56	1792 × $f_{S,DUAL}$	1792
	256 × $f_{S,DUAL}$	1	0	0	8	56	1792 × $f_{S,DUAL}$	1792
Quad	16 × $f_{S,QUAD}$	0	0	0	1	56	896 × $f_{S,QUAD}$	896
	32 × $f_{S,QUAD}$	0	0	1	2	56	896 × $f_{S,QUAD}$	896
	64 × $f_{S,QUAD}$	0	1	0	4	56	896 × $f_{S,QUAD}$	896
	96 × $f_{S,QUAD}$	0	1	1	6	56	896 × $f_{S,QUAD}$	896
	128 × $f_{S,QUAD}$	1	0	0	8	56	896 × $f_{S,QUAD}$	896

[1] If the normal DSP core rate ($f_{S,NORMAL}$) is 44.1 kHz, the dual DSP core rate ($f_{S,DUAL}$) is 88.2 kHz, and the quad DSP core rate ($f_{S,QUAD}$) is 176.4 kHz. Likewise, if $f_{S,NORMAL}$ is 48 kHz, then $f_{S,DUAL}$ is 96 kHz and $f_{S,QUAD}$ is 192 kHz.
[2] The PLL divider is set by the PLLx pins.

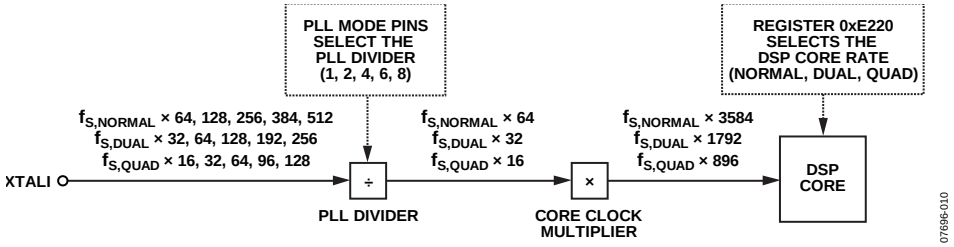


Figure 10. Master Clock Signal Flow

VOLTAGE REGULATOR

The digital supply voltage of the ADAU1442/ADAU1445/ADAU1446 must be set to 1.8 V. The chip includes an on-board voltage regulator that allows the device to be used in systems where a 1.8 V supply is not available but a 3.3 V supply is. The only external components needed for this are a PNP transistor and one resistor. Only one pin, VDRIVE, is necessary to support the regulator.

The recommended design for the voltage regulator is shown in Figure 12. The 10 µF and 100 nF capacitors shown in this schematic are recommended for bypassing but are not necessary for operation. Each DVDD pin should have its own 100 nF bypass capacitor, but only one bulk capacitor (10 µF) is needed for all pins. In this design, 3.3 V is the main system voltage; 1.8 V is generated at the collector of the transistor, which is connected to the DVDD pins. VDRIVE is connected to the base of the PNP transistor. If the regulator is not used in the design, VDRIVE can be tied to ground.

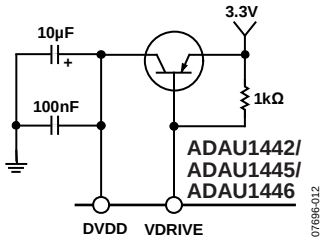


Figure 12. Voltage Regulator Design

Two specifications must be considered when choosing a regulator transistor: the current amplification factor (h_{FE} or beta) should be at least 200, and the collector must be able to dissipate the heat generated when regulating from 3.3 V to 1.8 V. The maximum digital current draw of the ADAU1442 and ADAU1445, which use ASRCs, is 310 mA. The equation to determine the minimum power dissipation specifications of the transistor is as follows:

$$(3.3\text{ V} - 1.8\text{ V}) \times 310\text{ mA} = 465\text{ mW}$$

Many transistors fit these specifications. Analog Devices recommends the NJT4030P from On Semiconductor. For projects with stringent size constraints, an FMMT734 from Zetex can be used.

The ADAU1446, which does not contain ASRCs, has a lower maximum digital current draw of approximately 235 mA. The maximum power dissipation of the transistor in this case should be around 355 mW.

SRC GROUP DELAY

The group delay of the sample rate converter is dependent on the input and output sampling frequencies as described in the following equations.

For $f_{S\_OUT} > f_{S\_IN}$,

$$GDS = \frac{16}{f_{S\_IN}} + \frac{32}{f_{S\_IN}}$$

For $f_{S\_OUT} < f_{S\_IN}$,

$$GDS = \frac{16}{f_{S\_IN}} + \left(\frac{32}{f_{S\_IN}}\right) \times \left(\frac{f_{S\_IN}}{f_{S\_OUT}}\right)$$

where *GDS* is the group delay in seconds.

SERIAL DATA INPUT/OUTPUT

The flexible serial data input and output ports of the ADAU1442/ADAU1445/ADAU1446 can be set to accept or transmit data in a 2-channel (usually I²S format), packed TDM4, or standard 4-, 8-, or 16-channel TDM stream. Data is processed in twos complement, MSB-first format. The left-channel data field always precedes the right-channel data field in 2-channel streams. In the TDMn modes (where n represents the total number of channels in the stream), Slot 0 to Slot (n/2) − 1 fall in the first half of the audio frame, and Slot n/2 to Slot n − 1 are in the second half of the frame. TDM mode allows fewer serial data pins to be used, freeing more pins for other data streams. The serial modes are set in the serial output port modes and serial input port modes control registers.

When referring to audio data streams, the terms *TDM2* and *I²S* should be treated with care. In this document, *TDM2* refers to any 2-channel stream, whereas *I²S* refers specifically to a 2-channel, negative BCLK polarity, negative LRCLK polarity, MSB delay-by-1 stream.

The serial data clocks are fully bidirectional and do not need to be synchronous with the ADAU1442/ADAU1445/ADAU1446 master clock input. However, asynchronous data streams must be routed through an on-board asynchronous sample rate converter to be processed in the core.

The input control registers allow control of clock polarity and data input modes. All common data formats are available with flexible MSB start, bit depth (24-, 20-, or 16-bit), and TDM settings. In all modes except the right-justified modes, the serial port accepts an arbitrary number of bits up to a limit of 24. Extra bits do not cause an error, but they are truncated internally. Proper operation of the right-justified modes requires that there be exactly 64 BCLKs per audio frame (for 2-channel data). The LRCLK in TDM mode can be input to the ADAU1442/ADAU1445/ADAU1446 either as a 50/50 duty cycle clock or as a bit-wide pulse.

In TDM mode, the bit clock supplied by the ADAU1442/ADAU1445/ADAU1446 in master mode is limited to 25 MHz. This, in turn, limits the sampling rate at which it can supply master clocks in various TDM modes. Table 18 displays the modes in which the serial output port functions for some common audio sample rates.

The output control registers give the user control of clock polarities, clock frequencies, clock types, and data format. In all modes except the right-justified modes (MSB delayed by 8, 12, or 16), the serial port accepts an arbitrary number of bits up to a limit of 24. Extra bits do not cause an error, but are truncated internally. Proper operation of the right-justified modes requires the LSB to align with the edge of the LRCLK. The default settings of all serial port control registers correspond to 2-channel, I²S mode, and 24-bit slave mode, and these registers are set as slaves to the clock domain corresponding to their channel number.

Table 18. Serial Input and Output Port TDM Capabilities

Mode	BCLK Cycles per Frame	f_S (kHz)	BCLK Frequency (MHz)	Valid Mode
TDM2	64	44.1	2.8224	Yes
	64	48	3.072	Yes
	64	88.2	5.6448	Yes
	64	96	6.144	Yes
	64	192	12.288	Yes
TDM4	128	44.1	5.6448	Yes
	128	48	6.144	Yes
	128	88.2	11.2896	Yes
	128	96	12.288	Yes
	128	192	24.576	Yes
TDM8	256	44.1	11.2896	Yes
	256	48	12.288	Yes
	256	88.2	22.5792	Yes
	256	96	24.576	Yes
	256	192	49.152	No[1]
TDM16	512	44.1	22.5792	Yes
	512	48	24.576	Yes
	512	88.2	45.1584	No[1]
	512	96	49.152	No[1]
	512	192	98.304	No[1]

[1] The device will not work in this mode.

Connections to an external DAC are handled exclusively with the output port pins. The output LRCLKx and BCLKx pins can be set to be either master or slave, and the SDATA_OUT pins are used to output data from the SigmaDSP to the external DAC.

Table 19 shows the proper configurations for standard audio data formats, and Figure 21 presents an overview of the serial data input/output ports.

Serial Clock Domains

There are 12 clock domains (pairs of LRCLKx and BCLKx pins) available in the ADAU1442/ADAU1445/ADAU1446. Of these, three are available exclusively to the serial data input ports, three are available exclusively to the serial data output ports, and the remaining six can be assigned to clock either input or output ports.

The ADAU1442 contains eight 2-channel ASRCs and the ADAU1445 contains two 8-channel ASRCs, whereas the ADAU1446 contains no ASRCs. However, all clock domain pins are available on every device. In a system with no sample rate conversion and with serial ports in slave mode, at least two pairs of LRCLKx and BCLKx pins must be connected: one pair for the input serial ports and one pair for the output serial ports. If all serial ports are in master mode and synchronous, then only one pair of LRCLKx and BCLKx pins needs to be connected.

Figure 27 shows a simplified view of the assignment of clock domains to the input and output sides of the chip. Note that each clock domain comprises two signals, namely the BCLK (bit clock) and LRCLK (frame clock). Therefore, the 12 clock domains contain a total of 24 clock signals.

Each clock domain is capable of acting as a master or slave. For this reason, all LRCLK and BCLK pins are bidirectional. In slave mode, the LRCLK and BCLK pins receive clock signals from an external source, such as a codec. In master mode, the LRCLK and BCLK pins output clock signals to external slave ICs.

Although a clock domain in slave mode can clock an arbitrary number of serial ports, a clock domain in master mode can only clock a single serial port. For Clock Domains[2:0] and Clock Domains[11:9], the corresponding serial port is fixed as an input or output. For assignable clock domains (Clock Domains[8:3]), the corresponding serial port can be either an input or output, depending on the setting of the clock pad multiplexer register (see Table 20 for more details).

Table 20. Master Mode Clock Domain Assignment

Clock Domain	Chip Pins	Serial Port
0	LRCLK0, BCLK0	SDATA_IN0
1	LRCLK1, BCLK1	SDATA_IN1
2	LRCLK2, BCLK2	SDATA_IN2
3	LRCLK3, BCLK3	SDATA_IN3 or SDATA_OUT3[1]
4	LRCLK4, BCLK4	SDATA_IN4 or SDATA_OUT4[1]
5	LRCLK5, BCLK5	SDATA_IN5 or SDATA_OUT5[1]
6	LRCLK6, BCLK6	SDATA_IN6 or SDATA_OUT6[1]
7	LRCLK7, BCLK7	SDATA_IN7 or SDATA_OUT7[1]
8	LRCLK8, BCLK8	SDATA_IN8 or SDATA_OUT8[1]
9	LRCLK9, BCLK9	SDATA_OUT0
10	LRCLK10, BCLK10	SDATA_OUT1
11	LRCLK11, BCLK11	SDATA_OUT2

[1] Depends on the setting of the clock pad multiplexer register (Address 0xE240).

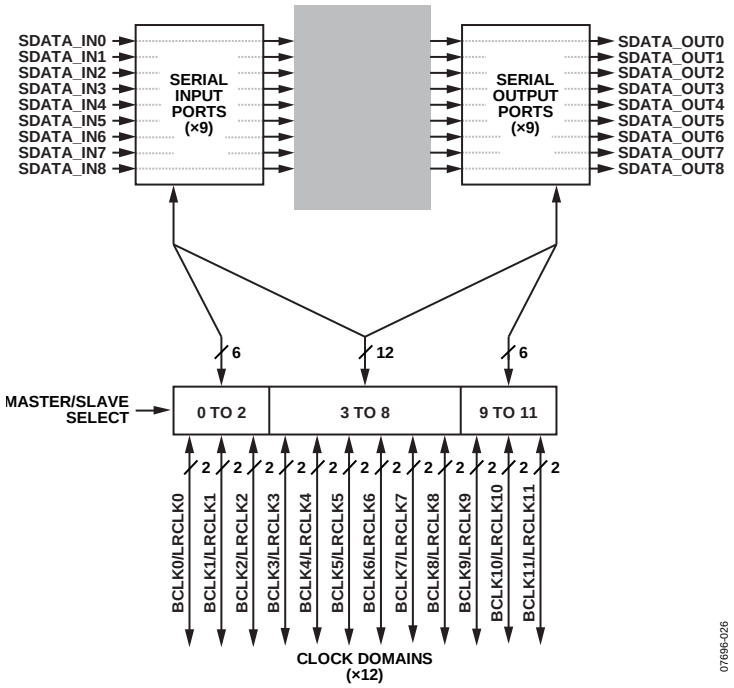


Figure 27. Simplified Serial Clock Domain Assignment

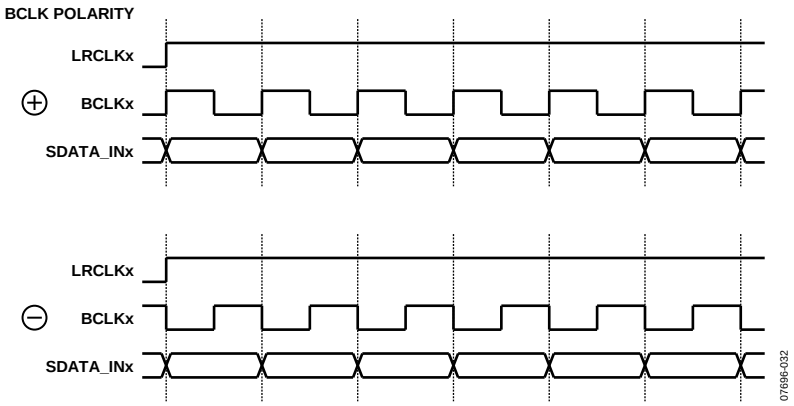


Figure 31. Serial Input BCLK Polarity

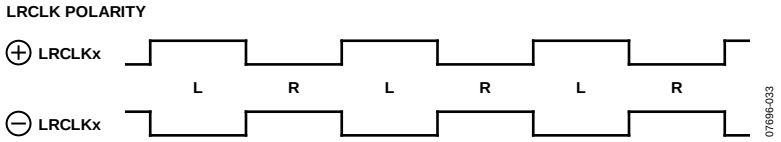


Figure 32. Serial Input LRCLK Polarity

Word Length Bits (Bits[7:6])

These bits set the word length of the input data to 16, 20, or 24 bits. If the input signal has more data bits than this word length, the extra bits are truncated. The fourth setting is flexible TDM. For more information, see the Serial Input Flexible TDM Interface Modes section.

MSB Position Bits (Bits[5:3])

These bits set the position of the MSB in the data stream.

TDM Type (Bits[2:0])

These bits set the number of channels contained in the data stream. The possible choices are TDM2 (stereo), TDM4, TDM8 or flexible TDM, TDM16, and packed TDM4 mode. For more information on the packed TDM4 mode, see the Packed TDM4 Mode section. If the word length bits (Bits[7:6]) are set to 11 for flexible TDM mode, then TDM type bits (Bits[2:0]) must also be set for flexible TDM mode (that is, set to 010).

In master mode, the ADAU1442/ADAU1445/ADAU1446 can generate either an LRCLK clock signal (50% duty cycle) or an LRCLK synchronization pulse at the specified frequency ($f_{S,NORMAL}$, $f_{S,DUAL}$, or $f_{S,QUAD}$). When a pulse is generated, its width is equal to one single internal BCLK. Each channel requires 32 BCLK cycles per LRCLK. Therefore, for TDM4, 128 BCLK cycles are required; for TDM8, 256 BCLK cycles; for TDM16, 512 BCLK cycles; for TDM2, 64 BCLK cycles (except when the LRCLK signal is a 50% duty cycle signal (that is, not a pulse) or when it is running in I²S or left-justified mode); and for packed TDM4, 64 BCLK cycles.

SERIAL OUTPUT PORTS

The serial output ports convert 16-, 20-, and 24-bit audio signals coming from the audio processor to standard I²S and TDM signals on the serial data outputs. They support TDM2, TDM4, TDM8, and TDM16 time division multiplexing schemes and I²S, left-justified, right-justified, and MSB delay-by-12 and delay-by-16 modes. Different clock polarities and multiple word lengths are supported, as well as the capability to drive in master mode or to be driven in slave mode.

The serial output ports are composed of up to nine clock domains (Clock Domain 3 to Clock Domain 11) and up to nine serial data signals (SDATA_IN0 to SDATA_IN8).

In slave mode, the nine serial output clock domains are driven directly from the corresponding nine pairs of LRCLKx and BCLKx pins on the IC. Three pairs of LRCLKx and BCLKx pins (LRCLK[11:9] and BCLK[11:9]) are hardwired to Clock Domains[11:9], which are serial outputs. The remaining six pairs of LRCLKx and BCLKx pins (LRCLK[8:3] and BCLK[8:3]) are multiplexed to Clock Domains[8:3] as either inputs or outputs. The multiplexer can be set to use these signals as output clock domains by writing to Bits[5:0] of the clock pad multiplexer register (Address 0xE240) as explained in Table 27. This configuration is also valid in master mode.

Table 27. Output Clock Domain Multiplexing

Clock Domain	Chip Pins	Register 0xE240 Setting
0	LRCLK9, BCLK9	N/A
1	LRCLK10, BCLK10	N/A
2	LRCLK11, BCLK11	N/A
3	LRCLK3, BCLK3	Set Bit 0 to 1
4	LRCLK4, BCLK4	Set Bit 1 to 1
5	LRCLK5, BCLK5	Set Bit 2 to 1
6	LRCLK6, BCLK6	Set Bit 3 to 1
7	LRCLK7, BCLK7	Set Bit 4 to 1
8	LRCLK8, BCLK8	Set Bit 5 to 1

Figure 33 shows in detail how the clocks are routed to and from the serial output ports. For the assignable clock domains (Clock Domains[8:3]), the clock pad multiplexer allows each clock domain to be individually routed to either the serial input ports or to the serial output ports. In slave mode, the clock domain

ASRC Input Select Pairs[7:0] Registers (Address 0xE080 to Address 0xE087)

The inputs to each of the eight ASRCs can come from any stereo pair from either the serial input channels or the DSP core.

In the case of the ADAU1442, each input to the stereo ASRCs can receive a separate data input.

In the case of the ADAU1445, each input to the stereo ASRCs can receive a separate data input; however, all inputs to Stereo ASRC[3:0] must be synchronous to each other, and all inputs to Stereo ASRC[7:4] must be synchronous to each other. The first group of ASRCs (Stereo ASRC[3:0]) takes its input rate from the Stereo ASRC 0 input, and the second group of ASRCs (Stereo ASRC[7:4]) takes its input rate from Stereo ASRC 4 input.

In the case of the ADAU1446, which contains no ASRCs, these registers do not affect system operation in any way and can be ignored.

Table 33. Bit Descriptions of ASRC Input Select Pairs[7:0] Registers

Bit Position	Description	Default
[15:6]	Reserved	
[5:0]	ASRC input data selector 000000 = Serial Input Pair 0 (Channel 0, Channel 1) 000001 = Serial Input Pair 1 (Channel 2, Channel 3) 000010 = Serial Input Pair 2 (Channel 4, Channel 5) 000011 = Serial Input Pair 3 (Channel 6, Channel 7) 000100 = Serial Input Pair 4 (Channel 8, Channel 9) 000101 = Serial Input Pair 5 (Channel 10, Channel 11) 000110 = Serial Input Pair 6 (Channel 12, Channel 13) 000111 = Serial Input Pair 7 (Channel 14, Channel 15) 001000 = Serial Input Pair 8 (Channel 16, Channel 17) 001001 = Serial Input Pair 9 (Channel 18, Channel 19) 001010 = Serial Input Pair 10 (Channel 20, Channel 21) 001011 = Serial Input Pair 11 (Channel 22, Channel 23) 010000 = DSP-to-ASRC Pair 0 (Channel 0, Channel 1) 010001 = DSP-to-ASRC Pair 1 (Channel 2, Channel 3) 010010 = DSP-to-ASRC Pair 2 (Channel 4, Channel 5) 010011 = DSP-to-ASRC Pair 3 (Channel 6, Channel 7) 010100 = DSP-to-ASRC Pair 4 (Channel 8, Channel 9) 010101 = DSP-to-ASRC Pair 5 (Channel 10, Channel 11) 010110 = DSP-to-ASRC Pair 6 (Channel 12, Channel 13) 010111 = DSP-to-ASRC Pair 7 (Channel 14, Channel 15) 100000 = S/PDIF Receiver Pair 0 (Channel 0, Channel 1) 111111 = no data	111111

Serial Output Data Selector Bits (Bits[5:0])

These bits select where each of the 12 stereo serial output channels comes from. The channels can come either from one of the 12 DSP core stereo outputs or from one of the eight ASRC stereo outputs.

In the case of the ADAU1446, setting the serial output data selector bits to a value corresponding to an ASRC output pair yields no data.

As shown in Figure 50, the stereo output pairs can come from any of the DSP serial or ASRC outputs.

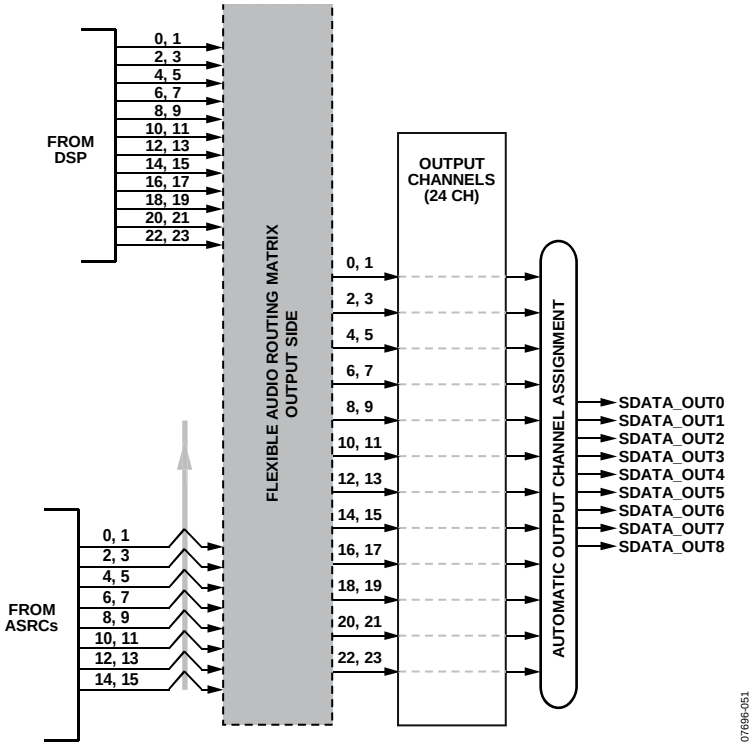


Figure 50. Serial Output Select Pair

Every sample rate converter pair for Stereo ASRC[7:4]) can be muted. This function is controlled by a single 12-bit register. The mute bits (Bits[3:0]) are active high; therefore, a value of 1 mutes the corresponding ASRC, and a value of 0 unmutes the corresponding ASRC. The muting is done with a volume ramp and is click and pop free. If desired, the mute ramp can be disabled (see the Stereo ASRC[7:4] Mute Ramp Disable Register (Address 0xE143) section).

When the device is powered up and brought out of reset, the ASRC lock bits default to a value of 0. When the master clocks to the ASRC are enabled (see the Master Clock Enable Switch Register (Address 0xE280) section), the corresponding ASRC lock bits are set to 1, and the outputs are automatically muted. When an ASRC's output rate is set (see the ASRC Output Rate Select Pairs[7:0] Registers (Address 0xE088 to Address 0xE08F) section) and it locks to a valid output clock, the corresponding lock bit changes from 1 to 0. This signifies that the ASRC has found the target clock rate and locked to it. From that moment onward, the lock bit remains at 0 until the device is reset. Changing the target rate setting or removing the output clock from the ASRC will not cause its lock bit to change from 0 back to 1.

In the case of the ADAU1446, setting these registers does not affect system operation in any way.

Stereo ASRC[7:4] Mute Ramp Disable Register (Address 0xE143)

Table 40. Bit Descriptions of Register 0xE143

Bit Position	Description	Default
[15:1]	Reserved	
0	Stereo ASRC[7:4] (Channels[15:8]) mute ramp disable 0 = enable ramp 1 = disable ramp	0

This single-bit register controls the mute behavior of Stereo ASRC[7:4] (Channels[15:8]). When Bit 0 is set to the default (0), Stereo ASRC[7:4] (Channels[15:8]) mute with a volume ramp. When Bit 0 is set to 1, Stereo ASRC[7:4] mute abruptly. In addition, setting this bit to 1 ignores the ASRC mute bits (Bits[3:0]) in Register 0xE141 (see the Stereo ASRC[7:4] Lock Status and Mute Register (Address 0xE141) section); therefore, a mute only occurs on a loss of lock.

In the case of the ADAU1446, setting this register does not affect system operation in any way.

Auxiliary Outputs—Set Enable Mode Register (Address 0xE0C8)

Table 59. Bit Descriptions of Register 0xE0C8

Bit Position	Description	Default
[15:2]	Reserved	
[1:0]	Auxiliary outputs enable mode 00 = auxiliary outputs are always off. 01 = auxiliary outputs are always on. 10 = auxiliary outputs are off on reset. (They switch on as soon as the hot enable bit is 1 and switch off as soon as the S/PDIF lock bit is 0.)	01

This register controls when the S/PDIF stream is active on the multipurpose pins when the S/PDIF to I²S mode is active. For more information, see the Enable S/PDIF to I²S Output section.

Setting Bits[1:0] of Register 0xE0C8 to 10 (auxiliary outputs are off on reset) is useful for situations in which the S/PDIF stream may be interrupted unexpectedly. An interruption causes the S/PDIF lock bit to go low, which in turn disables the auxiliary outputs. When the S/PDIF stream is recovered, the hot enable bit must be activated to restore the auxiliary outputs (see the Set Hot Enable Register (Address 0xE0CA) section for more information).

S/PDIF Lock Bit Detection Register (Address 0xE0C9)

Table 60. Bit Descriptions of Register 0xE0C9

Bit Position	Description
[15:1]	Reserved
0	S/PDIF input lock bit (read only) 0 = no valid input stream 1 = successful lock to input stream

This read-only register shows the status of the S/PDIF input lock bit.

Set Hot Enable Register (Address 0xE0CA)

Table 61. Bit Descriptions of Register 0xE0CA

Bit Position	Description	Default
[15:1]	Reserved	
0	Hot enable bit 0 = hot enable inactive 1 = hot enable active	0

This register allows the hot enable bit to be set, which restarts the auxiliary outputs when they are configured so that the auxiliary outputs are off on a reset (that is, Bits[1:0] of Register 0xE0C8 are set to 10). The hot enable bit is set to 0 automatically in the event that the S/PDIF receiver loses lock. For more information, see the Auxiliary Outputs—Set Enable Mode Register (Address 0xE0C8) section.

Read Enable Auxiliary Output Register (Address 0xE0CB)

Table 62. Bit Descriptions of Register 0xE0CB

Bit Position	Description
[15:1]	Reserved
0	Read enable auxiliary output (read only) 0 = S/PDIF auxiliary outputs disabled 1 = S/PDIF auxiliary outputs enabled

This read-only register shows the status of the S/PDIF auxiliary outputs.

S/PDIF Loss-of-Lock Behavior Register (Address 0xE0CC)

Table 63. Bit Descriptions of Register 0xE0CC

Bit Position	Description	Default
[15:1]	Reserved	
0	S/PDIF loss-of-lock behavior 0 = S/PDIF disable on loss of lock 1 = S/PDIF ignore loss of lock	0

This register controls the behavior of the S/PDIF receiver in the event of a loss of lock to the input stream. A loss of lock can arise when there is severe noise or jitter on the S/PDIF input stream, rendering it unrecognizable to the receiver. In the default mode, such an event disables the S/PDIF receiver, causing it to stop outputting frame sync pulses. This in turn causes the target ASRC to be muted. Frame sync pulses do not resume until lock is regained.

When the register is set to 1, the S/PDIF receiver always outputs frame sync pulses, even if the integrity of the S/PDIF stream is compromised and the audio samples cannot be recovered. In such a case, the S/PDIF receiver data output remains at 0 until lock is regained.

The S/PDIF receiver is robust and can recover streams with integrity well below the standards of the AES/EBU specification. Therefore, even in cases of extreme signal degradation, this register should be used only when audio recovery is required. In general, a loss-of-lock event is much shorter than an ASRC mute or unmute ramp.

Enable S/PDIF to I²S Output Register (Address 0xE241)

Table 64. Bit Descriptions of Register 0xE241

Bit Position	Description	Default
[15:3]	Reserved	
2	Output mode 0 = I²S 1 = TDM	0
1	Group 2 enable 0 = Group 2 off 1 = Group 2 on	0
0	Group 1 enable 0 = Group 1 off 1 = Group 1 on	0

The S/PDIF receiver can be set to send the stereo audio stream and the auxiliary S/PDIF bits in I²S or TDM format on eight of the 12 MP pins. The eight outputs are divided into two groups: Group 1 converts S/PDIF to I²S (LRCLK, BCLK, and SDATA signals), and Group 2 decodes the channel status and user data bits (virtual LRCLK, user data, channel status, validity bit, and block start signal).

This MP output is controlled by setting three bits in Register 0xE241:

- Bit 0 switches Group 1 on and off.
- Bit 1 switches Group 2 on and off.
- Bit 2 switches between I²S and TDM modes.

When S/PDIF to I²S mode is active, the pins described in Table 53 are used.

When TDM mode is active, Slot 0 and Slot 4 contain the audio data, and Slot 1 contains the streamed block start, channel status, user data, and validity bits (see Table 65). The bits are streamed in real time and are synchronized to the audio data. Only the seven MSBs of Slot 1 are used, as shown in Table 65. The corresponding TDM format is shown in more detail in Figure 54.

Table 65. Function of Decoded Bits in Figure 54

Bit Position	Description
31	Block start (high for first 16 samples)
30	Channel status of right channel
29	Channel status of left channel
28	User data bit, right channel
27	User data bit, left channel
26	Validity bit, right channel
25	Validity bit, left channel
[24:0]	Not used

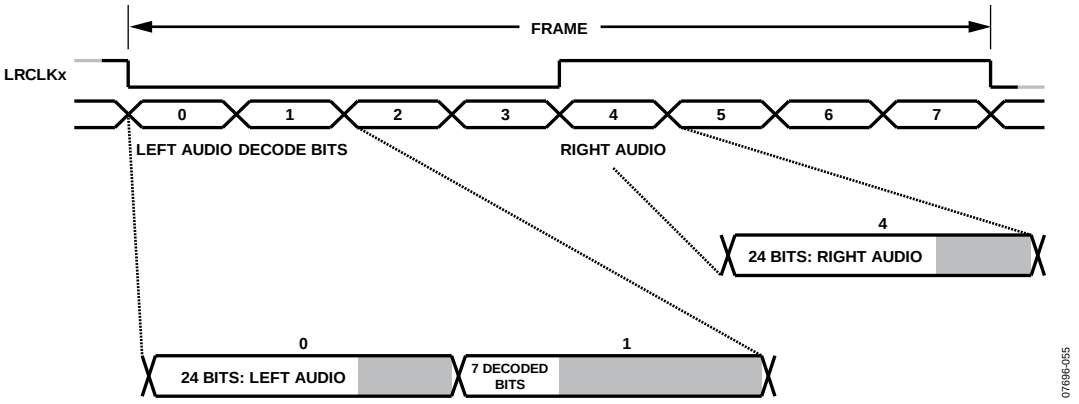


Figure 54. S/PDIF TDM Signal

MULTIPURPOSE PINS

The ADAU1442/ADAU1445/ADAU1446 each include 12 multipurpose pins that can be used either as digital general-purpose inputs/outputs (GPIOs) or as inputs to the 4-channel auxiliary ADC.

Each of the 12 multipurpose pins is controlled by a 4-bit mode. Pins can be configured as digital inputs, digital outputs, or, when applicable, as an analog input to the auxiliary ADC. A debounce circuit is included for use with digital inputs, and it has a range of selectable time constants between 0.3 µs and 40 µs.

When the inputs or outputs are driven by the control port, the value can be directly read or controlled by reading or writing the addresses listed in Table 66.

Each of these registers is four bytes long and is in 5.23 format. To write a Logic 1, the bytes written should be 0x00, 0x80, 0x00, and 0x00. To write a Logic 0, the bytes written should be 0x00, 0x00, 0x00, and 0x00.

When the outputs are driven by the core, they are represented as MP outputs in the SigmaStudio programming tool and are driven directly from the DSP program in 5.23 format.

In addition, there are 12 multipurpose pin value registers that allow the input/output data to be written to or read directly from the control port. The corresponding addresses are listed in Table 68. Each value register contains four bytes and can only store one of two values: logic high or logic low. Logic high is stored as 0x00, 0x80, 0x00, 0x00. Logic low is stored as 0x00, 0x00, 0x00, 0x00. The value of the auxiliary ADC is not stored in these registers. The value of these registers can only be one of two values: 0x00 0x00 0x00 0x00 (digital zero) or 0x00 0x80 0x00 0x00 (digital one). More information about the multipurpose pins can be found in the AN-951 Application Note, *Using Hardware Controls with SigmaDSP GPIO Pins*.

MULTIPURPOSE PINS MODES AND SETTINGS

Multipurpose Pin Control Registers (Address 0xE204 to Address 0xE20F)

Table 66. Addresses of Multipurpose Pin Control Registers

Address		
Decimal	**Hex**	**Register**
57860	E204	Multipurpose pin control, MP0
57861	E205	Multipurpose pin control, MP1
57862	E206	Multipurpose pin control, MP2
57863	E207	Multipurpose pin control, MP3
57864	E208	Multipurpose pin control, MP4
57865	E209	Multipurpose pin control, MP5
57866	E20A	Multipurpose pin control, MP6
57867	E20B	Multipurpose pin control, MP7
57868	E20C	Multipurpose pin control, MP8
57869	E20D	Multipurpose pin control, MP9
57870	E20E	Multipurpose pin control, MP10
57871	E20F	Multipurpose pin control, MP11

Table 67. Bit Settings of Multipurpose Pin Control Registers

Bit Position	Description	Default
[15:4]	Reserved	
[3:0]	MP pin mode 0000 = input without a debounce 0001 = input with a debounce of 0.3 ms 0010 = input with a debounce of 0.6 ms 0011 = input with a debounce of 0.9 ms 0100 = input with a debounce of 5 ms 0101 = input with a debounce of 10 ms 0110 = input with a debounce of 20 ms 0111 = input with a debounce of 40 ms 1000 = input driven by control port 1001 = output driven by control port with pull-up 1010 = output driven by control port without pull-up 1011 = output driven by core with pull-up 1100 = output driven by core without pull-up 1101 = input auxiliary ADC (MP0 to MP3 only) 1110 = output CRC error sticky 1111 = output watchdog error sticky	0000

Multipurpose Pin Value Registers (Address 0x129A to Address 0x12A5)

Table 68. Addresses of Multipurpose Pin Value Registers

Address		
Dec	**Hex**	**Register**
4672	0x1240	Multipurpose pin value, MP0
4673	0x1241	Multipurpose pin value, MP1
4674	0x1242	Multipurpose pin value, MP2
4675	0x1243	Multipurpose pin value, MP3
4676	0x1244	Multipurpose pin value, MP4
4677	0x1245	Multipurpose pin value, MP5
4678	0x1246	Multipurpose pin value, MP6
4679	0x1247	Multipurpose pin value, MP7
4680	0x1248	Multipurpose pin value, MP8
4681	0x1249	Multipurpose pin value, MP9
4682	0x124A	Multipurpose pin value, MP10
4683	0x124B	Multipurpose pin value, MP11

INTERFACING WITH OTHER DEVICES

When interfacing the ADAU1442/ADAU1445/ADAU1446 to other devices in the system, it may be necessary to set the drive strength of each pin.

DRIVE STRENGTH MODES AND SETTINGS

Bit Clock Pad Strength Register (Address 0xE247)

This register controls the pad drive strength of all bit clock pins configured in master mode. The default 2 mA setting should be adequate for most applications. The 6 mA setting should be used only when the integrity of the signal is compromised.

Table 71. Bit Descriptions of Bit Clock Pad Strength Register

Bit Position	Description	Default
[15:12]	Reserved	
11	BCLK11 0 = low strength (2 mA) 1 = high strength (6 mA)	0
10	BCLK10 0 = low strength (2 mA) 1 = high strength (6 mA)	0
9	BCLK9 0 = low strength (2 mA) 1 = high strength (6 mA)	0
8	BCLK8 0 = low strength (2 mA) 1 = high strength (6 mA)	0
7	BCLK7 0 = low strength (2 mA) 1 = high strength (6 mA)	0
6	BCLK6 0 = low strength (2 mA) 1 = high strength (6 mA)	0
5	BCLK5 0 = low strength (2 mA) 1 = high strength (6 mA)	0
4	BCLK4 0 = low strength (2 mA) 1 = high strength (6 mA)	0
3	BCLK3 0 = low strength (2 mA) 1 = high strength (6 mA)	0
2	BCLK2 0 = low strength (2 mA) 1 = high strength (6 mA)	0
1	BCLK1 0 = low strength (2 mA) 1 = high strength (6 mA)	0
0	BCLK0 0 = low strength (2 mA) 1 = high strength (6 mA)	0

Address			
Decimal	Hex	Name	Read/Write Word Length
57821	E1DD	TDM Slot 58 and TDM Slot 59 (SDATA_OUT1)	16 bits (2 bytes)
57822	E1DE	TDM Slot 60 and TDM Slot 61 (SDATA_OUT1)	16 bits (2 bytes)
57823	E1DF	TDM Slot 62 and TDM Slot 63 (SDATA_OUT1)[1]	16 bits (2 bytes)

[1] Slot 31 and Slot 63 can only be used to hold the MS byte of an 8-bit channel and cannot be used in conjunction with other slots to hold more than eight bits of data.

Serial Output Flexible TDM Interface Modes Registers—Upper Slot (Address 0xE1C0 to Address 0xE1DF, Bits[15:8])

Table 79. Bit Descriptions of Serial Output Flexible TDM Interface Modes Registers—Upper Slot[1]

Bit Position	Description	Default
15	MSB position 0 = MSB first 1 = LSB first	1
[14:10]	Output channel 00000 = Output Channel 0 00001 = Output Channel 1 … 10110 = Output Channel 22 10111 = Output Channel 23 … 11111 = unused	11111
[9:8]	Byte position 00 = most significant (MS) byte 01 = middle (M) byte 10 = least significant (LS) byte 11 = unused	11

[1] Bits[15:8] control TDM Slot 1.

Serial Output Flexible TDM Interface Modes Registers—Lower Slot (Address 0xE1C0 to Address 0xE1DF, Bits[7:0])

Table 80. Bit Descriptions of Serial Output Flexible TDM Interface Modes Registers—Lower Slot[1]

Bit Position	Description	Default
7	MSB position 0 = MSB first 1 = LSB first	1
[6:2]	Output channel 00000 = Output Channel 0 00001 = Output Channel 1 … 10110 = Output Channel 22 10111 = Output Channel 23 … 11111 = unused	11111
[1:0]	Byte position 00 = most significant (MS) byte 01 = middle (M) byte 10 = least significant (LS) byte 11 = unused	11

[1] Bits[7:0] control TDM Slot 0.