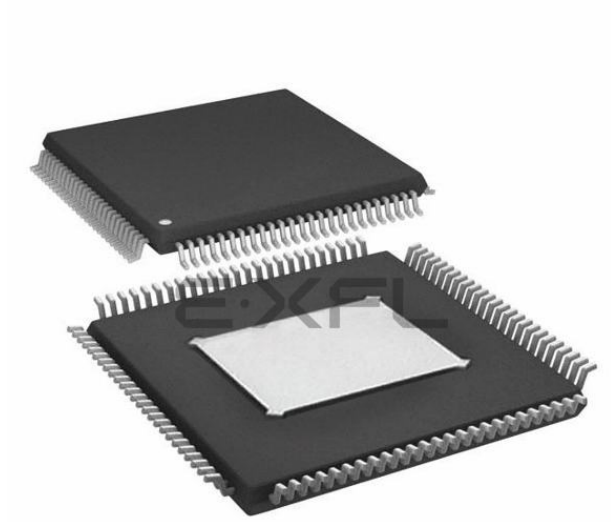

Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Sigma
Interface	I²C, SPI
Clock Rate	172MHz
Non-Volatile Memory	-
On-Chip RAM	46kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP Exposed Pad
Supplier Device Package	100-TQFP-EP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adau1445ysvz-3a

TABLE OF CONTENTS

GENERAL DESCRIPTION

The ADAU1442/ADAU1445/ADAU1446 are enhanced audio processors that allow full flexibility in routing all input and output signals. The SigmaDSP® core features full 28-bit processing (56-bit in double-precision mode), synchronous parameter loading for ensuring filter stability, and 100% code efficiency with the SigmaStudio™ tools. This DSP allows system designers to compensate for the real-world limitations of speakers, amplifiers, and listening environments, resulting in a dramatic improvement of the perceived audio quality through speaker equalization, multiband compression, limiting, and third-party branded algorithms.

The flexible audio routing matrix (FARM) allows the user to multiplex inputs from multiple sources running at various sample rates to or from the SigmaDSP core. This drastically reduces the complexity of signal routing and clocking issues in the audio system. FARM includes up to eight stereo asynchronous sample rate converters (depending on the device model), Sony/Philips Digital Interconnect Format (S/PDIF) input and output, and serial (I^2S) and time division multiplexing (TDM) I/Os. Any of these inputs can be routed to the SigmaDSP core or to any of the asynchronous sample rate converters (ASRCs). Similarly, any one of the output signals can be taken from the SigmaDSP core or from any of the ASRC outputs. This routing scheme, which can be modified at any time via control registers, allows for maximum system flexibility.

The ADAU1442, ADAU1445, and ADAU1446 differ only in ASRC functionality and packaging. The ADAU1442/ADAU1445 contain 16 channels of ASRCs and are packaged in TQFP packages, whereas the ADAU1446 contains no ASRCs and is packaged in an LQFP. The ADAU1442 can handle nine clock domains, the ADAU1445 can handle three clock domains, and the ADAU1446 can handle one clock domain.

The ADAU1442/ADAU1445/ADAU1446 can be controlled in one of two operational modes: the settings of the chip can be loaded and dynamically updated through the SPI/I^2C® port, or the DSP can self-boot from an external EEPROM in a system with no microcontroller. There is also a bank of multipurpose (MP) pins that can be used as general-purpose digital I/Os or as inputs to the 4-channel auxiliary control ADC.

The ADAU1442/ADAU1445/ADAU1446 are supported by the SigmaStudio graphical development environment. This software includes audio processing blocks such as FIR and IIR filters, dynamics processors, mixers, low level DSP functions, and third-party algorithms for fast development of custom signal flows.

Table 1.

Device	ASRC Channels	ASRC Clock Domains	Package
ADAU1442	16	8	TQFP
ADAU1445	16	2	TQFP
ADAU1446	0	N/A	LQFP

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
I/O Sample Rate Ratio	1:8		7.75:1		
THD + N		−133	−120	dB	
CRYSTAL OSCILLATOR					
Transconductance		40		mS	
REGULATOR[2]					
DVDD Voltage	1.65	1.75	1.85	V	Maximum 500 mA load.

[1] To calculate the group delay, refer to the SRC Group Delay section.
[2] Regulator specifications are calculated using an NJT4030P transistor from On Semiconductor in the circuit.

AVDD = 3.3 V ± 10%, DVDD = 1.8 V ± 10%, PVDD = 3.3 V, IOVDD = 3.3 V ± 10%, T_A = −40°C to +105°C, master clock input = 12.288 MHz, core clock f_{CORE} = 172.032 MHz, I/O pins set to 2 mA drive setting, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG PERFORMANCE					AVDD = 3.3 V ± 10%.
Auxiliary Analog Inputs					
Resolution		10		Bits	
Full-Scale Analog Input		AVDD		V	
Integral Nonlinearity (INL)	−2.3		+2.3	LSB	
Differential Nonlinearity (DNL)	−2.0		+2.0	LSB	
Gain Error	−2.0		+2.0	LSB	
Input Impedance		200		kΩ	
Sample Rate		f_{CORE}/896		kHz	4:1 multiplexed input, each channel at f_{CORE}/3584. For f_{CORE} = 172.032 MHz, each channel is sampled at 48 kHz.
DIGITAL I/O					
Input Voltage, High (V_{IH})	0.7 × IOVDD			V	Digital input pins except SPDIFI.[1]
Input Voltage, Low (V_{IL})			0.3 × IOVDD	V	Digital input pins except SPDIFI.[1]
Input Leakage, High (I_{IH}) at 3.3 V	−2		+2	µA	Digital input pins except MCLK and SPDIFI.
	−2		+8	µA	MCLK.
	60		140	µA	SPDIFI.
Input Leakage, Low (I_{IL}) at 0 V	−85		−10	µA	All other pins.
	−2		+2	µA	CLKMODEx, RSVD, PLLx, RESET.
	−8		+2	µA	MCLK.
	−140		−60	µA	SPDIFI.
High Level Output Voltage (V_{OH})	0.85 × IOVDD			V	I_{OH} = 1 mA.
Low Level Output Voltage (V_{OL})			0.1 × IOVDD	V	I_{OL} = 1 mA.
Input Capacitance (C_I)		5		pF	Guaranteed by design.
Multipurpose Pins Output Drive		2		mA	These pins are not designed for static current draw and should not drive LEDs directly.
POWER					
Supply Voltage					
Analog Voltage (AVDD)	2.97	3.3	3.63	V	
Digital Voltage (DVDD)	1.62	1.8	1.98	V	
PLL Voltage (PVDD)	2.97	3.3	3.63	V	
IOVDD Voltage (IOVDD)	2.97	3.3	3.63	V	
Supply Current					
Analog Current (AVDD)		2		mA	

Pin No.	Mnemonic	Type[1]	Description
34	MP6	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
35	MP5	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
36	MP4	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
40	VDRIVE	A_OUT	Regulator Drive. Supplies the drive current for the 1.8 V regulator. The base of the voltage regulator's external PNP transistor is driven from VDRIVE.
41	XTALO	A_OUT	Crystal Oscillator Output. A 100 Ω damping resistor should be connected between this pin and the crystal. This output should not be used to directly drive a clock to another IC; the CLKOUT pin exists for this purpose. If the crystal oscillator is not used, the XTALO pin can be left unconnected.
42	XTALI	A_IN	Crystal Oscillator Input. This pin provides the master clock for the ADAU1442/ADAU1445/ADAU1446. If the ADAU1442/ADAU1445/ADAU1446 generate the master clock in the system, this pin should be connected to the crystal oscillator circuit. If the ADAU1442/ADAU1445/ADAU1446 are slaves to an external master clock, this pin should be connected to the master clock signal generated by another IC.
43	PLL_FILT	A_OUT	Phase-Locked Loop Filter. Two capacitors and a resistor must be connected to this pin as shown in Figure 11.
44	PVDD	PWR	Phase-Locked Loop Supply. Provides the 3.3 V power supply for the PLL. This should be decoupled to PGND with a100 nF capacitor.
45	PGND	PWR	Phase-Locked Loop Ground. Ground for the PLL supply. The AGND, DGND, and PGND pins can be tied directly together in a common ground plane. PGND should be decoupled to PVDD with a 100 nF capacitor.
46	SPDIFI	D_IN	S/PDIF Input. Accepts digital audio data in the S/PDIF format. When not used, this pin can be left disconnected.
47	SPDIFO	D_OUT	S/PDIF Output. Outputs digital audio data in the S/PDIF format. When not used, this pin can be left disconnected.
48	AVDD	PWR	Analog Supply. 3.3 V analog supply for the auxiliary ADC. This pin should be decoupled to AGND with a 100 nF capacitor.
49	AGND	PWR	Analog Ground. Ground for the analog supply. This pin should be decoupled to AVDD with a 100 nF capacitor.
53	CLKOUT	D_OUT	Master Clock Output. Used to output a master clock to other ICs in the system. Set using the CLKMODEx pins. When not used, this pin can be left disconnected.
54	$\overline{\text{RESET}}$	D_IN	Reset. Active-low reset input. Reset is triggered on a high-to-low edge and exited on a low-to-high edge. For detailed information about initialization, see the Power-Up Sequence section. A reset event sets all RAMs and registers to their default values.
55	MP3/ADC3	D_IO, A_IN	Multipurpose, General-Purpose Input or Output/Auxiliary ADC Input 3. When not used, this pin can be left disconnected.
56	MP2/ADC2	D_IO, A_IN	Multipurpose, General-Purpose Input or Output/Auxiliary ADC Input 2. When not used, this pin can be left disconnected.
57	MP1/ADC1	D_IO, A_IN	Multipurpose, General-Purpose Input or Output/Auxiliary ADC Input 1. When not used, this pin can be left disconnected.
58	MP0/ADC0	D_IO, A_IN	Multipurpose, General-Purpose IO/Auxiliary ADC Input 0. When not used, this pin can be left disconnected.
59	PLL1	D_IN	Phase-Locked Loop Mode Select Pin 1.
60	PLL0	D_IN	Phase-Locked Loop Mode Select Pin 0.
61	SDATA_OUT8	D_OUT	Serial Data Port 0 Output. When not used, this pin can be left disconnected.
64	BCLK11	D_IO	Bit Clock, Output Clock Domain 11. This pin is bidirectional, with the direction depending on whether the Output Clock Domain 11 is set up as a master or slave. When not used, this pin can be left disconnected.
65	LRCLK11	D_IO	Frame Clock, Output Clock Domain 11. This pin is bidirectional, with the direction depending on whether the Output Clock Domain 11 is set up as a master or slave. When not used, this pin can be left disconnected.

Table 9. PLL Modes

DSP Core Rate[1]	Input to MCLK (XTALI Pin)	PLL2	PLL1	PLL0	PLL Divider[2]	Core Clock Multiplier	Core Clock (f_{CORE})	Instructions per Sample
Normal	64 × $f_{S,NORMAL}$	0	0	0	1	56	3584 × $f_{S,NORMAL}$	3584
	128 × $f_{S,NORMAL}$	0	0	1	2	56	3584 × $f_{S,NORMAL}$	3584
	256 × $f_{S,NORMAL}$	0	1	0	4	56	3584 × $f_{S,NORMAL}$	3584
	384 × $f_{S,NORMAL}$	0	1	1	6	56	3584 × $f_{S,NORMAL}$	3584
	512 × $f_{S,NORMAL}$	1	0	0	8	56	3584 × $f_{S,NORMAL}$	3584
Dual	32 × $f_{S,DUAL}$	0	0	0	1	56	1792 × $f_{S,DUAL}$	1792
	64 × $f_{S,DUAL}$	0	0	1	2	56	1792 × $f_{S,DUAL}$	1792
	128 × $f_{S,DUAL}$	0	1	0	4	56	1792 × $f_{S,DUAL}$	1792
	192 × $f_{S,DUAL}$	0	1	1	6	56	1792 × $f_{S,DUAL}$	1792
	256 × $f_{S,DUAL}$	1	0	0	8	56	1792 × $f_{S,DUAL}$	1792
Quad	16 × $f_{S,QUAD}$	0	0	0	1	56	896 × $f_{S,QUAD}$	896
	32 × $f_{S,QUAD}$	0	0	1	2	56	896 × $f_{S,QUAD}$	896
	64 × $f_{S,QUAD}$	0	1	0	4	56	896 × $f_{S,QUAD}$	896
	96 × $f_{S,QUAD}$	0	1	1	6	56	896 × $f_{S,QUAD}$	896
	128 × $f_{S,QUAD}$	1	0	0	8	56	896 × $f_{S,QUAD}$	896

[1] If the normal DSP core rate ($f_{S,NORMAL}$) is 44.1 kHz, the dual DSP core rate ($f_{S,DUAL}$) is 88.2 kHz, and the quad DSP core rate ($f_{S,QUAD}$) is 176.4 kHz. Likewise, if $f_{S,NORMAL}$ is 48 kHz, then $f_{S,DUAL}$ is 96 kHz and $f_{S,QUAD}$ is 192 kHz.
[2] The PLL divider is set by the PLLx pins.

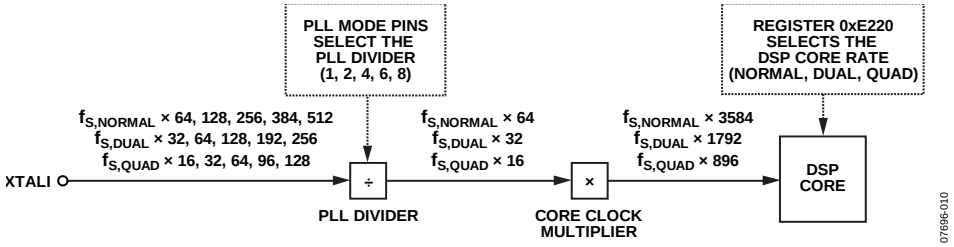

Figure 10. Master Clock Signal Flow

VOLTAGE REGULATOR

The digital supply voltage of the ADAU1442/ADAU1445/ADAU1446 must be set to 1.8 V. The chip includes an on-board voltage regulator that allows the device to be used in systems where a 1.8 V supply is not available but a 3.3 V supply is. The only external components needed for this are a PNP transistor and one resistor. Only one pin, VDRIVE, is necessary to support the regulator.

The recommended design for the voltage regulator is shown in Figure 12. The 10 µF and 100 nF capacitors shown in this schematic are recommended for bypassing but are not necessary for operation. Each DVDD pin should have its own 100 nF bypass capacitor, but only one bulk capacitor (10 µF) is needed for all pins. In this design, 3.3 V is the main system voltage; 1.8 V is generated at the collector of the transistor, which is connected to the DVDD pins. VDRIVE is connected to the base of the PNP transistor. If the regulator is not used in the design, VDRIVE can be tied to ground.

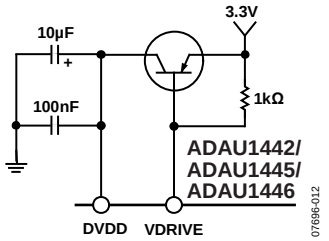

Figure 12. Voltage Regulator Design

Two specifications must be considered when choosing a regulator transistor: the current amplification factor (h_{FE} or beta) should be at least 200, and the collector must be able to dissipate the heat generated when regulating from 3.3 V to 1.8 V. The maximum digital current draw of the ADAU1442 and ADAU1445, which use ASRCs, is 310 mA. The equation to determine the minimum power dissipation specifications of the transistor is as follows:

$$(3.3\text{ V} - 1.8\text{ V}) \times 310\text{ mA} = 465\text{ mW}$$

Many transistors fit these specifications. Analog Devices recommends the NJT4030P from On Semiconductor. For projects with stringent size constraints, an FMMT734 from Zetex can be used.

The ADAU1446, which does not contain ASRCs, has a lower maximum digital current draw of approximately 235 mA. The maximum power dissipation of the transistor in this case should be around 355 mW.

SRC GROUP DELAY

The group delay of the sample rate converter is dependent on the input and output sampling frequencies as described in the following equations.

For $f_{S\_OUT} > f_{S\_IN}$,

$$GDS = \frac{16}{f_{S\_IN}} + \frac{32}{f_{S\_IN}}$$

For $f_{S\_OUT} < f_{S\_IN}$,

$$GDS = \frac{16}{f_{S\_IN}} + \left(\frac{32}{f_{S\_IN}}\right) \times \left(\frac{f_{S\_IN}}{f_{S\_OUT}}\right)$$

where *GDS* is the group delay in seconds.

address responds by pulling the data line low during the ninth clock pulse. This ninth bit is known as an acknowledge bit. All other devices withdraw from the bus at this point and return to the idle condition. The R/$\overline{W}$ bit determines the direction of the data. A Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. A Logic 1 on the LSB of the first byte means that the master reads information from the peripheral. A data transfer takes place until a stop condition is encountered. A stop condition occurs when SDA transitions from low to high while SCL is held high. Figure 13 shows the timing of an I²C write.

Burst mode addressing, where the subaddresses are automatically incremented at word boundaries, can be used for writing large amounts of data to contiguous memory locations. This increment happens automatically, unless a stop condition is encountered after a single-word write. The registers and RAMs in the ADAU1445/ADAU1446 range in width from one to five bytes; therefore, the auto-increment feature knows the mapping between subaddresses and the word length of the destination register (or memory location). A data transfer is always terminated by a stop condition.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCL high period, the user should only issue one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADAU1442/ADAU1445/ADAU1446 do not issue an acknowledge and return to the idle condition. If the user exceeds the highest subaddress while in auto-increment mode, one of two actions is taken. In read mode, the ADAU1442/ADAU1445/ADAU1446 output the highest subaddress register contents until the master device issues a no acknowledge, indicating the end of a read. A no-acknowledge condition is where the SDA line is not pulled low on the ninth clock pulse on SCL. If the highest subaddress location is reached while in write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the ADAU1442/ADAU1445/ADAU1446, and the part returns to the idle condition.

I²C Read and Write Operations

Figure 15 shows the sequence of a single-word write operation. Every ninth clock, the ADAU1442/ADAU1445/ADAU1446 issue an acknowledge by pulling SDA low.

Figure 16 shows the sequence of a burst mode write operation. This figure shows an example in which the target destination registers are two bytes. The ADAU1442/ADAU1445/ADAU1446 know to increment the subaddress register every two bytes because the requested subaddress corresponds to a register or memory area with a 2-byte word length.

The sequence of a single-word read operation is shown in Figure 17. Note that, even though this is a read operation, the first R/$\overline{W}$ bit is a 0, indicating a write operation. This is because the subaddress must be written to set up the internal address. After the ADAU1442/ADAU1445/ADAU1446 acknowledge the receipt of the subaddress, the master must issue a repeated start command followed by the chip address byte with the R/$\overline{W}$ set to 1, indicating a read operation. This causes the SDA pin of the ADAU1442/ADAU1445/ADAU1446 to switch directions and begin driving data back to the master. The master then responds every ninth pulse with an acknowledge pulse to the ADAU1442/ADAU1445/ADAU1446.

Figure 18 shows the sequence of a burst mode read operation. This figure shows an example in which the target read registers are two bytes. The ADAU1442/ADAU1445/ADAU1446 increment the subaddress every two bytes because the requested subaddress corresponds to a register or memory area with word lengths of two bytes. Other address ranges can have a variety of word lengths, ranging from one to five bytes; the ADAU1442/ADAU1445/ADAU1446 always decode the subaddress and set the auto-increment circuit so that the address increments after the appropriate number of bytes.

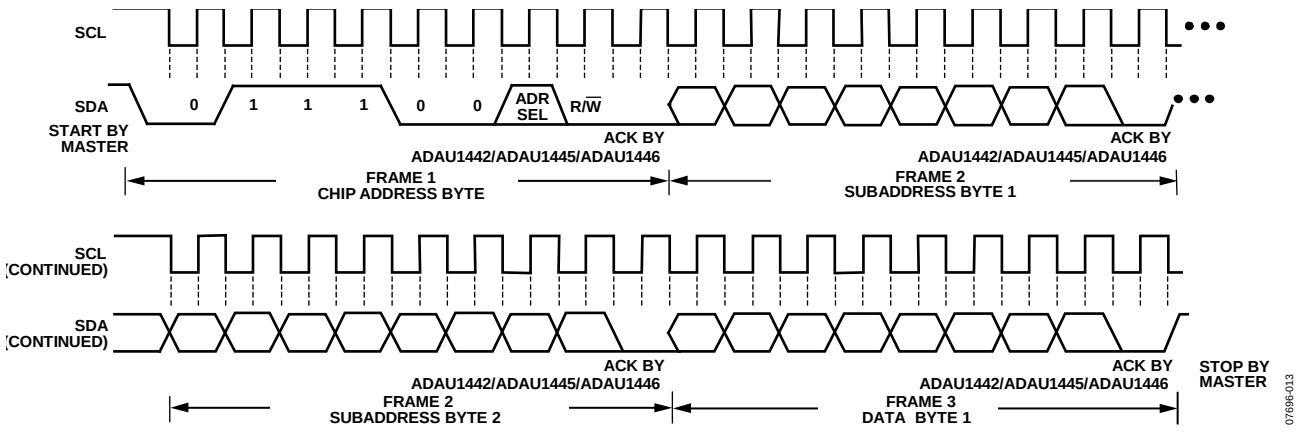

Figure 13. I²C Write Clocking

SERIAL DATA INPUT/OUTPUT

The flexible serial data input and output ports of the ADAU1442/ADAU1445/ADAU1446 can be set to accept or transmit data in a 2-channel (usually I²S format), packed TDM4, or standard 4-, 8-, or 16-channel TDM stream. Data is processed in twos complement, MSB-first format. The left-channel data field always precedes the right-channel data field in 2-channel streams. In the TDMn modes (where n represents the total number of channels in the stream), Slot 0 to Slot (n/2) − 1 fall in the first half of the audio frame, and Slot n/2 to Slot n − 1 are in the second half of the frame. TDM mode allows fewer serial data pins to be used, freeing more pins for other data streams. The serial modes are set in the serial output port modes and serial input port modes control registers.

When referring to audio data streams, the terms *TDM2* and *I²S* should be treated with care. In this document, *TDM2* refers to any 2-channel stream, whereas *I²S* refers specifically to a 2-channel, negative BCLK polarity, negative LRCLK polarity, MSB delay-by-1 stream.

The serial data clocks are fully bidirectional and do not need to be synchronous with the ADAU1442/ADAU1445/ADAU1446 master clock input. However, asynchronous data streams must be routed through an on-board asynchronous sample rate converter to be processed in the core.

The input control registers allow control of clock polarity and data input modes. All common data formats are available with flexible MSB start, bit depth (24-, 20-, or 16-bit), and TDM settings. In all modes except the right-justified modes, the serial port accepts an arbitrary number of bits up to a limit of 24. Extra bits do not cause an error, but they are truncated internally. Proper operation of the right-justified modes requires that there be exactly 64 BCLKs per audio frame (for 2-channel data). The LRCLK in TDM mode can be input to the ADAU1442/ADAU1445/ADAU1446 either as a 50/50 duty cycle clock or as a bit-wide pulse.

In TDM mode, the bit clock supplied by the ADAU1442/ADAU1445/ADAU1446 in master mode is limited to 25 MHz. This, in turn, limits the sampling rate at which it can supply master clocks in various TDM modes. Table 18 displays the modes in which the serial output port functions for some common audio sample rates.

The output control registers give the user control of clock polarities, clock frequencies, clock types, and data format. In all modes except the right-justified modes (MSB delayed by 8, 12, or 16), the serial port accepts an arbitrary number of bits up to a limit of 24. Extra bits do not cause an error, but are truncated internally. Proper operation of the right-justified modes requires the LSB to align with the edge of the LRCLK. The default settings of all serial port control registers correspond to 2-channel, I²S mode, and 24-bit slave mode, and these registers are set as slaves to the clock domain corresponding to their channel number.

Table 18. Serial Input and Output Port TDM Capabilities

Mode	BCLK Cycles per Frame	f_S (kHz)	BCLK Frequency (MHz)	Valid Mode
TDM2	64	44.1	2.8224	Yes
	64	48	3.072	Yes
	64	88.2	5.6448	Yes
	64	96	6.144	Yes
	64	192	12.288	Yes
TDM4	128	44.1	5.6448	Yes
	128	48	6.144	Yes
	128	88.2	11.2896	Yes
	128	96	12.288	Yes
	128	192	24.576	Yes
TDM8	256	44.1	11.2896	Yes
	256	48	12.288	Yes
	256	88.2	22.5792	Yes
	256	96	24.576	Yes
	256	192	49.152	No[1]
TDM16	512	44.1	22.5792	Yes
	512	48	24.576	Yes
	512	88.2	45.1584	No[1]
	512	96	49.152	No[1]
	512	192	98.304	No[1]

[1] The device will not work in this mode.

Connections to an external DAC are handled exclusively with the output port pins. The output LRCLKx and BCLKx pins can be set to be either master or slave, and the SDATA_OUT pins are used to output data from the SigmaDSP to the external DAC.

Table 19 shows the proper configurations for standard audio data formats, and Figure 21 presents an overview of the serial data input/output ports.

Packed TDM4 Mode

A special TDM mode is available that allows four channels to be fit into a space of 64 bit clock cycles. This mode is called packed TDM4 mode, or MOST™ mode. MOST (Media Oriented Systems Transport) is a networking standard intended for interconnecting multimedia components in automobiles and other vehicles. Many ICs intended to interface with a MOST bus use a packed TDM4 data format.

For this mode to be used, the serial port must be set up with the following register settings:

- Packed TDM4 mode
- Left-justified or delay by 1
- Word length of 16 bits

See Figure 29 for a timing diagram of the packed TDM4 mode. This figure is shown with a negative BCLK polarity, a negative LRCLK polarity, and an MSB delay of 1.

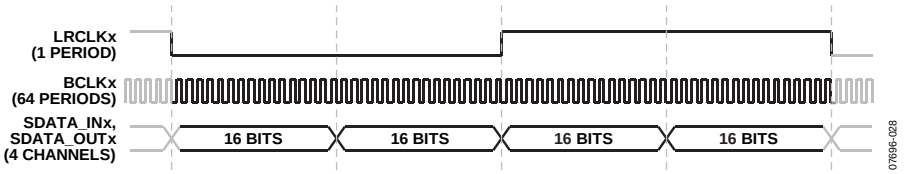

Figure 29. Packed TDM4 Mode

Routing Matrix Functionality

Serial Input Ports

The far left side of Figure 36 represents the audio input pins to the ADAU1442/ADAU1445/ADAU1446, namely SDATA_IN0 to SDATA_IN8 and SPDIFI. The serial audio data signals can be represented in any standard mode, including time division multiplexing (TDM) modes, as detailed in the Serial Data Input/Output section. After passing through the serial input ports, the signals undergo an automatic input channel assignment procedure.

Automatic Input Channel Assignment

The serial input ports can handle up to nine input signals. A standard data format is I²S (inter-IC sound), which contains both the left and right channels of a stereo pair. However, some of the signals input to the serial input ports may contain data, in TDM format, for more than two channels. The input to the FARM allows for 24 channels, or 12 stereo pairs. Therefore, a method is required to decompose nine signals (containing two or more channels) into 12 stereo audio channel pairs. This is accomplished by the automatic input channel assignment block. In sequential order, each input signal is appropriated by a number of input channels that corresponds to its channel content.

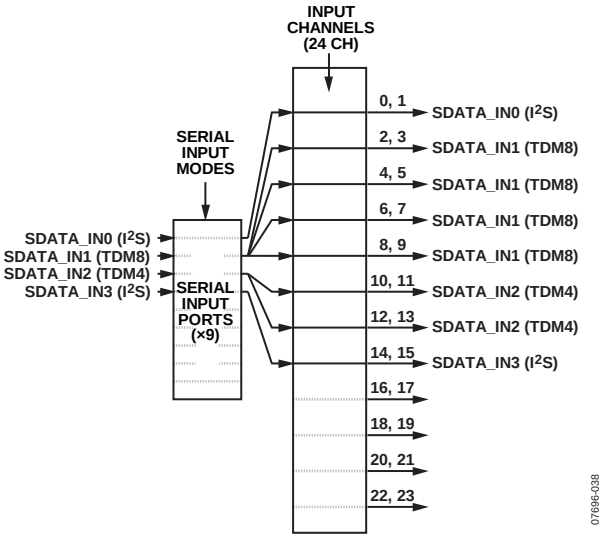

Figure 37. Automatic Input Channel Assignment Example

In the example shown in Figure 37, there are four input signals to the serial input ports: SDATA_IN0 (I²S), SDATA_IN1 (TDM8), SDATA_IN2 (TDM4), and SDATA_IN3 (I²S). SDATA_IN0, containing two channels (I²S), is routed to Input Channel 0 and Input Channel 1. SDATA_IN1, containing eight channels (TDM8), is routed sequentially to the 2, 3, 4, 5, 6, 7, 8, and 9 input channels. SDATA_IN2, containing two stereo pairs (TDM4), is routed sequentially to the 10, 11, 12, and 13 input channels. Finally, SDATA_IN3, containing two channels (I²S), is routed to Input Channel 14 and Input Channel 15.

In this way, the input channels are filled automatically according to the inputs and modes seen on the serial input ports.

When a pin is skipped, it is assigned to input channels regardless, so care must be taken to select the proper input channels within the DSP. Automatic channel assignment is entirely based on the mode settings for a particular serial port; therefore, a port set to a 2-channel mode is assigned to two sequential input channels, and a port set to a 4-channel mode is assigned to four sequential input channels, and so on. Figure 38 shows an example in which several pins are disconnected in hardware and the corresponding empty input channels are automatically assigned.

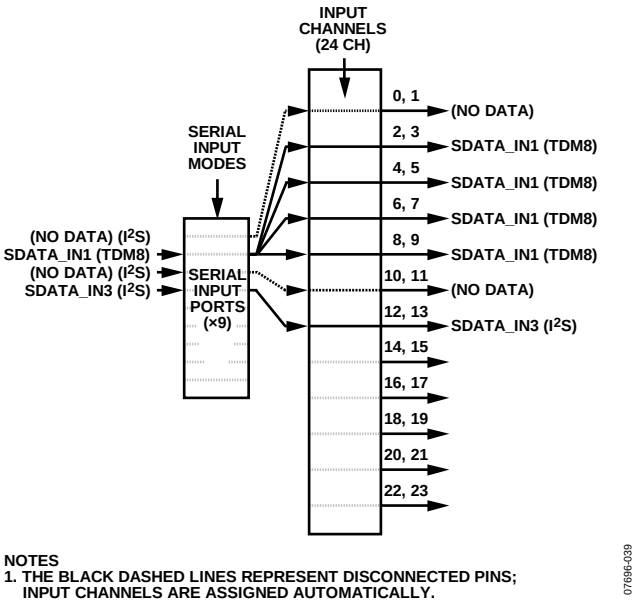

Figure 38. Automatic Input Channel Assignment Example with Skipped Pins

Stereo ASRC Routing Overview

Within the ADAU1442 and ADAU1445, signals are required to be synchronous to the master clock only when they are within the DSP core itself. At all other times, signals can be asynchronous to one another and the core. This is illustrated in Figure 42. Because the ADAU1446 has no ASRCs, all audio signals must be synchronous at all times.

The stereo ASRCs allow asynchronous signals to be converted for processing in the DSP.

The input to an ASRC can come from one of 21 sources: the 12 input channel pairs, the S/PDIF Rx pair, or the eight DSP-to-ASRC pairs. This allows the ASRCs to be placed both before and after the DSP. Figure 43 and Figure 44 show examples of how the ASRCs can be used both before and after the DSP.

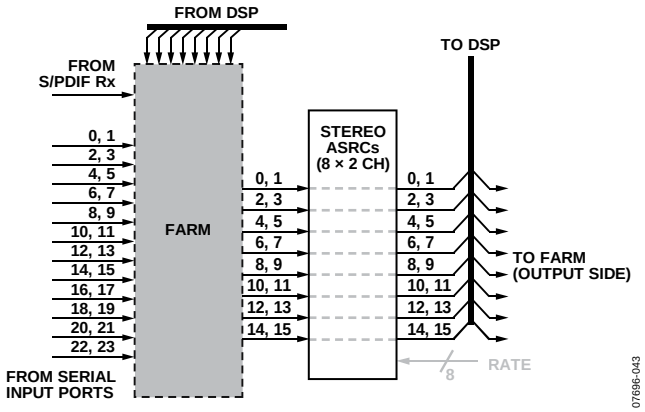

Figure 41. Stereo ASRC Routing

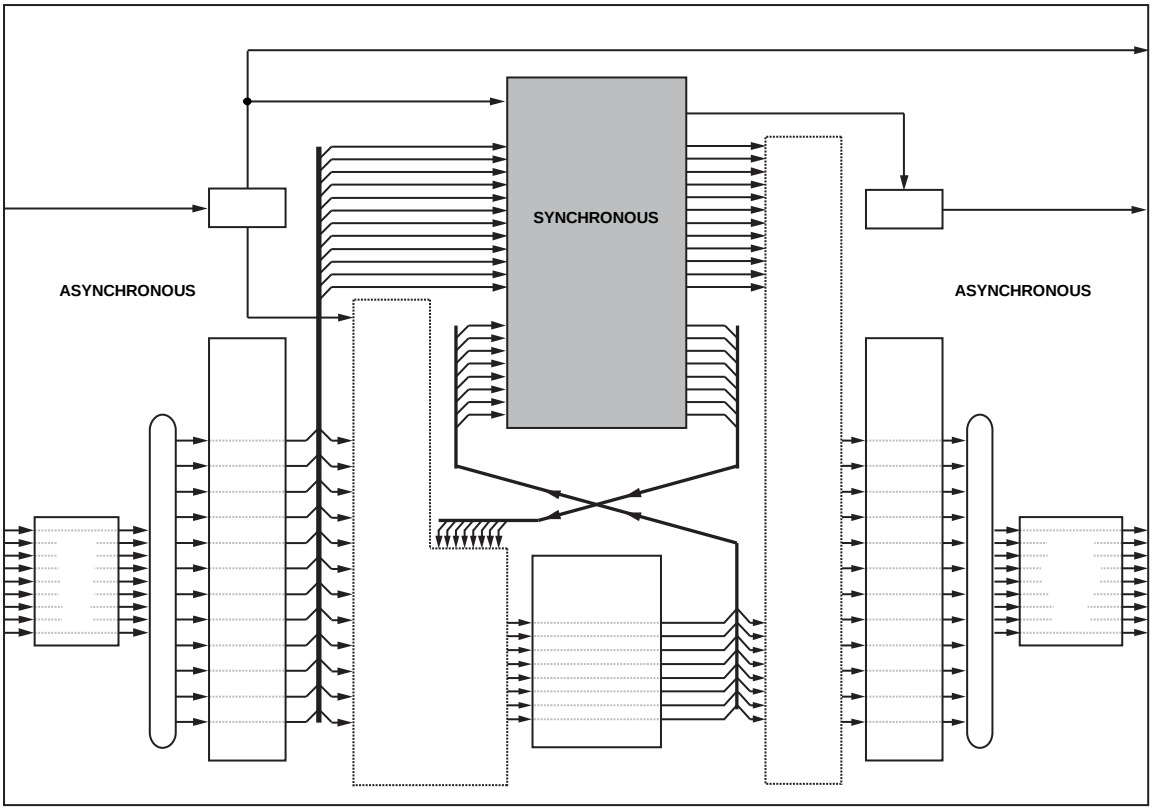

Figure 42. Synchronous and Asynchronous Zones of the ADAU1442 and ADAU1445

Flexible Audio Routing Matrix—Output Side

Much like the input side, the output side of the flexible audio routing matrix takes several stereo pairs, which can be asynchronous, and connects them to the 12 stereo pairs that are output from the chip on the serial output ports. The connections must again be one-to-one, meaning that from the 20 possible stereo pairs entering the FARM output side, only 12 can be selected to output from the chip. This process is represented in Figure 47 as a large gray box.

The outputs from the ASRCs are automatically connected to both the DSP and to the FARM output sides.

Note that on the output side, unlike on the input side, the DSP outputs are not hardwired to the output channels.

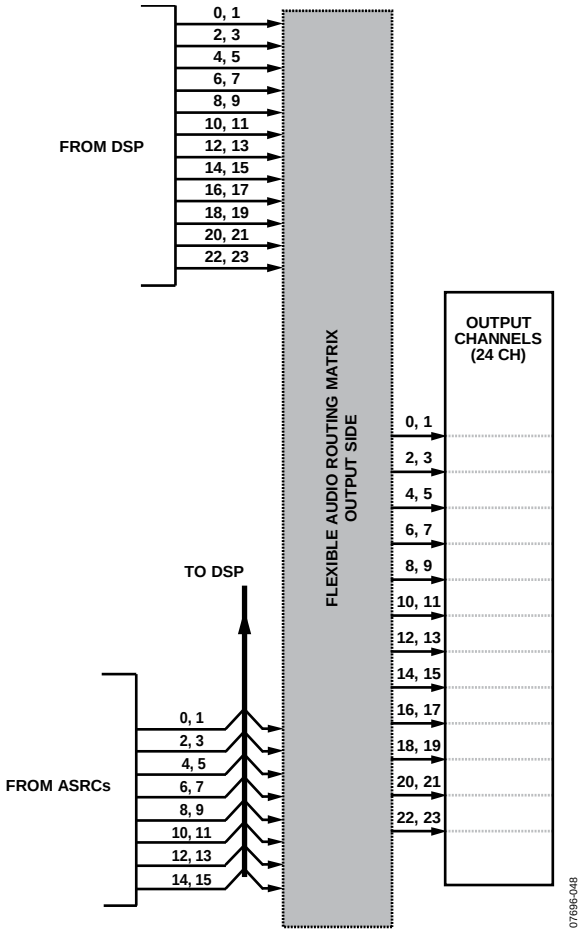

Figure 47. Flexible Audio Routing Matrix—Output Side

Automatic Output Channel Assignment

From the 24 output channels, there are nine serial output ports available to output the data. By selecting different output modes, the user can output the data in the desired format. After the modes are selected for each serial output port, the output channels are automatically assigned to sequentially corresponding serial output ports according to the number of channels desired in the stream. For clarification, see Figure 48.

In this example, 14 output channels must be output on three serial output ports. To accomplish this, serial output modes must be chosen to fit the desired system. In this case, SDATA_OUT0 is set to TDM8 mode, SDATA_OUT1 is set to I²S mode, and SDATA_OUT2 is set to TDM4 mode. Using this information, the automatic output channel assignment algorithm routes Output Channels[7:0] to SDATA_OUT0, Output Channels[9:8] to SDATA_OUT1, and Output Channels[13:10] to SDATA_OUT2. Note that output channels must be assigned sequentially, and no pair can be skipped. If an output channel is left empty (that is, no data is routed to it from the ASRCs or DSP), it is still assigned to a serial output port.

ASRC Input Data Selector Bits (Bits[5:0])

As shown in Figure 49, the gray box representing the input side of the flexible audio routing matrix can be thought of as a multiplexer. Any input to the box can make a one-to-one connection to any output from the box. The inputs are the Serial Input Pairs[11:0] and the DSP-to-ASRC Pairs[7:0]. The outputs from FARM are the Stereo ASRC[7:0] inputs.

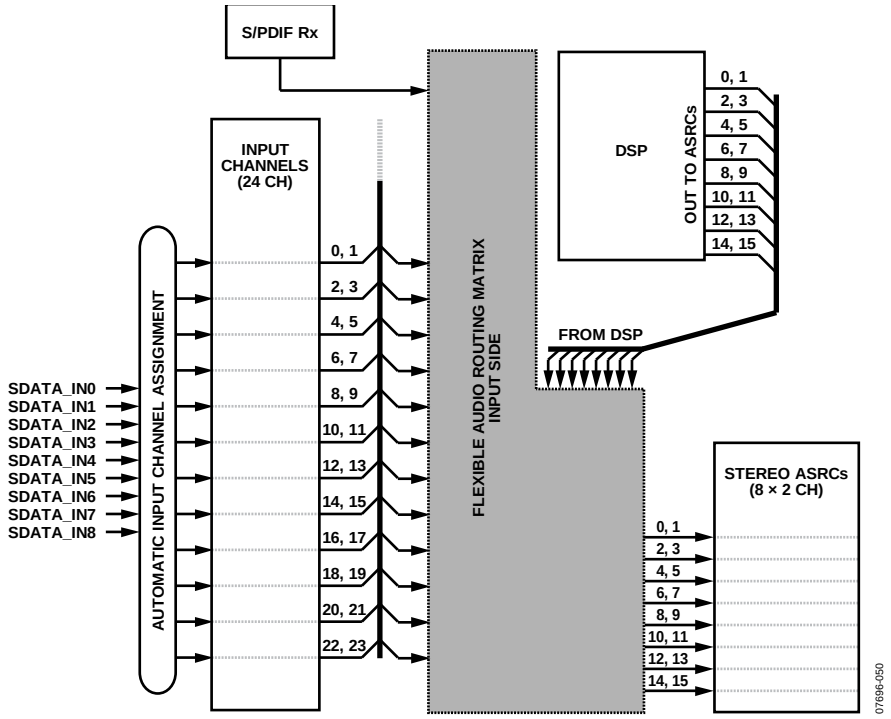

Figure 49. ASRC Input Select

Serial Output Data Selector Bits (Bits[5:0])

These bits select where each of the 12 stereo serial output channels comes from. The channels can come either from one of the 12 DSP core stereo outputs or from one of the eight ASRC stereo outputs.

In the case of the ADAU1446, setting the serial output data selector bits to a value corresponding to an ASRC output pair yields no data.

As shown in Figure 50, the stereo output pairs can come from any of the DSP serial or ASRC outputs.

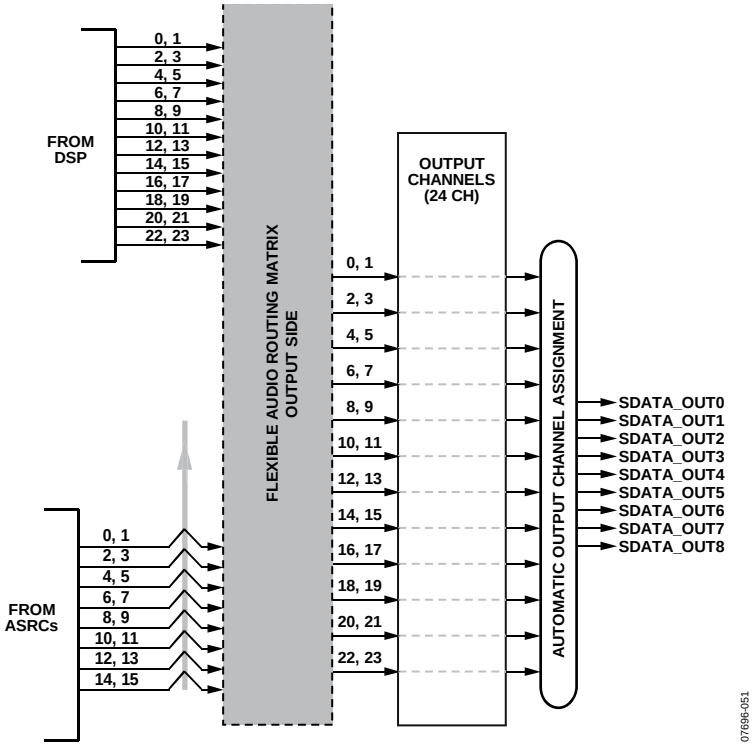

Figure 50. Serial Output Select Pair

Numeric Formats

DSP systems commonly use a standard numeric format. Fractional number systems are specified by an A.B format, where A is the number of bits to the left of the decimal point and B is the number of bits to the right of the decimal point.

The ADAU1442/ADAU1445/ADAU1446 use the same numeric format for both the parameter and data values. The format is as shown in the Numerical Format: 5.23 section.

Numerical Format: 5.23

Linear range: –16.0 to (+16.0 – 1 LSB)

Examples:
1000 0000 0000 0000 0000 0000 0000 = –16.0
1110 0000 0000 0000 0000 0000 0000 = –4.0
1111 1000 0000 0000 0000 0000 0000 = –1.0
1111 1110 0000 0000 0000 0000 0000 = –0.25

1111 1111 0011 0011 0011 0011 0011 = –0.1
1111 1111 1111 1111 1111 1111 1111 = (1 LSB below 0.0)
0000 0000 0000 0000 0000 0000 0000 = 0.0

0000 0000 1100 1100 1100 1100 1101 = 0.1
0000 0010 0000 0000 0000 0000 0000 = 0.25
0000 1000 0000 0000 0000 0000 0000 = 1.0
0010 0000 0000 0000 0000 0000 0000 = 4.0
0111 1111 1111 1111 1111 1111 1111 = (16.0 – 1 LSB).

The serial port accepts up to 24 bits of input and is sign-extended to the full 28 bits of the DSP core. This allows internal gains of up to 24 dB without encountering internal clipping.

A digital clipper circuit is used within the DSP core before outputting to the serial port outputs, ASRCs, and S/PDIF transmitter (see Figure 52). This clips the top four bits of the signal to produce a 24-bit output with a range of 1.0 (minus 1 LSB) to –1.0. Figure 52 shows the maximum signal levels at each point in the data flow in both binary and decibel levels.

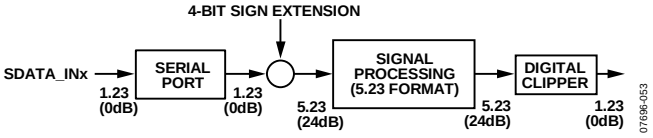

Figure 52. Numeric Precision and Clipping Structure (TBD)

Programming

On power-up, the ADAU1442/ADAU1445/ADAU1446 have no default program loaded. There are 3584 instruction cycles per audio sample, resulting in an internal clock rate of 172.032 MHz when $f_{S,NORMAL}$ is 48 kHz. The DSP runs in a stream-oriented manner, meaning that all 3584 instructions are executed each sample period. The ADAU1442/ADAU1445/ADAU1446 can also be set up to accept dual- or quad-speed inputs by reducing the number of instructions per sample. These modes can be set in the core control register.

The ADAU1442/ADAU1445/ADAU1446 can be programmed easily using SigmaStudio, an entirely graphical tool provided by Analog Devices. No knowledge of writing line-level DSP code is required, and the large library of predesigned algorithms should drastically reduce development time. More information on SigmaStudio can be found at the Analog Devices website.

Program Counter

The execution of instructions in the core is governed by a program counter, which sequentially steps through the addresses of the program RAM. The program counter starts every time a new audio frame is clocked into the core. SigmaStudio inserts a jump-to-start command at the end of every program. The program counter increments sequentially until reaching this command, and then jumps to the program start address (Program RAM Address 0x2010) and waits for the next audio frame to clock into the core.

Branching and Looping

Some cells in SigmaStudio can optionally modify the program counter to implement simple branching and looping structures. However, care must be taken that the program counter returns to its starting address before a new frame is clocked. If the new frame starts before the counter has returned to start, the audio output is corrupted, and a reset is necessary.

The software compiler in SigmaStudio calculates the maximum possible program cycles for a given project and generates an error when a user exceeds the allowable limit.

DSP CORE MODES AND SETTINGS

Core Run Register (Address 0xE228)

Table 41. Descriptions of Register 0xE228

Bit Position	Description	Default
[15:1]	Reserved	
0	Core run bit	0

This single-bit register initiates the run signal to start the core. This should be the very last register that is set when the system is initialized.

Before the core is halted, set the DSP core rate select register (0xE220) to 0x001C. This disables the start pulse to the core.

Before the care is started, set the DSP Core Rate Select register (0xE220) to the desired value. This enables the start pulse to the core. Table 12 contains a list of valid settings.

If the core is halted (that is, if Bit 0 of Register 0xE228 is set to 0) during operation, the serial outputs jump immediately to 0. This ensures that no dc level is left on the serial outputs and helps prevent speaker damage in the system. It also allows the system to mute and unmute all audio channels while minimizing pops and clicks on the outputs.

The core run bit can be used to implement a system mute functionality, as opposed to muting all of the individual channels in software. However, this approach instantaneously mutes the outputs, potentially causing clicks or pops on the output. If a click- and pop-free mute is required, software slew mute cells should be implemented into the DSP core's signal processing flow.

Enable S/PDIF to I²S Output Register (Address 0xE241)

Table 64. Bit Descriptions of Register 0xE241

Bit Position	Description	Default
[15:3]	Reserved	
2	Output mode 0 = I²S 1 = TDM	0
1	Group 2 enable 0 = Group 2 off 1 = Group 2 on	0
0	Group 1 enable 0 = Group 1 off 1 = Group 1 on	0

The S/PDIF receiver can be set to send the stereo audio stream and the auxiliary S/PDIF bits in I²S or TDM format on eight of the 12 MP pins. The eight outputs are divided into two groups: Group 1 converts S/PDIF to I²S (LRCLK, BCLK, and SDATA signals), and Group 2 decodes the channel status and user data bits (virtual LRCLK, user data, channel status, validity bit, and block start signal).

This MP output is controlled by setting three bits in Register 0xE241:

- Bit 0 switches Group 1 on and off.
- Bit 1 switches Group 2 on and off.
- Bit 2 switches between I²S and TDM modes.

When S/PDIF to I²S mode is active, the pins described in Table 53 are used.

When TDM mode is active, Slot 0 and Slot 4 contain the audio data, and Slot 1 contains the streamed block start, channel status, user data, and validity bits (see Table 65). The bits are streamed in real time and are synchronized to the audio data. Only the seven MSBs of Slot 1 are used, as shown in Table 65. The corresponding TDM format is shown in more detail in Figure 54.

Table 65. Function of Decoded Bits in Figure 54

Bit Position	Description
31	Block start (high for first 16 samples)
30	Channel status of right channel
29	Channel status of left channel
28	User data bit, right channel
27	User data bit, left channel
26	Validity bit, right channel
25	Validity bit, left channel
[24:0]	Not used

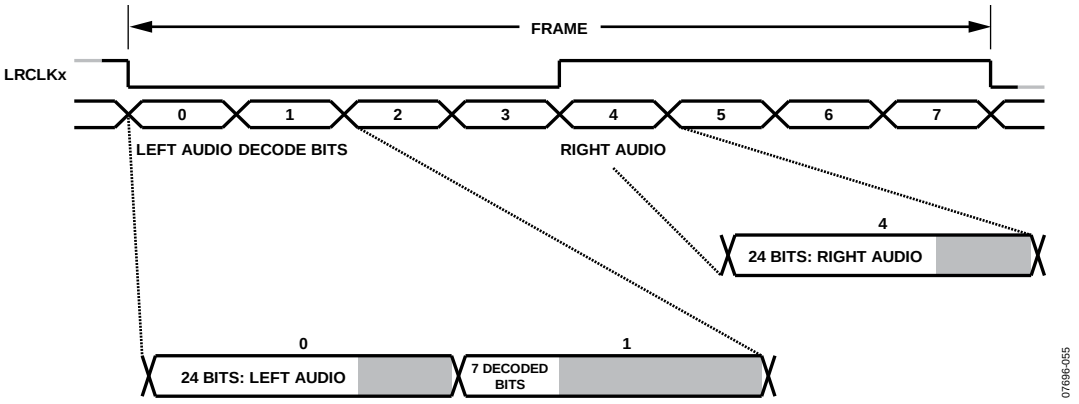

Figure 54. S/PDIF TDM Signal

MULTIPURPOSE PINS

The ADAU1442/ADAU1445/ADAU1446 each include 12 multipurpose pins that can be used either as digital general-purpose inputs/outputs (GPIOs) or as inputs to the 4-channel auxiliary ADC.

Each of the 12 multipurpose pins is controlled by a 4-bit mode. Pins can be configured as digital inputs, digital outputs, or, when applicable, as an analog input to the auxiliary ADC. A debounce circuit is included for use with digital inputs, and it has a range of selectable time constants between 0.3 µs and 40 µs.

When the inputs or outputs are driven by the control port, the value can be directly read or controlled by reading or writing the addresses listed in Table 66.

Each of these registers is four bytes long and is in 5.23 format. To write a Logic 1, the bytes written should be 0x00, 0x80, 0x00, and 0x00. To write a Logic 0, the bytes written should be 0x00, 0x00, 0x00, and 0x00.

When the outputs are driven by the core, they are represented as MP outputs in the SigmaStudio programming tool and are driven directly from the DSP program in 5.23 format.

In addition, there are 12 multipurpose pin value registers that allow the input/output data to be written to or read directly from the control port. The corresponding addresses are listed in Table 68. Each value register contains four bytes and can only store one of two values: logic high or logic low. Logic high is stored as 0x00, 0x80, 0x00, 0x00. Logic low is stored as 0x00, 0x00, 0x00, 0x00. The value of the auxiliary ADC is not stored in these registers. The value of these registers can only be one of two values: 0x00 0x00 0x00 0x00 (digital zero) or 0x00 0x80 0x00 0x00 (digital one). More information about the multipurpose pins can be found in the AN-951 Application Note, *Using Hardware Controls with SigmaDSP GPIO Pins*.

MULTIPURPOSE PINS MODES AND SETTINGS

Multipurpose Pin Control Registers (Address 0xE204 to Address 0xE20F)

Table 66. Addresses of Multipurpose Pin Control Registers

Address		
Decimal	**Hex**	**Register**
57860	E204	Multipurpose pin control, MP0
57861	E205	Multipurpose pin control, MP1
57862	E206	Multipurpose pin control, MP2
57863	E207	Multipurpose pin control, MP3
57864	E208	Multipurpose pin control, MP4
57865	E209	Multipurpose pin control, MP5
57866	E20A	Multipurpose pin control, MP6
57867	E20B	Multipurpose pin control, MP7
57868	E20C	Multipurpose pin control, MP8
57869	E20D	Multipurpose pin control, MP9
57870	E20E	Multipurpose pin control, MP10
57871	E20F	Multipurpose pin control, MP11

Table 67. Bit Settings of Multipurpose Pin Control Registers

Bit Position	Description	Default
[15:4]	Reserved	
[3:0]	MP pin mode 0000 = input without a debounce 0001 = input with a debounce of 0.3 ms 0010 = input with a debounce of 0.6 ms 0011 = input with a debounce of 0.9 ms 0100 = input with a debounce of 5 ms 0101 = input with a debounce of 10 ms 0110 = input with a debounce of 20 ms 0111 = input with a debounce of 40 ms 1000 = input driven by control port 1001 = output driven by control port with pull-up 1010 = output driven by control port without pull-up 1011 = output driven by core with pull-up 1100 = output driven by core without pull-up 1101 = input auxiliary ADC (MP0 to MP3 only) 1110 = output CRC error sticky 1111 = output watchdog error sticky	0000

Multipurpose Pin Value Registers (Address 0x129A to Address 0x12A5)

Table 68. Addresses of Multipurpose Pin Value Registers

Address		
Dec	**Hex**	**Register**
4672	0x1240	Multipurpose pin value, MP0
4673	0x1241	Multipurpose pin value, MP1
4674	0x1242	Multipurpose pin value, MP2
4675	0x1243	Multipurpose pin value, MP3
4676	0x1244	Multipurpose pin value, MP4
4677	0x1245	Multipurpose pin value, MP5
4678	0x1246	Multipurpose pin value, MP6
4679	0x1247	Multipurpose pin value, MP7
4680	0x1248	Multipurpose pin value, MP8
4681	0x1249	Multipurpose pin value, MP9
4682	0x124A	Multipurpose pin value, MP10
4683	0x124B	Multipurpose pin value, MP11

Other Pad Strength Register (Address 0xE24C)

This register controls the pad drive strength of the communications port, S/PDIF output, and master clock outputs. The default 2 mA setting should be adequate for most applications. The 6 mA setting should be used only when the integrity of the signal is compromised.

Table 75. Bit Descriptions of Other Pad Strength Register

Bit Position	Description	Default
[15:7]	Reserved	
6	SCL/CCLK 0 = low strength (2 mA) 1 = high strength (6 mA)	0
5	CLATCH 0 = low strength (2 mA) 1 = high strength (6 mA)	0
4	ADDR1/CDATA 0 = low strength (2 mA) 1 = high strength (6 mA)	0
3	ADDR0 0 = low strength (2 mA) 1 = high strength (6 mA)	0
2	SDA/COUT 0 = low strength (2 mA) 1 = high strength (6 mA)	0
1	SPDIFO 0 = low strength (2 mA) 1 = high strength (6 mA)	0
0	CLKOUT 0 = low strength (2 mA) 1 = high strength (6 mA)	0

Flexible TDM to Input Channel Modes Registers (Address 0xE180 to Address 0xE197)

Table 76. Addresses of Serial Input Flexible TDM Interface Modes Registers

Address			
Decimal	**Hex**	**Name**	**Read/Write Word Length**
57728	E180	Flexible TDM to Input Channel 0	16 bits (2 bytes)
57729	E181	Flexible TDM to Input Channel 1	16 bits (2 bytes)
57730	E182	Flexible TDM to Input Channel 2	16 bits (2 bytes)
57731	E183	Flexible TDM to Input Channel 3	16 bits (2 bytes)
57732	E184	Flexible TDM to Input Channel 4	16 bits (2 bytes)
57733	E185	Flexible TDM to Input Channel 5	16 bits (2 bytes)
57734	E186	Flexible TDM to Input Channel 6	16 bits (2 bytes)
57735	E187	Flexible TDM to Input Channel 7	16 bits (2 bytes)
57736	E188	Flexible TDM to Input Channel 8	16 bits (2 bytes)
57737	E189	Flexible TDM to Input Channel 9	16 bits (2 bytes)
57738	E18A	Flexible TDM to Input Channel 10	16 bits (2 bytes)
57739	E18B	Flexible TDM to Input Channel 11	16 bits (2 bytes)
57740	E18C	Flexible TDM to Input Channel 12	16 bits (2 bytes)
57741	E18D	Flexible TDM to Input Channel 13	16 bits (2 bytes)
57742	E18E	Flexible TDM to Input Channel 14	16 bits (2 bytes)
57743	E18F	Flexible TDM to Input Channel 15	16 bits (2 bytes)
57744	E190	Flexible TDM to Input Channel 16	16 bits (2 bytes)
57745	E191	Flexible TDM to Input Channel 17	16 bits (2 bytes)
57746	E192	Flexible TDM to Input Channel 18	16 bits (2 bytes)
57747	E193	Flexible TDM to Input Channel 19	16 bits (2 bytes)
57748	E194	Flexible TDM to Input Channel 20	16 bits (2 bytes)
57749	E195	Flexible TDM to Input Channel 21	16 bits (2 bytes)
57750	E196	Flexible TDM to Input Channel 22	16 bits (2 bytes)
57751	E197	Flexible TDM to Input Channel 23	16 bits (2 bytes)

Table 77. Bit Descriptions of Flexible TDM to Input Channel Modes Registers

Bit Position	Description	Default
[15:9]	Reserved	
8	MSB position 0 = MSB first 1 = LSB first	1
[7:6]	Number of bytes in the channel (audio bit depth) 00 = 1 byte (8-bit audio) 01 = 2 bytes (16-bit audio) 10 = 3 bytes (24-bit audio) 11 = unused	11
[5:0]	Position of the first byte on the TDM stream 000000 = TDM Slot 0 000001 = TDM Slot 1 … 111110 = TDM Slot 62 111111 = TDM Slot 63	111111

Address			
Decimal	Hex	Name	Read/Write Word Length
57821	E1DD	TDM Slot 58 and TDM Slot 59 (SDATA_OUT1)	16 bits (2 bytes)
57822	E1DE	TDM Slot 60 and TDM Slot 61 (SDATA_OUT1)	16 bits (2 bytes)
57823	E1DF	TDM Slot 62 and TDM Slot 63 (SDATA_OUT1)	16 bits (2 bytes)

Table 93. Other Modes Registers

Address			
Decimal	Hex	Name	Read/Write Word Length
57856	E200	Cyclic Redundancy Check Ideal Value 1	16 bits (2 bytes)
57857	E201	Cyclic Redundancy Check Ideal Value 2	16 bits (2 bytes)
57858	E202	Cyclic redundancy check enable	16 bits (2 bytes)
57860	E204	Multipurpose pin control, MP0	16 bits (2 bytes)
57861	E205	Multipurpose pin control, MP1	16 bits (2 bytes)
57862	E206	Multipurpose pin control, MP2	16 bits (2 bytes)
57863	E207	Multipurpose pin control, MP3	16 bits (2 bytes)
57864	E208	Multipurpose pin control, MP4	16 bits (2 bytes)
57865	E209	Multipurpose pin control, MP5	16 bits (2 bytes)
57866	E20A	Multipurpose pin control, MP6	16 bits (2 bytes)
57867	E20B	Multipurpose pin control, MP7	16 bits (2 bytes)
57868	E20C	Multipurpose pin control, MP8	16 bits (2 bytes)
57569	E20D	Multipurpose pin control, MP9	16 bits (2 bytes)
57870	E20E	Multipurpose pin control, MP10	16 bits (2 bytes)
57871	E20F	Multipurpose pin control, MP11	16 bits (2 bytes)
57872	E210	Watchdog enable	16 bits (2 bytes)
57873	E211	Watchdog Value 1	16 bits (2 bytes)
57874	E212	Watchdog Value 2	16 bits (2 bytes)
57887	E21F	Modulo data memory	16 bits (2 bytes)
57888	E220	DSP core rate select	16 bits (2 bytes)
57889	E221	Dejitter window	16 bits (2 bytes)
57892	E224	ADC filter mode	16 bits (2 bytes)
57893	E225	Cyclic redundancy check error sticky	16 bits (2 bytes)
57894	E226	Watchdog error sticky	16 bits (2 bytes)
57895	E227	CRC and watchdog mute	16 bits (2 bytes)
57896	E228	Core run	16 bits (2 bytes)
57897	E229	Program counter peak count	16 bits (2 bytes)
57920	E240	Clock pad multiplexer	16 bits (2 bytes)
57921	E241	Enable S/PDIF to I^2S output	16 bits (2 bytes)
57927	E247	Bit clock pad strength	16 bits (2 bytes)
57928	E248	Frame clock pad strength	16 bits (2 bytes)
57929	E249	Multipurpose pin pad strength	16 bits (2 bytes)
57930	E24A	Serial data output pad strength	16 bits (2 bytes)
57932	E24C	Other pad strength	16 bits (2 bytes)
57984	E280	Master clock enable switch	16 bits (2 bytes)