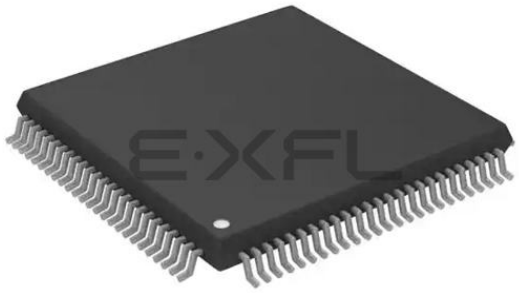

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Sigma
Interface	I²C, SPI
Clock Rate	172MHz
Non-Volatile Memory	-
On-Chip RAM	46kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adau1446ystz-3a-rl

REVISION HISTORY

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9/10—Rev. B to Rev. C

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4/09—Rev. 0 to Rev. A

Added ADAU1446 ..... Universal
Added LQFP ..... Universal
Added Minimum Digital Current (DVDD) of ADAU1446, Maximum Digital Current (DVDD) of ADAU1446, and AVDD, DVDD, PVDD During Operation of ADAU1446 Parameters, Table 1 5
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Changes to EEPROM Format Section 28
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1/09—Revision 0: Initial Version

SPECIFICATIONS

AVDD = 3.3 V, DVDD = 1.8 V, PVDD = 3.3 V, IOVDD = 3.3 V, T_A = 25°C, master clock input = 12.288 MHz, core clock f_{CORE} = 172.032 MHz, I/O pins set to 2 mA drive setting, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG PERFORMANCE					AVDD = 3.3 V ± 10%.
Auxiliary Analog Inputs					
Resolution		10		Bits	
Full-Scale Analog Input		AVDD		V	
Integral Nonlinearity (INL)	−2.3		+2.3	LSB	
Differential Nonlinearity (DNL)	−2.0		+2.0	LSB	
Gain Error	−2.0		+2.0	LSB	
Input Impedance		200		kΩ	
Sample Rate		f_{CORE}/896		kHz	4:1 multiplexed input, each channel at f_{CORE}/3584. For f_{CORE} = 172.032 MHz, each channel is sampled at 48 kHz.
POWER					
Supply Voltage					
Analog Voltage (AVDD)	2.97	3.3	3.63	V	
Digital Voltage (DVDD)	1.62	1.8	1.98	V	
PLL Voltage (PVDD)	2.97	3.3	3.63	V	
IOVDD Voltage (IOVDD)	2.97	3.3	3.63	V	
Supply Current					
Analog Current (AVDD)		2		mA	
PLL Current (PVDD)		10		mA	
I/O Current (IOVDD)		10		mA	Depends greatly on the number of active serial ports, clock pins, and characteristics of external loads.
Digital Current (DVDD)					
ADAU1442					
Typical Program		335		mA	Test program includes 16 channels I/O, 10-band EQ per channel, all ASRCs active.
Minimal Program		115		mA	Test program includes 2 channels I/O, 10-band EQ per channel.
ADAU1445					
Typical Program		270		mA	Test program includes 16 channels I/O, 10-band EQ per channel, all ASRCs active.
Minimal Program		115		mA	Test program includes 2 channels I/O, 10-band EQ per channel.
ADAU1446					
Typical Program		135		mA	Test program includes 16 channels I/O, 10-band EQ per channel, all ASRCs active.
Minimal Program		110			Test program includes 2 channels I/O, 10-band EQ per channel.
ASYNCHRONOUS SAMPLE RATE CONVERTERS[1]					
Dynamic Range		139		dB	A-weighted, 20 Hz to 20 kHz.
I/O Sample Rate	6		192	kHz	

Digital Timing Diagrams

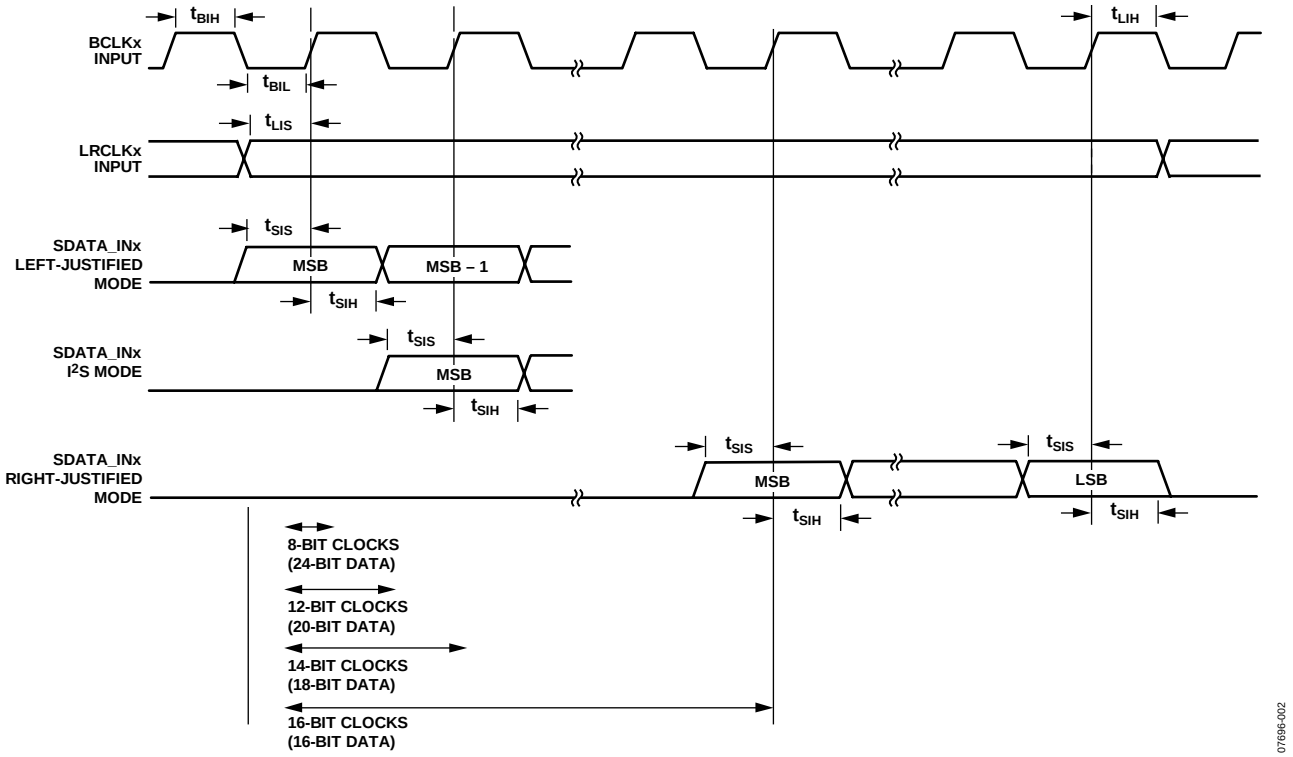

Figure 2. Serial Input Port Timing

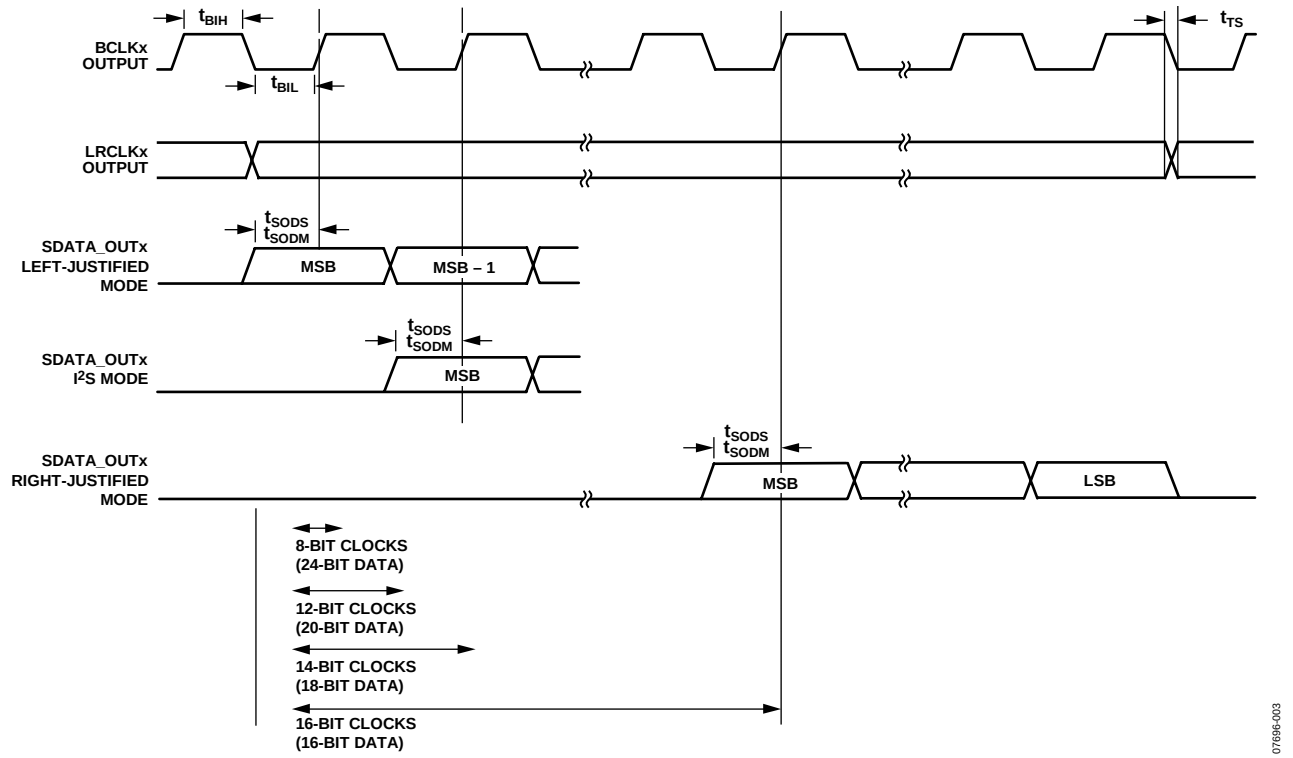

Figure 3. Serial Output Port Timing

Pin No.	Mnemonic	Type[1]	Description
6	BCLK2	D_IO	Bit Clock, Input Clock Domain 2. This pin is bidirectional, with the direction depending on whether the Input Clock Domain 2 is set up as a master or slave. When not used, this pin can be left disconnected.
7	LRCLK2	D_IO	Frame Clock, Input Clock Domain 2. This pin is bidirectional, with the direction depending on whether the Input Clock Domain 2 is set up as a master or slave. When not used, this pin can be left disconnected.
8	SDATA_IN1	D_IN	Serial Data Port 1 Input. When not used, this pin can be left disconnected.
9	BCLK1	D_IO	Bit Clock, Input Clock Domain 1. This pin is bidirectional, with the direction depending on whether the Input Clock Domain 1 is set up as a master or slave. When not used, this pin can be left disconnected.
10	LRCLK1	D_IO	Frame Clock, Input Clock Domain 1. This pin is bidirectional, with the direction depending on whether the Input Clock Domain 1 is set up as a master or slave. When not used, this pin can be left disconnected.
11	SDATA_IN0	D_IN	Serial Data Port 0 Input. When not used, this pin can be left disconnected.
12	BCLK0	D_IO	Bit Clock, Input Clock Domain 0. This pin is bidirectional, with the direction depending on whether the Input Clock Domain 0 is set up as a master or slave. When not used, this pin can be left disconnected.
15	LRCLK0	D_IO	Frame Clock, Input Clock Domain 0. This pin is bidirectional, with the direction depending on whether the Input Clock Domain 0 is set up as a master or slave. When not used, this pin can be left disconnected.
16	MP11	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
17	MP10	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
18	MP9	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
19	MP8	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
20	ADDR0	D_IN	Address 0 for I²C and SPI. In I²C mode, this pin, in combination with ADDR1, allows up to four ADAU1442/ADAU1445/ADAU1446 devices to be used on the same I²C bus. In SPI mode, setting ADDR0 either low or high allows up to two ICs to be used with a common SPI latch signal.
21	CLATCH	D_IN	SPI Latch Signal. Must go low at the beginning of an SPI transaction and high at the end of a transaction. Each SPI transaction may take a different number of CCLK cycles to complete, depending on the address and read/write bits that are sent at the beginning of the SPI transaction. When not used, this pin should be tied to ground, preferably with a 10 kΩ pull-down resistor.
22	SCL/CCLK	D_IN	Serial Clock/Continuous Clock. In I²C mode, this pin functions as SCL and is always an open collector input, except when in self-boot mode, where it is an open collector output (I²C master). The line connected to this pin should have a 2.0 kΩ pull-up resistor. In SPI mode, this pin functions as CCLK and is an input pin that can be either run continuously or gated off between SPI transactions.
23	SDA/COUT	D_IO	Serial Data/Continuous Output. In I²C mode, this pin functions as SDA and is a bidirectional open collector. The line connected to the SDA pin should have a 2.0 kΩ pull-up resistor. In SPI mode, this pin functions as COUT and is used for reading back registers and memory locations. The COUT pin is three-stated when an SPI read is not active.
24	ADDR1/CDATA	D_IN	Address 1/Continuous Data. In I²C mode, this pin functions as ADDR1 and, in combination with ADDR0, sets the I²C address of the IC. This allows up to four ADAU1442/ADAU1445/ADAU1446 devices to be used on the same I²C bus. In SPI mode, this pin functions as CDATA and is the SPI data input.
25, 37, 50, 75, 87, 100	DVDD	PWR	1.8 V Digital Supply. This can be supplied externally or generated from a 3.3 V supply with the on-board 1.8 V regulator. Each DVDD pin should be decoupled to DGND with a 100 nF capacitor.
28	SELFBOOT	D_IN	Self-Boot Select. Allows the ADAU1442/ADAU1445/ADAU1446 to be controlled by the control port or to perform a self-boot. Setting this pin high (that is, to 1) initiates a self-boot operation when the ADAU1442/ADAU1445/ADAU1446 are brought out of a reset. This pin can be tied directly to a voltage source or ground or pulled up/down with a resistor.
29	CLKMODE1	D_IN	Output Clock Mode 1. With CLKMODE0, this pin sets the frequency of the CLKOUT signal.
30	CLKMODE0	D_IN	Output Clock Mode 0. With CLKMODE1, this pin sets the frequency of the CLKOUT signal.
31	RSVD	D_IN	Reserved. Tie this pin to ground, preferably with a 10 kΩ pull-down resistor.
32	PLL2	D_IN	PLL Mode Select Pin 2.
33	MP7	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.

Pin No.	Mnemonic	Type[1]	Description
34	MP6	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
35	MP5	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
36	MP4	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
40	VDRIVE	A_OUT	Regulator Drive. Supplies the drive current for the 1.8 V regulator. The base of the voltage regulator's external PNP transistor is driven from VDRIVE.
41	XTALO	A_OUT	Crystal Oscillator Output. A 100 Ω damping resistor should be connected between this pin and the crystal. This output should not be used to directly drive a clock to another IC; the CLKOUT pin exists for this purpose. If the crystal oscillator is not used, the XTALO pin can be left unconnected.
42	XTALI	A_IN	Crystal Oscillator Input. This pin provides the master clock for the ADAU1442/ADAU1445/ADAU1446. If the ADAU1442/ADAU1445/ADAU1446 generate the master clock in the system, this pin should be connected to the crystal oscillator circuit. If the ADAU1442/ADAU1445/ADAU1446 are slaves to an external master clock, this pin should be connected to the master clock signal generated by another IC.
43	PLL_FILT	A_OUT	Phase-Locked Loop Filter. Two capacitors and a resistor must be connected to this pin as shown in Figure 11.
44	PVDD	PWR	Phase-Locked Loop Supply. Provides the 3.3 V power supply for the PLL. This should be decoupled to PGND with a100 nF capacitor.
45	PGND	PWR	Phase-Locked Loop Ground. Ground for the PLL supply. The AGND, DGND, and PGND pins can be tied directly together in a common ground plane. PGND should be decoupled to PVDD with a 100 nF capacitor.
46	SPDIFI	D_IN	S/PDIF Input. Accepts digital audio data in the S/PDIF format. When not used, this pin can be left disconnected.
47	SPDIFO	D_OUT	S/PDIF Output. Outputs digital audio data in the S/PDIF format. When not used, this pin can be left disconnected.
48	AVDD	PWR	Analog Supply. 3.3 V analog supply for the auxiliary ADC. This pin should be decoupled to AGND with a 100 nF capacitor.
49	AGND	PWR	Analog Ground. Ground for the analog supply. This pin should be decoupled to AVDD with a 100 nF capacitor.
53	CLKOUT	D_OUT	Master Clock Output. Used to output a master clock to other ICs in the system. Set using the CLKMODEx pins. When not used, this pin can be left disconnected.
54	$\overline{\text{RESET}}$	D_IN	Reset. Active-low reset input. Reset is triggered on a high-to-low edge and exited on a low-to-high edge. For detailed information about initialization, see the Power-Up Sequence section. A reset event sets all RAMs and registers to their default values.
55	MP3/ADC3	D_IO, A_IN	Multipurpose, General-Purpose Input or Output/Auxiliary ADC Input 3. When not used, this pin can be left disconnected.
56	MP2/ADC2	D_IO, A_IN	Multipurpose, General-Purpose Input or Output/Auxiliary ADC Input 2. When not used, this pin can be left disconnected.
57	MP1/ADC1	D_IO, A_IN	Multipurpose, General-Purpose Input or Output/Auxiliary ADC Input 1. When not used, this pin can be left disconnected.
58	MP0/ADC0	D_IO, A_IN	Multipurpose, General-Purpose IO/Auxiliary ADC Input 0. When not used, this pin can be left disconnected.
59	PLL1	D_IN	Phase-Locked Loop Mode Select Pin 1.
60	PLL0	D_IN	Phase-Locked Loop Mode Select Pin 0.
61	SDATA_OUT8	D_OUT	Serial Data Port 0 Output. When not used, this pin can be left disconnected.
64	BCLK11	D_IO	Bit Clock, Output Clock Domain 11. This pin is bidirectional, with the direction depending on whether the Output Clock Domain 11 is set up as a master or slave. When not used, this pin can be left disconnected.
65	LRCLK11	D_IO	Frame Clock, Output Clock Domain 11. This pin is bidirectional, with the direction depending on whether the Output Clock Domain 11 is set up as a master or slave. When not used, this pin can be left disconnected.

Pin No.	Mnemonic	Type[1]	Description
96	BCLK4	D_IO	Bit Clock, Input/Output Clock Domain 4. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 4 is set up as a master or slave. When not used, this pin can be left disconnected.
97	LRCLK4	D_IO	Frame Clock, Input/Output Clock Domain 4. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 4 is set up as a master or slave. When not used, this pin can be left disconnected.
98	SDATA_OUT0	D_OUT	Serial Data Port 0 Output. When not used, this pin can be left disconnected.
99	SDATA_IN3	D_IN	Serial Data Port 3 Output. When not used, this pin can be left disconnected.

[1] PWR = power/ground, A_IN = analog input, D_IN = digital input, A_OUT = analog output, D_OUT = digital output, D_IO = digital input/output.

OVERVIEW

The ADAU1442/ADAU1445/ADAU1446 are each a 24-channel audio DSP with an integrated S/PDIF receiver and transmitter, flexible serial audio ports, up to 16 channels of asynchronous sample rate converters (ASRCs), flexible audio routing, and user interface capabilities. Signal processing capabilities include equalization, crossover, bass enhancement, multiband dynamics processing, delay compensation, speaker compensation, and stereo image widening. These algorithms can be used to compensate for the real-world limitations of speakers, amplifiers, and listening environments, resulting in an improvement in the perceived audio quality.

An on-board oscillator can be connected to an external crystal to generate the master clock. A phase-locked loop (PLL) allows the ADAU1442/ADAU1445/ADAU1446 to be clocked from a variety of clock frequencies. The PLL can accept inputs of 64 × f_S, 128 × f_S, 256 × f_S, 384 × f_S, or 512 × f_S to generate the internal master clock of the core, where f_S is the sampling rate of audio in normal-rate processing mode. In dual- or quad-rate mode, these multipliers are halved or quartered, respectively. System sample rates include, but are not limited to, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, and 192 kHz.

Each ADAU1442/ADAU1445/ADAU1446 operates from a 1.8 V digital power supply and a 3.3 V analog supply. An on-board voltage regulator can be used to operate the chip from a single 3.3 V supply.

The ADAU1442/ADAU1445/ADAU1446 have a sophisticated control port that supports complete read and write capability of all memory locations, excluding read-only addresses. Control registers are provided to offer complete control of the chip's configuration and serial modes. Handshaking is included for ease of memory uploads and downloads. The ADAU1442/ADAU1445/ADAU1446 can be configured for either SPI or I²C control. Program RAM, parameter RAM, and register contents can be saved in an external EEPROM, from which the ADAU1442/ADAU1445/ADAU1446 can self-boot on startup.

The ADAU1442/ADAU1445/ADAU1446 serial ports operate with digital audio I/Os in the I²S, left-justified, right-justified, or TDM-compatible mode. The flexible serial data ports allow for direct interconnection to a variety of ADCs, DACs, and general-purpose DSPs. The combination of an on-board S/PDIF transmitter and receiver and 16 channels of ASRCs allows for easy compatibility with an extensive number of external devices, and a system with up to nine sampling rates.

The flexible audio routing matrix (FARM) is a system of multiplexers used to distribute the audio signals in the ADAU1442/ADAU1445/ADAU1446 among the serial inputs and outputs, audio core, and ASRCs. FARM can easily be configured by setting the appropriate registers.

The ADAU1442, ADAU1445, and ADAU1446 are distinguished by the number of on-board ASRCs and maximum sample rates. The ADAU1442 contains eight 2-channel ASRCs, the ADAU1445 contains two 8-channel ASRCs, and the ADAU1446 has no ASRCs.

Two sets of serial ports at the input and output can operate in a special flexible TDM mode, which allows the user to independently assign byte-specific locations to audio streams at varying bit depths. This mode ensures compatibility with codecs using similar flexible TDM streams.

The core of the ADAU1442/ADAU1445/ADAU1446 is a 28-bit DSP (or a 56-bit DSP when using double-precision mode) optimized for audio processing, and it can process audio at sample rates of up to 192 kHz. The program and parameter RAMs can be loaded with a custom audio processing signal flow built with the SigmaStudio graphical programming software from Analog Devices, Inc. The values stored in the parameter RAM control individual signal processing blocks, such as IIR and FIR equalization filters, dynamics processors, audio delays, and mixer levels. A software safeload feature allows for transparent parameter updates and prevents clicks on the output signals.

Reliability features such as a CRC and program counter watchdog help ensure that the system can detect and recover from any errors related to memory corruption.

S/PDIF signals can be routed through an ASRC for processing in the DSP or can be sent directly to output on MP pins for recovery of the embedded audio signal. Other components of the embedded signal, including status and user bits, are not lost and can be output on the MP pins as well.

Multipurpose (MP) pins are available for providing a simple user interface without the need for an external microcontroller. Twelve pins are available to input external control signals and output flags or controls to other devices in the system. Four of these can alternatively be assigned to an auxiliary ADC for use with analog controls such as potentiometers or system voltages. As inputs, MP pins can be connected to push buttons, switches, rotary encoders, potentiometers, or other external control circuitry to control the internal signal processing program. When configured as outputs, these pins can be used to drive LEDs (with a buffer), to output flags to a microcontroller, to control other ICs, or to connect to other external circuitry in an application.

The SigmaStudio software is used to program and control the ADAU1442/ADAU1445/ADAU1446 through the control port. Along with designing and tuning a signal flow, the software can configure all of the DSP registers in real time and download a new program and parameter into the external self-boot EEPROM. SigmaStudio's easy-to-use graphical interface allows anyone with audio processing knowledge to easily design a DSP signal flow and port it to a target application without the need for writing line-level code. At the same time, the software provides enough flexibility and programmability for an experienced DSP programmer to have in-depth control of the design. In SigmaStudio, the user can add signal processing cells from the library by dragging and dropping cells, connect them together in a flow, compile the design, and load the program and parameter files into the ADAU1442/ADAU1445/ADAU1446 memory through the control port. The complicated tasks of linking, compiling, and downloading the project are all handled automatically by the software.

Table 9. PLL Modes

DSP Core Rate[1]	Input to MCLK (XTALI Pin)	PLL2	PLL1	PLL0	PLL Divider[2]	Core Clock Multiplier	Core Clock (f_{CORE})	Instructions per Sample
Normal	64 × $f_{S,NORMAL}$	0	0	0	1	56	3584 × $f_{S,NORMAL}$	3584
	128 × $f_{S,NORMAL}$	0	0	1	2	56	3584 × $f_{S,NORMAL}$	3584
	256 × $f_{S,NORMAL}$	0	1	0	4	56	3584 × $f_{S,NORMAL}$	3584
	384 × $f_{S,NORMAL}$	0	1	1	6	56	3584 × $f_{S,NORMAL}$	3584
	512 × $f_{S,NORMAL}$	1	0	0	8	56	3584 × $f_{S,NORMAL}$	3584
Dual	32 × $f_{S,DUAL}$	0	0	0	1	56	1792 × $f_{S,DUAL}$	1792
	64 × $f_{S,DUAL}$	0	0	1	2	56	1792 × $f_{S,DUAL}$	1792
	128 × $f_{S,DUAL}$	0	1	0	4	56	1792 × $f_{S,DUAL}$	1792
	192 × $f_{S,DUAL}$	0	1	1	6	56	1792 × $f_{S,DUAL}$	1792
	256 × $f_{S,DUAL}$	1	0	0	8	56	1792 × $f_{S,DUAL}$	1792
Quad	16 × $f_{S,QUAD}$	0	0	0	1	56	896 × $f_{S,QUAD}$	896
	32 × $f_{S,QUAD}$	0	0	1	2	56	896 × $f_{S,QUAD}$	896
	64 × $f_{S,QUAD}$	0	1	0	4	56	896 × $f_{S,QUAD}$	896
	96 × $f_{S,QUAD}$	0	1	1	6	56	896 × $f_{S,QUAD}$	896
	128 × $f_{S,QUAD}$	1	0	0	8	56	896 × $f_{S,QUAD}$	896

[1] If the normal DSP core rate ($f_{S,NORMAL}$) is 44.1 kHz, the dual DSP core rate ($f_{S,DUAL}$) is 88.2 kHz, and the quad DSP core rate ($f_{S,QUAD}$) is 176.4 kHz. Likewise, if $f_{S,NORMAL}$ is 48 kHz, then $f_{S,DUAL}$ is 96 kHz and $f_{S,QUAD}$ is 192 kHz.
[2] The PLL divider is set by the PLLx pins.

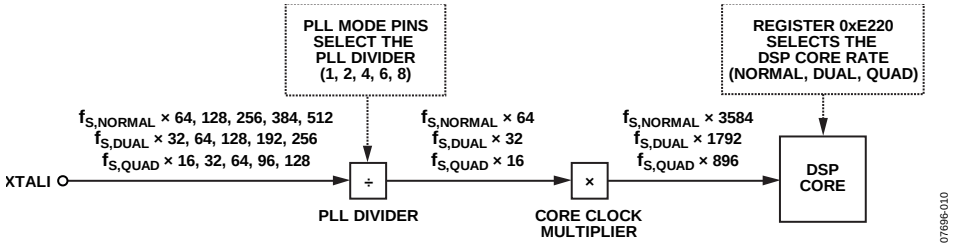

Figure 10. Master Clock Signal Flow

Table 12. Bit Descriptions of Register 0xE220

Bit Position	Description	Default
[15:5]	Reserved	
[4:0]	Start pulse select 00000 = internally generated normal rate ($f_{S,NORMAL}$) 00001 = internally generated dual rate ($f_{S,DUAL}$) 00010 = internally generated quad rate ($f_{S,QUAD}$) 00011 = f_S from serial input Stereo Pair 0[1] 00100 = f_S from serial input Stereo Pair 1[1] 00101 = f_S from serial input Stereo Pair 2[1] 00110 = f_S from serial input Stereo Pair 3[1] 00111 = f_S from serial input Stereo Pair 4[1] 01000 = f_S from serial input Stereo Pair 5[1] 01001 = f_S from serial input Stereo Pair 6[1] 01010 = f_S from serial input Stereo Pair 7[1] 01011 = f_S from serial input Stereo Pair 8[1] 01100 = f_S from serial input Stereo Pair 9[1] 01101 = f_S from serial input Stereo Pair 10[1] 01110 = f_S from serial input Stereo Pair 11[1] 01111 = f_S from serial output Stereo Pair 0[1] 10000 = f_S from serial output Stereo Pair 1[1] 10001 = f_S from serial output Stereo Pair 2[1] 10010 = f_S from serial output Stereo Pair 3[1] 10011 = f_S from serial output Stereo Pair 4[1] 10100 = f_S from serial output Stereo Pair 5[1] 10101 = f_S from serial output Stereo Pair 6[1] 10110 = f_S from serial output Stereo Pair 7[1] 10111 = f_S from serial output Stereo Pair 8[1] 11000 = f_S from serial output Stereo Pair 9[1] 11001 = f_S from serial output Stereo Pair 10[1] 11010 = f_S from serial output Stereo Pair 11[1] 11011 = f_S from S/PDIF receiver[1] 11100 = no start pulse; core is disabled 11101 = no start pulse; core is disabled 11110 = no start pulse; core is disabled 11111 = no start pulse; core is disabled	00000

[1] f_S is the LRCLK of the associated stereo audio pair in the flexible audio routing matrix whose frequency is dependent on the settings of its associated serial port and the clock pad multiplexer. The intended function of the DSP core rate select register is to allow the DSP core to be synchronized to an external LRCLK signal that is being used by any of the serial ports or S/PDIF receiver.

Self-Boot

On power-up, the ADAU1442/ADAU1445/ADAU1446 can load a program and a set of parameters that are saved in an external EEPROM. Combined with the auxiliary ADC and the multipurpose pins, this can potentially eliminate the need for a microcontroller in a simple audio system. The self-boot sequence is accomplished by the ADAU1442/ADAU1445/ADAU1446 acting as masters on the I²C bus on startup, which occurs when the SELFBOOT pin is set high. The ADAU1442/ADAU1445/ADAU1446 cannot self-boot in SPI mode.

The maximum necessary EEPROM size is 40,960 bytes, or 40 kB. This much memory is only needed if the program RAM (4096 × 6 bytes) and parameter RAM (4096 × 4 bytes) are each completely full.

A self-boot operation is triggered on the rising edge of $\overline{\text{RESET}}$ when the SELFBOOT pin is set high, and it occurs after 10 ms when the PLL has locked. The ADAU1442/ADAU1445/ADAU1446 read the program, parameter, and register data from the EEPROM. After the ADAU1442/ADAU1445/ADAU1446 have finished self-booting, additional messages can be sent to the ADAU1442/ADAU1445/ADAU1446 on the I²C bus, although this typically is not necessary in a self-booting application. The I²C device address for the ADAU1442/ADAU1445/ADAU1446 is 0x68 for a write and 0x69 for a read in this mode. The ADDRx pins have different functions when the chip is in this mode; therefore, the settings on them are ignored.

The ADAU1442/ADAU1445/ADAU1446 are masters on the I²C bus during a self-boot operation. Care should be taken that no other device on the I²C bus tries to perform a write operation during self-booting. The ADAU1442/ADAU1445/ADAU1446 generate SCL at 8 × f_s; therefore, when $f_{s,NORMAL}$ is 48 kHz, SCL runs at 384 kHz. SCL has a duty cycle of ⅜ in accordance with the I²C specification.

The ADAU1442/ADAU1445/ADAU1446 read from EEPROM Chip Address 0xA1. The LSBs of the addresses of some EEPROMs are pin configurable; in most cases, these pins should be tied low to set this address. SigmaStudio writes to the EEPROM at Address 0xA0.

EEPROM Format

The EEPROM data contains a sequence of messages. Each discrete message is one of the four types defined in Table 17. Each message consists of a sequence of one or more bytes. The first byte identifies the message type. Bytes are written MSB first. Most messages are block write (0x01) types, which are used for writing to the ADAU1442/ADAU1445/ADAU1446 program RAM, parameter RAM, and control registers.

The body of the message following the message type should start with two bytes indicating message length and then include a byte indicating the chip address. Following this is always a 2-byte register or memory address field, as with all other control port transactions.

SigmaStudio is capable of generating the EEPROM data necessary to self-boot the ADAU1442/ADAU1445/ADAU1446, using the function called write latest compilation to E2PROM. This function can be accessed by right-clicking the ADAU1442/ADAU1445/ADAU1446 IC in the hardware configuration window.

Table 16. Functions of the Control Port Pins

Pin	I²C Mode	SPI Mode	Self-Boot
SCL/CCLK	SCL—input	CCLK—input	SCL—output
SDA/COUT	SDA—open collector output	COUT—output	SDA—open collector output
ADDR1/CDATA	ADDR1—input	CDATA—input	Unused input—tie to ground or power
CLATCH	Unused input—tie to ground or power	CLATCH—input	Unused input—tie to ground or power
ADDR0	ADDR0—input	ADDR0—input	Unused input—tie to ground or power

Table 17. EEPROM Message Types

Message ID	Message Type	Following Bytes
0x00	End	None
0x01	Write	One byte indicating message length (including chip address and subaddress), one byte indicating chip address, two bytes indicating subaddress, and an appropriate number of data bytes
0x02	Delay	Two bytes for delay
0x03	No op	None

Serial Output Port Modes Registers (Address 0xE040 to Address 0xE049)

Table 29. Addresses of Serial Output Port Modes Registers

Address			
Decimal	**Hex**	**Name**	**Read/Write Word Length**
57408	E040	Serial Output Port 0 modes	16 bits (2 bytes)
57409	E041	Serial Output Port 1 modes	16 bits (2 bytes)
57410	E042	Serial Output Port 2 modes	16 bits (2 bytes)
57411	E043	Serial Output Port 3 modes	16 bits (2 bytes)
57412	E044	Serial Output Port 4 modes	16 bits (2 bytes)
57413	E045	Serial Output Port 5 modes	16 bits (2 bytes)
57414	E046	Serial Output Port 6 modes	16 bits (2 bytes)
57415	E047	Serial Output Port 7 modes	16 bits (2 bytes)
57416	E048	Serial Output Port 8 modes	16 bits (2 bytes)
57417	E049	High speed slave interface mode	1 bit (2 bytes)

Clock Output Enable Bit (Bit 15)

This bit controls the serial port's respective bit clock as well as the left and right clocks. When this bit is set to 1, the clock pins are set to output. When this bit is set to 0, the clock pins are not output clocks. In Register 0xE040 to Register 0xE048, Bit 15 and Bits[13:10] must be used in conjunction to set the port as a master or slave. Clock domains are assigned to input or output serial ports with the clock pad multiplexer register (Address 0xE240). For more information, see the Clock Pad Multiplexer section.

Frame Sync Type Bit (Bit 14)

This bit sets the type of LRCLK signal that is used. When this bit is set to 0, the clock signal is a square wave. When this bit is set to 1, the signal is a narrow pulse.

Clock Domain Master/Slave Select Bits (Bits[13:10])

These bits set whether the serial port outputs its clocks as a master or slave to an available clock domain. If a serial port is set to be a master, the clock output enable bit (Bit 15) must be set to 1. If a serial port is set as a slave, the clock output enable bit (Bit 15) must be set to 0. In both cases, the corresponding clock pad multiplexer must be set to the serial output domain if it is assignable. For more information, see the Clock Pad Multiplexer section. Note that an arbitrary number of serial ports can be slaves to a single clock domain, but a single serial port can only be a master to one clock domain. The values for $f_{S,NORMAL}$, $f_{S,DUAL}$, and $f_{S,QUAD}$ are 48 kHz, 96 kHz, and 192 kHz, respectively, for a 172.032 MHz core clock signal.

Serial Output BCLK Polarity Bit (Bit 9)

The polarity of BCLKx determines whether LRCLKx and SDATA_OUTx change on a rising (+) or falling (−) edge of the BCLKx signal. Standard I²S signals use negative BCLK polarity.

Serial Output LRCLK Polarity Bit (Bit 8)

The polarity of LRCLKx determines whether the left stereo channel is initiated on a rising (+) or falling (−) edge of the LRCLKx signal. Standard I²S signals use negative LRCLK polarity.

Word Length Bits (Bits[7:6])

These bits set the word length of the input data at 16, 20, or 24 bits. The output stream always has space for 24 bits of data, but if the word length is set lower, the extra bits are set as 0s. The fourth setting is flexible TDM. For more information, see the Serial Output Flexible TDM Interface Modes and Settings section.

MSB Position Bits (Bits[5:3])

These bits set the position of the MSB in the data stream.

TDM Type Bits (Bits[2:0])

These bits set the number of channels contained in the data stream. The possible choices are TDM2 (stereo), TDM4, TDM8 or flexible TDM, TDM16, and packed TDM4 mode. For more information on the packed TDM4 mode, see the Packed TDM4 Mode section. If word length bits (Bits[7:6]) are set to 11 for flexible TDM mode, then the TDM type bits (Bits[2:0]) must also be set for flexible TDM mode (that is, set to 010).

High Speed Slave Interface Mode Register (Address 0xE049)

Table 31. Bit Descriptions of Register 0xE049

Bit Position	Description	Default
[15:1]	Reserved	
0	High speed slave interface mode 0 = disabled 1 = enabled	0

High Speed Slave Interface Mode Bit (Bit 0)

If any of the serial output ports are slaves to a bit clock greater than 22 MHz, the high speed slave interface mode must be enabled.

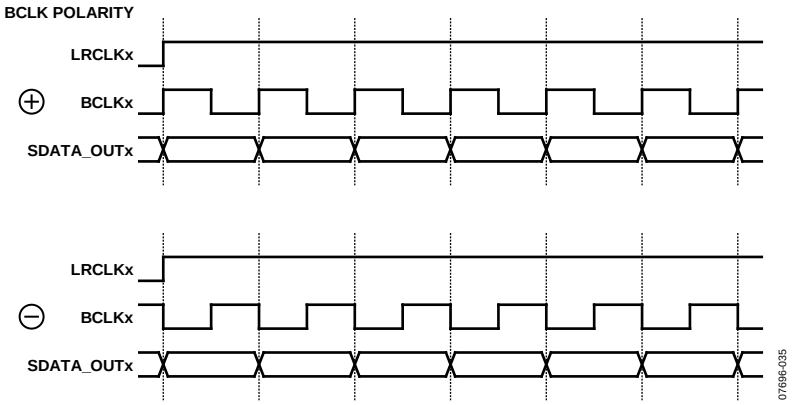

Figure 34. Serial Output BCLK Polarity

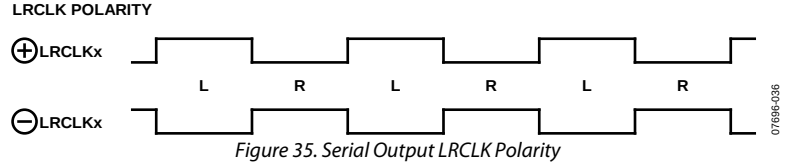

Figure 35. Serial Output LRCLK Polarity

Serial Output Data Selector Bits (Bits[5:0])

These bits select where each of the 12 stereo serial output channels comes from. The channels can come either from one of the 12 DSP core stereo outputs or from one of the eight ASRC stereo outputs.

In the case of the ADAU1446, setting the serial output data selector bits to a value corresponding to an ASRC output pair yields no data.

As shown in Figure 50, the stereo output pairs can come from any of the DSP serial or ASRC outputs.

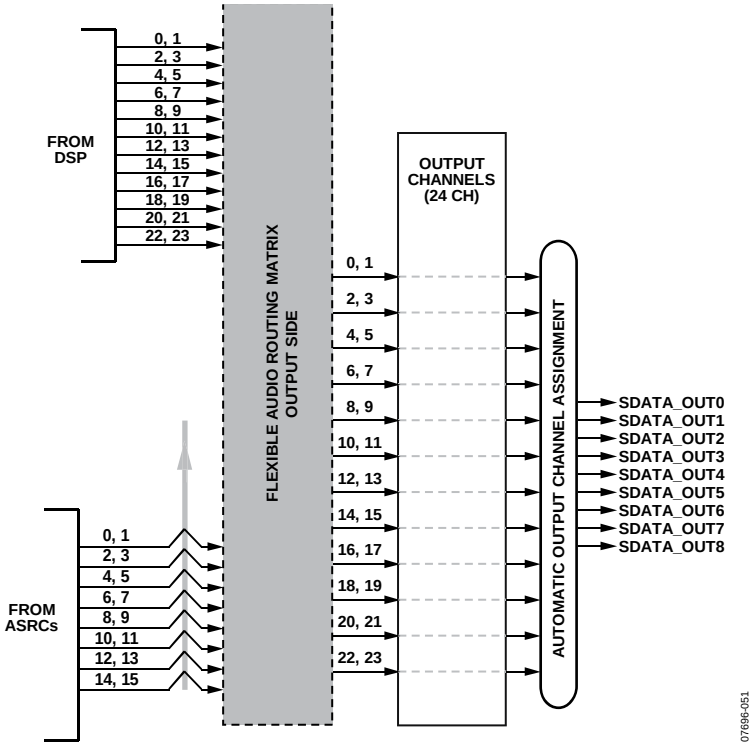

Figure 50. Serial Output Select Pair

DSP CORE

The DSP core performs calculations on audio data as specified by the instruction codes stored in program RAM. Because SigmaStudio generates the instructions, it is not necessary to have a detailed knowledge of the DSP core to use the SigmaDSP, but a brief description is provided in this section.

Architecture

The core consists of a simple 28-/56-bit multiply-accumulate unit (MAC) with two sources: a data source and a coefficient source. The data source can come from the data RAM, a ROM table of commonly used constant values, or the audio inputs to the core. The coefficient source can come from the parameter RAM, a ROM table of commonly used constant values. The two sources are multiplied in a 28-bit fixed-point multiplier, and then the signal is input to the 56-bit adder; the result is usually stored in one of three 56-bit accumulator registers. The accumulators can be output from the core (in 28-bit format) or can optionally be written back into the data or parameter RAMs.

Features

The SigmaDSP core is designed specifically for audio processing and, therefore, includes several features intended for maximizing efficiency. These include hardware decibel conversion and audio-specific ROM constants.

Signal Processing

The ADAU1442/ADAU1445/ADAU1446 are designed to provide all signal processing functions commonly used in stereo or multichannel playback systems. The signal processing flow is designed using SigmaStudio software from Analog Devices. This software allows graphical entry and real-time control of all signal processing functions.

Many of the signal processing functions are coded using full, 56-bit, double-precision arithmetic. The serial port input and output word lengths are 24 bits, but four extra headroom bits are used in the processor to allow internal gains of up to 24 dB without clipping. Additional gains can be achieved by initially scaling down the input signal in the DSP signal flow.

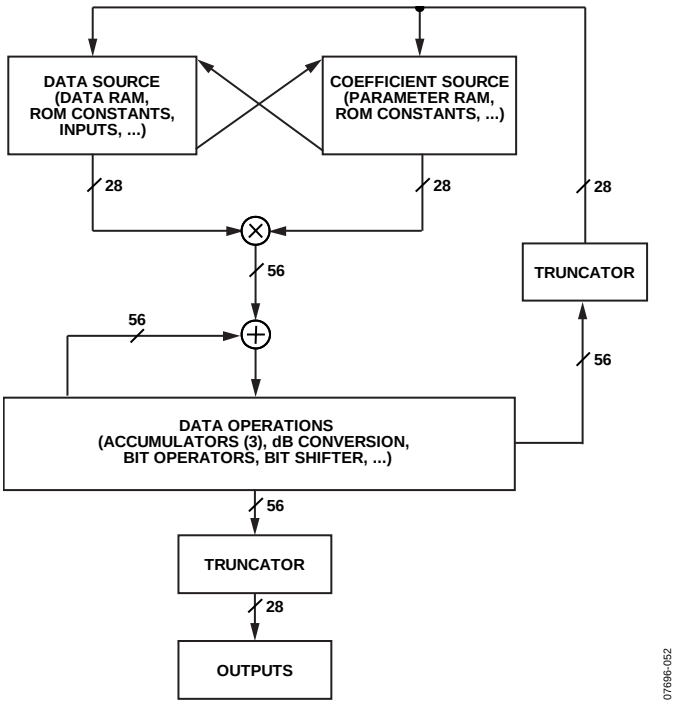

Figure 51. Simplified Core Architecture

Auxiliary Outputs—Set Enable Mode Register (Address 0xE0C8)

Table 59. Bit Descriptions of Register 0xE0C8

Bit Position	Description	Default
[15:2]	Reserved	
[1:0]	Auxiliary outputs enable mode 00 = auxiliary outputs are always off. 01 = auxiliary outputs are always on. 10 = auxiliary outputs are off on reset. (They switch on as soon as the hot enable bit is 1 and switch off as soon as the S/PDIF lock bit is 0.)	01

This register controls when the S/PDIF stream is active on the multipurpose pins when the S/PDIF to I²S mode is active. For more information, see the Enable S/PDIF to I²S Output section.

Setting Bits[1:0] of Register 0xE0C8 to 10 (auxiliary outputs are off on reset) is useful for situations in which the S/PDIF stream may be interrupted unexpectedly. An interruption causes the S/PDIF lock bit to go low, which in turn disables the auxiliary outputs. When the S/PDIF stream is recovered, the hot enable bit must be activated to restore the auxiliary outputs (see the Set Hot Enable Register (Address 0xE0CA) section for more information).

S/PDIF Lock Bit Detection Register (Address 0xE0C9)

Table 60. Bit Descriptions of Register 0xE0C9

Bit Position	Description
[15:1]	Reserved
0	S/PDIF input lock bit (read only) 0 = no valid input stream 1 = successful lock to input stream

This read-only register shows the status of the S/PDIF input lock bit.

Set Hot Enable Register (Address 0xE0CA)

Table 61. Bit Descriptions of Register 0xE0CA

Bit Position	Description	Default
[15:1]	Reserved	
0	Hot enable bit 0 = hot enable inactive 1 = hot enable active	0

This register allows the hot enable bit to be set, which restarts the auxiliary outputs when they are configured so that the auxiliary outputs are off on a reset (that is, Bits[1:0] of Register 0xE0C8 are set to 10). The hot enable bit is set to 0 automatically in the event that the S/PDIF receiver loses lock. For more information, see the Auxiliary Outputs—Set Enable Mode Register (Address 0xE0C8) section.

Read Enable Auxiliary Output Register (Address 0xE0CB)

Table 62. Bit Descriptions of Register 0xE0CB

Bit Position	Description
[15:1]	Reserved
0	Read enable auxiliary output (read only) 0 = S/PDIF auxiliary outputs disabled 1 = S/PDIF auxiliary outputs enabled

This read-only register shows the status of the S/PDIF auxiliary outputs.

S/PDIF Loss-of-Lock Behavior Register (Address 0xE0CC)

Table 63. Bit Descriptions of Register 0xE0CC

Bit Position	Description	Default
[15:1]	Reserved	
0	S/PDIF loss-of-lock behavior 0 = S/PDIF disable on loss of lock 1 = S/PDIF ignore loss of lock	0

This register controls the behavior of the S/PDIF receiver in the event of a loss of lock to the input stream. A loss of lock can arise when there is severe noise or jitter on the S/PDIF input stream, rendering it unrecognizable to the receiver. In the default mode, such an event disables the S/PDIF receiver, causing it to stop outputting frame sync pulses. This in turn causes the target ASRC to be muted. Frame sync pulses do not resume until lock is regained.

When the register is set to 1, the S/PDIF receiver always outputs frame sync pulses, even if the integrity of the S/PDIF stream is compromised and the audio samples cannot be recovered. In such a case, the S/PDIF receiver data output remains at 0 until lock is regained.

The S/PDIF receiver is robust and can recover streams with integrity well below the standards of the AES/EBU specification. Therefore, even in cases of extreme signal degradation, this register should be used only when audio recovery is required. In general, a loss-of-lock event is much shorter than an ASRC mute or unmute ramp.

Enable S/PDIF to I²S Output Register (Address 0xE241)

Table 64. Bit Descriptions of Register 0xE241

Bit Position	Description	Default
[15:3]	Reserved	
2	Output mode 0 = I²S 1 = TDM	0
1	Group 2 enable 0 = Group 2 off 1 = Group 2 on	0
0	Group 1 enable 0 = Group 1 off 1 = Group 1 on	0

The S/PDIF receiver can be set to send the stereo audio stream and the auxiliary S/PDIF bits in I²S or TDM format on eight of the 12 MP pins. The eight outputs are divided into two groups: Group 1 converts S/PDIF to I²S (LRCLK, BCLK, and SDATA signals), and Group 2 decodes the channel status and user data bits (virtual LRCLK, user data, channel status, validity bit, and block start signal).

This MP output is controlled by setting three bits in Register 0xE241:

- Bit 0 switches Group 1 on and off.
- Bit 1 switches Group 2 on and off.
- Bit 2 switches between I²S and TDM modes.

When S/PDIF to I²S mode is active, the pins described in Table 53 are used.

When TDM mode is active, Slot 0 and Slot 4 contain the audio data, and Slot 1 contains the streamed block start, channel status, user data, and validity bits (see Table 65). The bits are streamed in real time and are synchronized to the audio data. Only the seven MSBs of Slot 1 are used, as shown in Table 65. The corresponding TDM format is shown in more detail in Figure 54.

Table 65. Function of Decoded Bits in Figure 54

Bit Position	Description
31	Block start (high for first 16 samples)
30	Channel status of right channel
29	Channel status of left channel
28	User data bit, right channel
27	User data bit, left channel
26	Validity bit, right channel
25	Validity bit, left channel
[24:0]	Not used

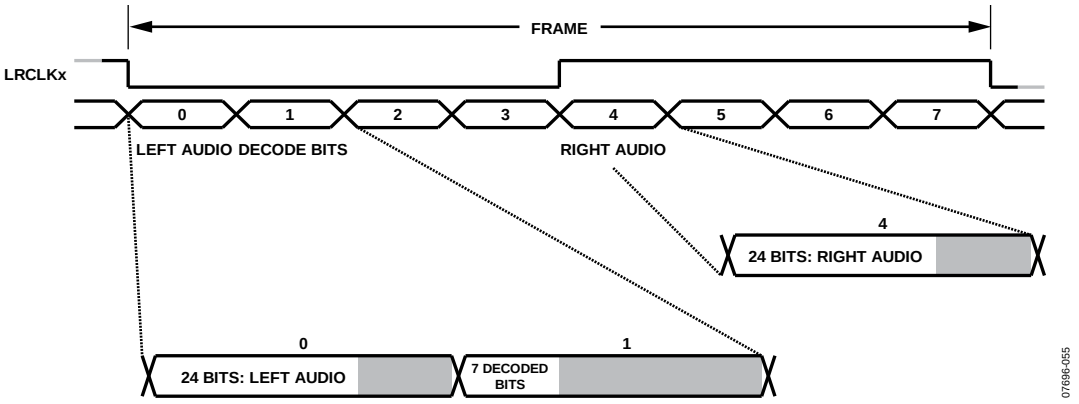

Figure 54. S/PDIF TDM Signal

Flexible TDM to Input Channel Modes Registers (Address 0xE180 to Address 0xE197)

Table 76. Addresses of Serial Input Flexible TDM Interface Modes Registers

Address			
Decimal	**Hex**	**Name**	**Read/Write Word Length**
57728	E180	Flexible TDM to Input Channel 0	16 bits (2 bytes)
57729	E181	Flexible TDM to Input Channel 1	16 bits (2 bytes)
57730	E182	Flexible TDM to Input Channel 2	16 bits (2 bytes)
57731	E183	Flexible TDM to Input Channel 3	16 bits (2 bytes)
57732	E184	Flexible TDM to Input Channel 4	16 bits (2 bytes)
57733	E185	Flexible TDM to Input Channel 5	16 bits (2 bytes)
57734	E186	Flexible TDM to Input Channel 6	16 bits (2 bytes)
57735	E187	Flexible TDM to Input Channel 7	16 bits (2 bytes)
57736	E188	Flexible TDM to Input Channel 8	16 bits (2 bytes)
57737	E189	Flexible TDM to Input Channel 9	16 bits (2 bytes)
57738	E18A	Flexible TDM to Input Channel 10	16 bits (2 bytes)
57739	E18B	Flexible TDM to Input Channel 11	16 bits (2 bytes)
57740	E18C	Flexible TDM to Input Channel 12	16 bits (2 bytes)
57741	E18D	Flexible TDM to Input Channel 13	16 bits (2 bytes)
57742	E18E	Flexible TDM to Input Channel 14	16 bits (2 bytes)
57743	E18F	Flexible TDM to Input Channel 15	16 bits (2 bytes)
57744	E190	Flexible TDM to Input Channel 16	16 bits (2 bytes)
57745	E191	Flexible TDM to Input Channel 17	16 bits (2 bytes)
57746	E192	Flexible TDM to Input Channel 18	16 bits (2 bytes)
57747	E193	Flexible TDM to Input Channel 19	16 bits (2 bytes)
57748	E194	Flexible TDM to Input Channel 20	16 bits (2 bytes)
57749	E195	Flexible TDM to Input Channel 21	16 bits (2 bytes)
57750	E196	Flexible TDM to Input Channel 22	16 bits (2 bytes)
57751	E197	Flexible TDM to Input Channel 23	16 bits (2 bytes)

Table 77. Bit Descriptions of Flexible TDM to Input Channel Modes Registers

Bit Position	Description	Default
[15:9]	Reserved	
8	MSB position 0 = MSB first 1 = LSB first	1
[7:6]	Number of bytes in the channel (audio bit depth) 00 = 1 byte (8-bit audio) 01 = 2 bytes (16-bit audio) 10 = 3 bytes (24-bit audio) 11 = unused	11
[5:0]	Position of the first byte on the TDM stream 000000 = TDM Slot 0 000001 = TDM Slot 1 … 111110 = TDM Slot 62 111111 = TDM Slot 63	111111

SOFTWARE FEATURES

SOFTWARE SAFELOAD

To update parameters in real time while avoiding pop and click noises on the output, the ADAU1442/ADAU1445/ADAU1446 use a software safeload mechanism. SigmaStudio automatically sets up the necessary code and parameters for new projects. The safeload code, along with other initialization code, fills the first 36 locations in program RAM. The first eight parameter RAM locations (Address 0x0000 to Address 0x0007) are configured by default in SigmaStudio as described in Table 81.

Table 81. Software Safeload Parameter RAM Defaults

Address (Hex)	Function
0x0000	Modulo RAM size
0x0001	Safeload Data 1
0x0002	Safeload Data 2
0x0003	Safeload Data 3
0x0004	Safeload Data 4
0x0005	Safeload Data 5
0x0006	Safeload target address (offset of −1)
0x0007	Number of words to write/safeload trigger

Address 0x0000, which controls the modulo RAM size, is set by SigmaStudio and is based on the dynamic address generator mode of the project.

Address 0x0001 to Address 0x0005 are the five data slots for storing the safeload data. The safeload parameter space contains five data slots by default because most standard signal processing algorithms have five parameters or fewer.

Address 0x0006 is the target address in parameter RAM (with an offset of −1). This designates the first address to be written. If more than one word is written, the address increments automatically for each data-word. The reason for the target address offset of −1 is that the write address is calculated relative to the address of the data, which starts at Address 0x0001. Therefore, if the intention is to update a parameter at Address 0x000A, the target address should be 0x0009.

Address 0x0007 designates the number of words to be written. For a biquad filter, the number is five. For a simple monogain cell, the number is one. This address also serves as the trigger; when it is written, a safeload write is triggered on the next frame.

The safeload mechanism is software based and executes once per audio frame. Therefore, system designers should take care when designing the communication protocol. A delay equal to or greater than the sampling period (the inverse of sampling frequency) is required between each safeload write. At a sample rate of 48 kHz, this equates to a delay of greater than or equal to 20.83 µs. If this delay is not observed, the downloaded data will be corrupted.

SOFTWARE SLEW

When the values of signal processing parameters are changed abruptly in real time, they sometimes cause pop and click sounds to appear on the audio outputs. To avoid this, some algorithms in SigmaStudio implement a software slew functionality. Software slew algorithms set a target value for the parameter and continuously update the parameter's value until it reaches the target.

The target value takes an additional space in parameter RAM, and the current value of the parameter is updated in the nonmodulo section of data RAM. Assignment of parameters and nonmodulo data RAM is handled by the SigmaStudio compiler and does not need to be programmed manually.

Slew parameters can follow several different curves, including an RC-type curve and a linear curve. These curve types are coded into each algorithm and cannot be modified by the user.

Because algorithms that use software slew generally require more RAM than their nonslew equivalents, they should be used only in situations in which a parameter is expected to change during operation of the device.

Figure 59 shows an example of a volume slew applied to a sine wave.

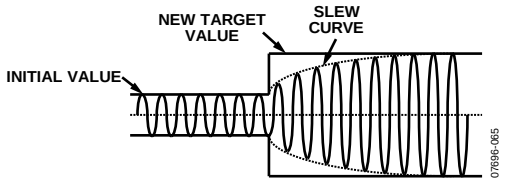

Figure 59. Example of Volume Slew

GLOBAL RAM AND REGISTER MAP

This section contains a list of all RAMS and registers.

OVERVIEW OF REGISTER ADDRESS MAP

Table 82. ADAU1442/ADAU1445/ADAU1446 RAM and Register Map

Address					
Decimal		Hex			
Start Value	End Value	Start Value	End Value	Name	Read/Write Word Length
0	4095	0000	0FFF	Parameter RAM	28 bits (4 bytes)
8192	12287	2000	2FFF	Program RAM	43 bits (6 bytes)
16384	24575	4000	5FFF	Data RAM	28 bits (4 bytes)
57344	57352	E000	E008	Serial input port modes	16 bits (2 bytes)
57408	57417	E040	E049	Serial output port modes	16 bits (2 bytes)
57472	57499	E080	E09B	Flexible audio routing matrix modes	16 bits (2 bytes)
57536	57548	E0C0	E0CC	S/PDIF modes	16 bits (2 bytes)
57601	57667	E101	E143	ASRC modes	16 bits (2 bytes)
57728	57751	E180	E197	Serial input flexible TDM interface modes	16 bits (2 bytes)
57792	57823	E1C0	E1DF	Serial output flexible TDM interface modes	16 bits (2 bytes)
57856	57984	E200	E280	Other modes	16 bits (2 bytes)

DETAILS OF REGISTER ADDRESS MAP

Table 83. Program RAM Registers

Address			
Decimal	Hex	Name	Read/Write Word Length
8192	2000	Program RAM	43 bits (6 bytes)

Table 84. Parameter RAM Registers

Address			
Decimal	Hex	Name	Read/Write Word Length
0	0000	Parameter RAM	28 bits (4 bytes)

Table 85. Data RAM Registers

Address			
Decimal	Hex	Name	Read/Write Word Length
16384	4000	Data RAM	28 bits (4 bytes)

APPLICATIONS INFORMATION

LAYOUT RECOMMENDATIONS

Parts Placement

All 100 nF bypass capacitors, which are recommended for every analog, digital, and PLL power-ground pair, should be placed as close to the ADAU1442/ADAU1445/ADAU1446 as possible. The AVDD, DVDD, PVDD, and IOVDD supply signals on the board should each be bypassed with an additional single bulk capacitor (10 µF to 47 µF).

All traces in the crystal oscillator circuit (Figure 9) should be kept as short as possible to minimize stray capacitance. There should not be any long board traces connected to crystal oscillator circuit components because such traces may affect crystal startup and operation.

Grounding

A single ground plane should be used in the application layout. Components in an analog signal path should be placed away from digital signals.

Exposed Pad PCB Design

The ADAU1442 and ADAU1445 packages include an exposed pad for improved heat dissipation. When designing a board for such a package, special consideration should be given to the following:

- A copper layer equal in size to the exposed pad should be on all layers of the board, from top to bottom, and should connect somewhere to a dedicated copper board layer (see Figure 60).
- Vias should be placed to connect all layers of copper, allowing for efficient heat and energy conductivity. For an example, see Figure 61, which has 16 vias arranged in a 4 × 4 grid in the pad area.

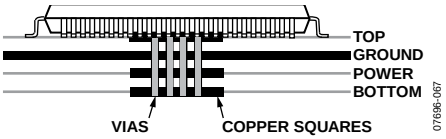

Figure 60. Exposed Pad Layout Example—Side View

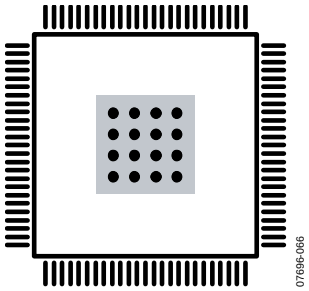

Figure 61. Exposed Pad Layout Example—Top View

PLL Loop Filter

The single resistor and two capacitors in the PLL loop filter should be connected to the PLL_FILT and PVDD pins with short traces to minimize jitter.

Power Supply Bypass Capacitors

Each power supply pin should be bypassed to its nearest appropriate ground pin with a single 100 nF capacitor. The connections to each side of the capacitor should be as short as possible, and the trace should stay on a single layer with no vias. For maximum effectiveness, the capacitor should preferably be located either equidistant from the power and ground pins or, when equidistant placement is not possible, slightly closer to the power pin. Thermal connections to the planes should be made on the far side of the capacitor.

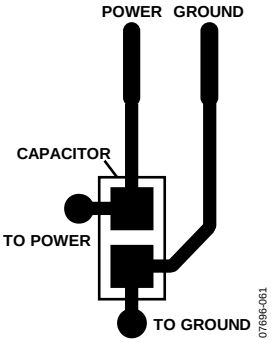

Figure 62. Recommended Power Supply Bypass Capacitor Layout

EOS/ESD Protection

Although the ADAU1442/ADAU1445/ADAU1446 have robust internal protection circuitry against overvoltages and electrostatic discharge, an external transient voltage suppressor (TVS) is recommended for all systems to prevent damage to the IC. Examples can be found in the AN-311 Application Note on the Analog Devices website.