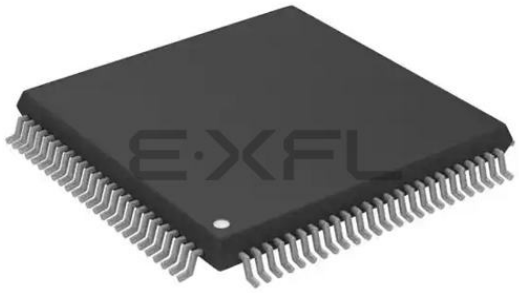

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Sigma
Interface	I²C, SPI
Clock Rate	172MHz
Non-Volatile Memory	-
On-Chip RAM	46kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adau1446ystz-3a

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
I/O Sample Rate Ratio	1:8		7.75:1		
THD + N		−133	−120	dB	
CRYSTAL OSCILLATOR					
Transconductance		40		mS	
REGULATOR[2]					
DVDD Voltage	1.65	1.75	1.85	V	Maximum 500 mA load.

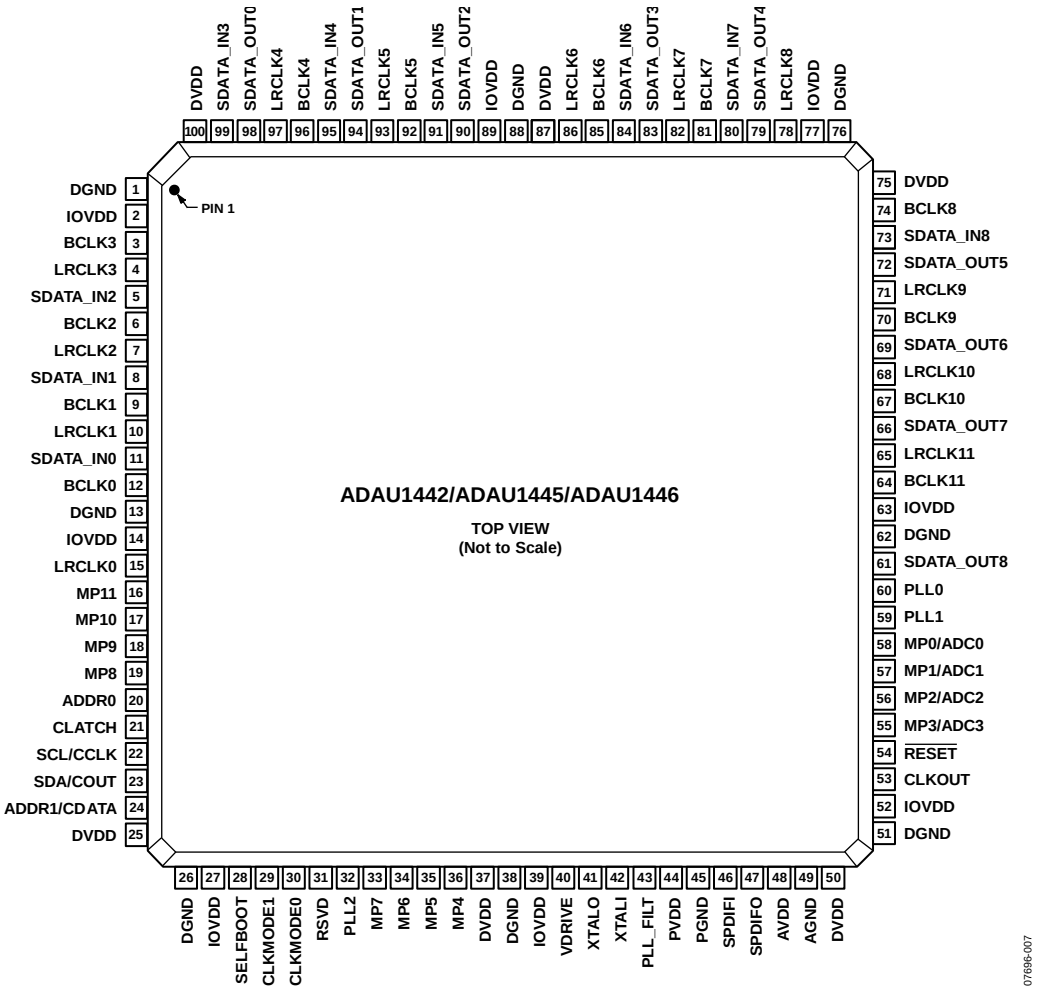
[1] To calculate the group delay, refer to the SRC Group Delay section.
[2] Regulator specifications are calculated using an NJT4030P transistor from On Semiconductor in the circuit.

AVDD = 3.3 V ± 10%, DVDD = 1.8 V ± 10%, PVDD = 3.3 V, IOVDD = 3.3 V ± 10%, T_A = −40°C to +105°C, master clock input = 12.288 MHz, core clock f_{CORE} = 172.032 MHz, I/O pins set to 2 mA drive setting, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG PERFORMANCE					AVDD = 3.3 V ± 10%.
Auxiliary Analog Inputs					
Resolution		10		Bits	
Full-Scale Analog Input		AVDD		V	
Integral Nonlinearity (INL)	−2.3		+2.3	LSB	
Differential Nonlinearity (DNL)	−2.0		+2.0	LSB	
Gain Error	−2.0		+2.0	LSB	
Input Impedance		200		kΩ	
Sample Rate		f_{CORE}/896		kHz	4:1 multiplexed input, each channel at f_{CORE}/3584. For f_{CORE} = 172.032 MHz, each channel is sampled at 48 kHz.
DIGITAL I/O					
Input Voltage, High (V_{IH})	0.7 × IOVDD			V	Digital input pins except SPDIFI.[1]
Input Voltage, Low (V_{IL})			0.3 × IOVDD	V	Digital input pins except SPDIFI.[1]
Input Leakage, High (I_{IH}) at 3.3 V	−2		+2	µA	Digital input pins except MCLK and SPDIFI.
	−2		+8	µA	MCLK.
	60		140	µA	SPDIFI.
Input Leakage, Low (I_{IL}) at 0 V	−85		−10	µA	All other pins.
	−2		+2	µA	CLKMODEx, RSVD, PLLx, RESET.
	−8		+2	µA	MCLK.
	−140		−60	µA	SPDIFI.
High Level Output Voltage (V_{OH})	0.85 × IOVDD			V	I_{OH} = 1 mA.
Low Level Output Voltage (V_{OL})			0.1 × IOVDD	V	I_{OL} = 1 mA.
Input Capacitance (C_I)		5		pF	Guaranteed by design.
Multipurpose Pins Output Drive		2		mA	These pins are not designed for static current draw and should not drive LEDs directly.
POWER					
Supply Voltage					
Analog Voltage (AVDD)	2.97	3.3	3.63	V	
Digital Voltage (DVDD)	1.62	1.8	1.98	V	
PLL Voltage (PVDD)	2.97	3.3	3.63	V	
IOVDD Voltage (IOVDD)	2.97	3.3	3.63	V	
Supply Current					
Analog Current (AVDD)		2		mA	

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD DOES NOT HAVE AN INTERNAL ELECTRICAL CONNECTION TO THE INTEGRATED CIRCUIT, BUT SHOULD BE CONNECTED TO THE GROUND PLANE OF THE PCB FOR PROPER HEAT DISSIPATION.

Figure 7. Pin Configuration

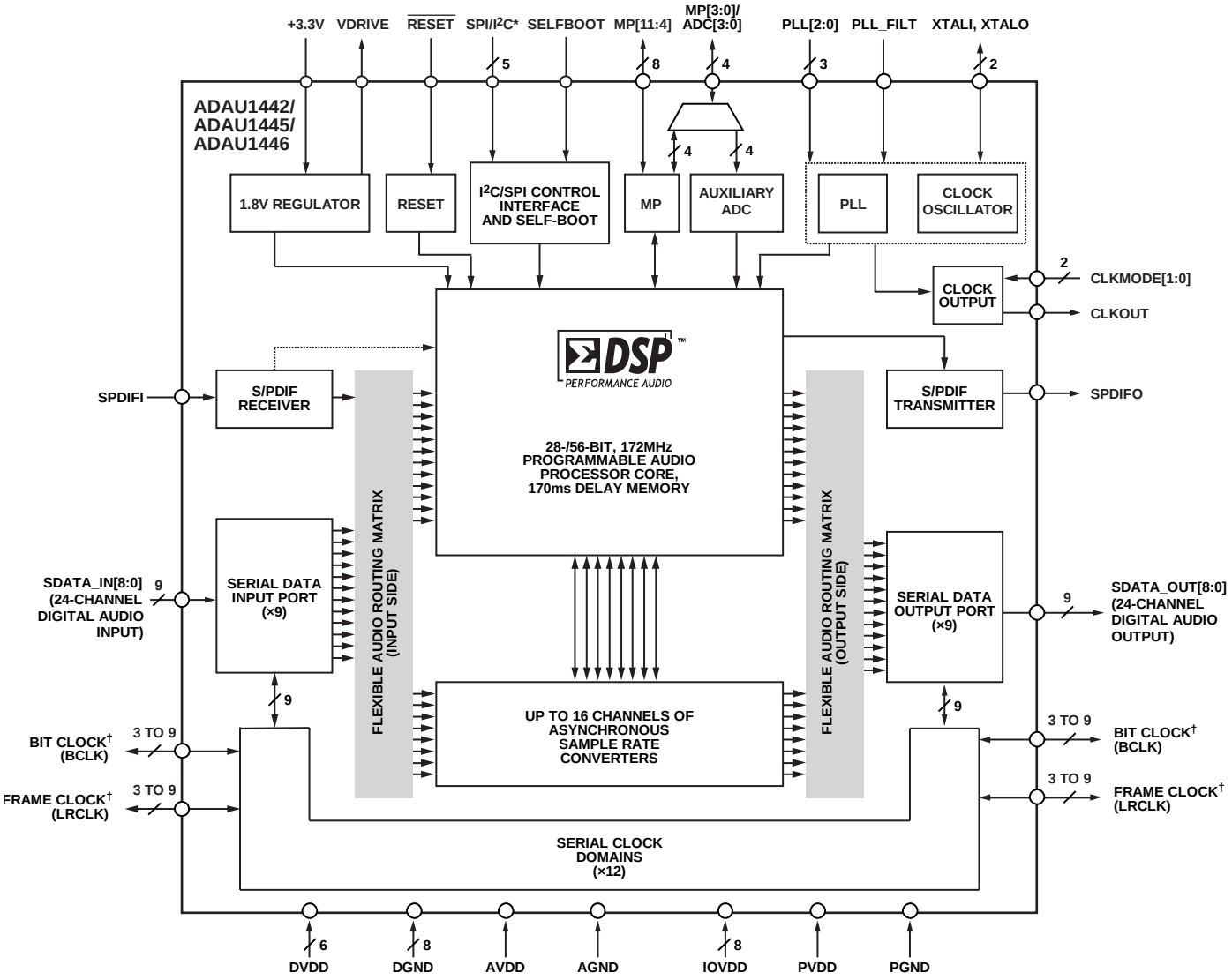
Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 13, 26, 38, 51, 62, 76, 88	DGND	PWR	Digital Ground. The AGND, DGND, and PGND pins should be tied directly together in a common ground plane. DGND pins should be decoupled to a DVDD pin with a 100 nF capacitor.
2, 14, 27, 39, 52, 63, 77, 89	IOVDD	PWR	Input and Output Supply. The voltage on this pin sets the highest input voltage that should be present on the digital input pins. This pin is also the supply for the digital output signals on the clock, data, control port, and MP pins. IOVDD should always be set to 3.3 V. The current draw of this pin is variable because it is dependent on the loads of the digital outputs.
3	BCLK3	D_IO	Bit Clock, Input/Output Clock Domain 3. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 3 is set up as a master or slave. When not used, this pin can be left disconnected.
4	LRCLK3	D_IO	Frame Clock, Input/Output Clock Domain 3. This pin is bidirectional, with the direction depending on whether the Input/Output Clock Domain 3 is set up as a master or slave. When not used, this pin can be left disconnected.
5	SDATA_IN2	D_IN	Serial Data Port 2 Input. When not used, this pin can be left disconnected.

Pin No.	Mnemonic	Type[1]	Description
34	MP6	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
35	MP5	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
36	MP4	D_IO	Multipurpose, General-Purpose Input/Output. When not used, this pin can be left disconnected.
40	VDRIVE	A_OUT	Regulator Drive. Supplies the drive current for the 1.8 V regulator. The base of the voltage regulator's external PNP transistor is driven from VDRIVE.
41	XTALO	A_OUT	Crystal Oscillator Output. A 100 Ω damping resistor should be connected between this pin and the crystal. This output should not be used to directly drive a clock to another IC; the CLKOUT pin exists for this purpose. If the crystal oscillator is not used, the XTALO pin can be left unconnected.
42	XTALI	A_IN	Crystal Oscillator Input. This pin provides the master clock for the ADAU1442/ADAU1445/ADAU1446. If the ADAU1442/ADAU1445/ADAU1446 generate the master clock in the system, this pin should be connected to the crystal oscillator circuit. If the ADAU1442/ADAU1445/ADAU1446 are slaves to an external master clock, this pin should be connected to the master clock signal generated by another IC.
43	PLL_FILT	A_OUT	Phase-Locked Loop Filter. Two capacitors and a resistor must be connected to this pin as shown in Figure 11.
44	PVDD	PWR	Phase-Locked Loop Supply. Provides the 3.3 V power supply for the PLL. This should be decoupled to PGND with a100 nF capacitor.
45	PGND	PWR	Phase-Locked Loop Ground. Ground for the PLL supply. The AGND, DGND, and PGND pins can be tied directly together in a common ground plane. PGND should be decoupled to PVDD with a 100 nF capacitor.
46	SPDIFI	D_IN	S/PDIF Input. Accepts digital audio data in the S/PDIF format. When not used, this pin can be left disconnected.
47	SPDIFO	D_OUT	S/PDIF Output. Outputs digital audio data in the S/PDIF format. When not used, this pin can be left disconnected.
48	AVDD	PWR	Analog Supply. 3.3 V analog supply for the auxiliary ADC. This pin should be decoupled to AGND with a 100 nF capacitor.
49	AGND	PWR	Analog Ground. Ground for the analog supply. This pin should be decoupled to AVDD with a 100 nF capacitor.
53	CLKOUT	D_OUT	Master Clock Output. Used to output a master clock to other ICs in the system. Set using the CLKMODEx pins. When not used, this pin can be left disconnected.
54	$\overline{\text{RESET}}$	D_IN	Reset. Active-low reset input. Reset is triggered on a high-to-low edge and exited on a low-to-high edge. For detailed information about initialization, see the Power-Up Sequence section. A reset event sets all RAMs and registers to their default values.
55	MP3/ADC3	D_IO, A_IN	Multipurpose, General-Purpose Input or Output/Auxiliary ADC Input 3. When not used, this pin can be left disconnected.
56	MP2/ADC2	D_IO, A_IN	Multipurpose, General-Purpose Input or Output/Auxiliary ADC Input 2. When not used, this pin can be left disconnected.
57	MP1/ADC1	D_IO, A_IN	Multipurpose, General-Purpose Input or Output/Auxiliary ADC Input 1. When not used, this pin can be left disconnected.
58	MP0/ADC0	D_IO, A_IN	Multipurpose, General-Purpose IO/Auxiliary ADC Input 0. When not used, this pin can be left disconnected.
59	PLL1	D_IN	Phase-Locked Loop Mode Select Pin 1.
60	PLL0	D_IN	Phase-Locked Loop Mode Select Pin 0.
61	SDATA_OUT8	D_OUT	Serial Data Port 0 Output. When not used, this pin can be left disconnected.
64	BCLK11	D_IO	Bit Clock, Output Clock Domain 11. This pin is bidirectional, with the direction depending on whether the Output Clock Domain 11 is set up as a master or slave. When not used, this pin can be left disconnected.
65	LRCLK11	D_IO	Frame Clock, Output Clock Domain 11. This pin is bidirectional, with the direction depending on whether the Output Clock Domain 11 is set up as a master or slave. When not used, this pin can be left disconnected.

THEORY OF OPERATION

SYSTEM BLOCK DIAGRAM



*SPI/I2C = THE ADDR0, CLATCH, SCL/CCLK, SDA/COUT, AND ADDR1/CDATA PINS.
†THERE ARE 12 BIT CLOCKS (BCLK[11:0]) AND 12 FRAME CLOCKS (LRCLK[11:0]) IN TOTAL. OF THE 12 CLOCKS, SIX ARE ASSIGNABLE, THREE MUST BE OUTPUTS, AND THREE MUST BE INPUTS.

07696-008

Figure 8. System Block Diagram

OVERVIEW

The ADAU1442/ADAU1445/ADAU1446 are each a 24-channel audio DSP with an integrated S/PDIF receiver and transmitter, flexible serial audio ports, up to 16 channels of asynchronous sample rate converters (ASRCs), flexible audio routing, and user interface capabilities. Signal processing capabilities include equalization, crossover, bass enhancement, multiband dynamics processing, delay compensation, speaker compensation, and stereo image widening. These algorithms can be used to compensate for the real-world limitations of speakers, amplifiers, and listening environments, resulting in an improvement in the perceived audio quality.

An on-board oscillator can be connected to an external crystal to generate the master clock. A phase-locked loop (PLL) allows the ADAU1442/ADAU1445/ADAU1446 to be clocked from a variety of clock frequencies. The PLL can accept inputs of 64 × f_S, 128 × f_S, 256 × f_S, 384 × f_S, or 512 × f_S to generate the internal master clock of the core, where f_S is the sampling rate of audio in normal-rate processing mode. In dual- or quad-rate mode, these multipliers are halved or quartered, respectively. System sample rates include, but are not limited to, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, and 192 kHz.

Each ADAU1442/ADAU1445/ADAU1446 operates from a 1.8 V digital power supply and a 3.3 V analog supply. An on-board voltage regulator can be used to operate the chip from a single 3.3 V supply.

The ADAU1442/ADAU1445/ADAU1446 have a sophisticated control port that supports complete read and write capability of all memory locations, excluding read-only addresses. Control registers are provided to offer complete control of the chip's configuration and serial modes. Handshaking is included for ease of memory uploads and downloads. The ADAU1442/ADAU1445/ADAU1446 can be configured for either SPI or I²C control. Program RAM, parameter RAM, and register contents can be saved in an external EEPROM, from which the ADAU1442/ADAU1445/ADAU1446 can self-boot on startup.

The ADAU1442/ADAU1445/ADAU1446 serial ports operate with digital audio I/Os in the I²S, left-justified, right-justified, or TDM-compatible mode. The flexible serial data ports allow for direct interconnection to a variety of ADCs, DACs, and general-purpose DSPs. The combination of an on-board S/PDIF transmitter and receiver and 16 channels of ASRCs allows for easy compatibility with an extensive number of external devices, and a system with up to nine sampling rates.

The flexible audio routing matrix (FARM) is a system of multiplexers used to distribute the audio signals in the ADAU1442/ADAU1445/ADAU1446 among the serial inputs and outputs, audio core, and ASRCs. FARM can easily be configured by setting the appropriate registers.

The ADAU1442, ADAU1445, and ADAU1446 are distinguished by the number of on-board ASRCs and maximum sample rates. The ADAU1442 contains eight 2-channel ASRCs, the ADAU1445 contains two 8-channel ASRCs, and the ADAU1446 has no ASRCs.

Two sets of serial ports at the input and output can operate in a special flexible TDM mode, which allows the user to independently assign byte-specific locations to audio streams at varying bit depths. This mode ensures compatibility with codecs using similar flexible TDM streams.

The core of the ADAU1442/ADAU1445/ADAU1446 is a 28-bit DSP (or a 56-bit DSP when using double-precision mode) optimized for audio processing, and it can process audio at sample rates of up to 192 kHz. The program and parameter RAMs can be loaded with a custom audio processing signal flow built with the SigmaStudio graphical programming software from Analog Devices, Inc. The values stored in the parameter RAM control individual signal processing blocks, such as IIR and FIR equalization filters, dynamics processors, audio delays, and mixer levels. A software safeload feature allows for transparent parameter updates and prevents clicks on the output signals.

Reliability features such as a CRC and program counter watchdog help ensure that the system can detect and recover from any errors related to memory corruption.

S/PDIF signals can be routed through an ASRC for processing in the DSP or can be sent directly to output on MP pins for recovery of the embedded audio signal. Other components of the embedded signal, including status and user bits, are not lost and can be output on the MP pins as well.

Multipurpose (MP) pins are available for providing a simple user interface without the need for an external microcontroller. Twelve pins are available to input external control signals and output flags or controls to other devices in the system. Four of these can alternatively be assigned to an auxiliary ADC for use with analog controls such as potentiometers or system voltages. As inputs, MP pins can be connected to push buttons, switches, rotary encoders, potentiometers, or other external control circuitry to control the internal signal processing program. When configured as outputs, these pins can be used to drive LEDs (with a buffer), to output flags to a microcontroller, to control other ICs, or to connect to other external circuitry in an application.

The SigmaStudio software is used to program and control the ADAU1442/ADAU1445/ADAU1446 through the control port. Along with designing and tuning a signal flow, the software can configure all of the DSP registers in real time and download a new program and parameter into the external self-boot EEPROM. SigmaStudio's easy-to-use graphical interface allows anyone with audio processing knowledge to easily design a DSP signal flow and port it to a target application without the need for writing line-level code. At the same time, the software provides enough flexibility and programmability for an experienced DSP programmer to have in-depth control of the design. In SigmaStudio, the user can add signal processing cells from the library by dragging and dropping cells, connect them together in a flow, compile the design, and load the program and parameter files into the ADAU1442/ADAU1445/ADAU1446 memory through the control port. The complicated tasks of linking, compiling, and downloading the project are all handled automatically by the software.

INITIALIZATION

Power-Up Sequence

The ADAU1442/ADAU1445/ADAU1446 have a built-in initialization period, which allows sufficient time for the PLL to lock and the registers to initialize their values. On a positive edge of $\overline{\text{RESET}}$, the PLL settings are immediately set by the PLL0, PLL1, and PLL2 pins, and the master clock signal is blocked from the chip subsystems. The initialization time, which is measured from the rising edge of $\overline{\text{RESET}}$, is dependent on the frequency of the signal input to the XTALI pin, or f_{XTALI}. The total initialization time is

$$1/(f_{XTALI}/D) \times 2^{15} \text{ sec}$$

where D is the PLL divider, as set by the PLL0, PLL1, and PLL2 pins. The PLL divider settings are described in Table 9.

For example, if the signal input to XTALI has a frequency of 12.288 MHz and the PLL divider is set to 4 (PLL = 0, PLL1 = 1, and PLL2 = 0), the initialization time lasts

$$1/(12288000/4) \times 2^{15} \text{ sec} = 0.010667 \text{ sec (or 10.667 ms)}$$

New values should not be written via the control port until the initialization is complete.

Table 8 shows some typical times to boot the ADAU1442/ADAU1445/ADAU1446 into the operational state necessary for an application, assuming that a 400 kHz I²C clock or a 5 MHz SPI clock is used and a full program, parameter set, and all registers (9 kB) are loaded. In reality, most applications use less than this full amount, and unused program and parameter RAM need not be initialized; therefore, the total boot time may be shorter.

Recommended Program/Parameter Loading Procedure

When writing large amounts of data to the program or parameter RAM in direct write mode, such as when downloading the initial contents of the RAMs from an external memory, the processor core should be disabled to prevent unpleasant noises from appearing at the audio output. When small amounts of data are transmitted during real-time operation of the DSP, such as when updating individual parameters, the software safeload mechanism can be used. More information is available in the Software Safeload section.

Power-Reduction Modes

Sections of the ADAU1442/ADAU1445/ADAU1446 chips can be turned on and off as needed to reduce power consumption. These include the ASRCs, S/PDIF receiver and transmitter, auxiliary ADCs, and DSP core. More information is available in the Master Clock and PLL Modes and Settings section.

System Initialization Sequence

Before the IC can process audio in the DSP, the following initialization sequence must be completed. (Step 5 through Step 11 can be performed in any order, as needed.)

1. Power on the IC and bring it out of reset. The order of the power supplies (DVDD, IOVDD, and AVDD) does not matter.
2. Wait at least 10.667 ms for the initialization to complete if the XTALI input is 12.288 MHz and the PLL divider is set to 4 (see the Power-Up Sequence section for information about calculating the initialization time if another f_{XTALI} is used).
3. Enable the master clocks of all modules to be used (see the Master Clock and PLL Modes and Settings section).
4. Set the DSP core rate select register (0xE220) to 0x001C. This disables the start pulse to the core.
5. Deassert the core run bit (see the DSP Core Modes and Settings section).
6. Set the serial input modes (see the Serial Input Port Modes Registers (Address 0xE000 to Address 0xE008) section).
7. Set the serial output modes (see the Serial Output Port Modes Registers (Address 0xE040 to Address 0xE049) section).
8. Set the routing matrix modes (see details of Address 0xE080 to Address 0xE09B in the Flexible Audio Routing Matrix Modes section).
9. Write the parameter RAM (Address 0x0000 to Address 0x0FFF).
10. Write the program RAM (Address 0x2000 to Address 0x2FFF).
11. Write the nonmodulo data RAM (Addresses vary based on the SigmaStudio project file).
12. Write all other necessary control registers, such as ASRCs and S/PDIF (Address 0xE221 to Address 0xE24C).
13. Set the DSP core rate select register (0xE220) to the desired value. This enables the start pulse to the core. Table 12 contains a list of valid settings.
14. Assert the core run bit (see the DSP Core Modes and Settings section).

Table 8. Power-Up Time

PLL Lock Time (ms) (f_{XTALI} = 12.288 MHz, PLL Divider = 4)	Approximate Boot Time; Loading Maximum Program/Parameter/Registers (ms)			
	I²C (at 400 kHz SCL)	SPI (at 5 MHz CCLK)	SPI (at 25 MHz CCLK)	Total (ms)
10.667	25	2	0.4	11.067 to 35.667

Table 9. PLL Modes

DSP Core Rate[1]	Input to MCLK (XTALI Pin)	PLL2	PLL1	PLL0	PLL Divider[2]	Core Clock Multiplier	Core Clock (f_{CORE})	Instructions per Sample
Normal	64 × $f_{S,NORMAL}$	0	0	0	1	56	3584 × $f_{S,NORMAL}$	3584
	128 × $f_{S,NORMAL}$	0	0	1	2	56	3584 × $f_{S,NORMAL}$	3584
	256 × $f_{S,NORMAL}$	0	1	0	4	56	3584 × $f_{S,NORMAL}$	3584
	384 × $f_{S,NORMAL}$	0	1	1	6	56	3584 × $f_{S,NORMAL}$	3584
	512 × $f_{S,NORMAL}$	1	0	0	8	56	3584 × $f_{S,NORMAL}$	3584
Dual	32 × $f_{S,DUAL}$	0	0	0	1	56	1792 × $f_{S,DUAL}$	1792
	64 × $f_{S,DUAL}$	0	0	1	2	56	1792 × $f_{S,DUAL}$	1792
	128 × $f_{S,DUAL}$	0	1	0	4	56	1792 × $f_{S,DUAL}$	1792
	192 × $f_{S,DUAL}$	0	1	1	6	56	1792 × $f_{S,DUAL}$	1792
	256 × $f_{S,DUAL}$	1	0	0	8	56	1792 × $f_{S,DUAL}$	1792
Quad	16 × $f_{S,QUAD}$	0	0	0	1	56	896 × $f_{S,QUAD}$	896
	32 × $f_{S,QUAD}$	0	0	1	2	56	896 × $f_{S,QUAD}$	896
	64 × $f_{S,QUAD}$	0	1	0	4	56	896 × $f_{S,QUAD}$	896
	96 × $f_{S,QUAD}$	0	1	1	6	56	896 × $f_{S,QUAD}$	896
	128 × $f_{S,QUAD}$	1	0	0	8	56	896 × $f_{S,QUAD}$	896

[1] If the normal DSP core rate ($f_{S,NORMAL}$) is 44.1 kHz, the dual DSP core rate ($f_{S,DUAL}$) is 88.2 kHz, and the quad DSP core rate ($f_{S,QUAD}$) is 176.4 kHz. Likewise, if $f_{S,NORMAL}$ is 48 kHz, then $f_{S,DUAL}$ is 96 kHz and $f_{S,QUAD}$ is 192 kHz.
[2] The PLL divider is set by the PLLx pins.

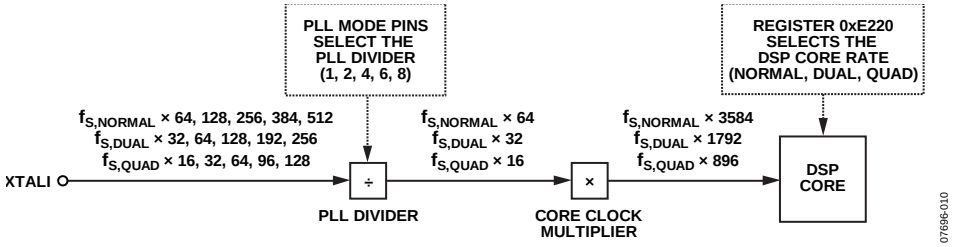


Figure 10. Master Clock Signal Flow

CONTROL PORT

Overview

The ADAU1442/ADAU1445/ADAU1446 can operate in one of three control modes: I²C control mode, SPI control mode, or self-boot mode (no external controller).

The ADAU1442/ADAU1445/ADAU1446 have both a 4-wire SPI control port and a 2-wire I²C bus control port. Each can be used to set the RAMs and registers. When the SELFBOOT pin is low at power-up, the chip defaults to I²C mode but can be put into SPI control mode by pulling Pin CLATCH low three times. When the SELFBOOT pin is set high at power-up, the ADAU1442/ADAU1445/ADAU1446 load the program, parameters, and register settings from an external EEPROM at startup.

The control port is capable of full read and write operations for all memories and registers, except for those that are read only. Most signal processing parameters are controlled by writing new values to the parameter RAM using the control port. Other functions, such as mute and input/output mode control, are programmed by writing to the registers.

All addresses can be accessed in either a single-word mode or a burst mode. A control word consists of the chip address, the register/RAM subaddress, and the data to be written. The number of bytes per word depends on the type of data that is being written.

The first byte (Byte 0) of a control word contains the 7-bit chip address plus the R/$\overline{W}$ bit. The next two bytes (Byte 1 and Byte 2) together form the subaddress of the memory or register location within the ADAU1442/ADAU1445/ADAU1446. This subaddress must be two bytes because the memory locations within the ADAU1442/ADAU1445/ADAU1446 are directly addressable, and their sizes exceed the range of single-byte addressing. All subsequent bytes (starting with Byte 3) contain the data, such as control port data, program data, or parameter data. The exact formats for specific types of writes are shown in Figure 13 and Figure 19.

The ADAU1442/ADAU1445/ADAU1446 have several mechanisms for updating signal processing parameters in real time without causing pops or clicks in the output. In cases where large blocks of data must be downloaded, the output of the DSP core can be halted, new data can be loaded, and then the output of the DSP core can be restarted. This is typically done during the booting sequence at startup or when loading a new program into RAM. In cases where only a few parameters must be changed, they can be loaded without halting the program. A software-based safeload mechanism is included for this purpose, and it can be used to buffer a full set of parameters (for example, the five coefficients of a biquad) and then transfer these parameters into the active program within one audio frame.

The control port pins are multifunctional according to the mode in which the part is operating. Table 16 details these functions.

I²C Port

The ADAU1442/ADAU1445/ADAU1446 support a 2-wire serial (I²C-compatible) microprocessor bus driving multiple peripherals. Two pins, serial data (SDA) and serial clock (SCL), carry information between the ADAU1442/ADAU1445/ADAU1446 and the system I²C master controller. In I²C mode, the ADAU1442/ADAU1445/ADAU1446 are always slaves on the bus, which means that the parts cannot initiate a data transfer.

Each slave device is recognized by a unique address. The address bit sequence is shown in Table 13. The ADAU1442/ADAU1445/ADAU1446 have eight possible slave addresses: four for writing operations and four for reading. These are unique addresses for the device and are listed in Table 14.

Users can communicate with these addresses by using the USBi communication channel list in the hardware configuration tab of SigmaStudio. The LSB of the byte sets either a read or write operation; Logic Level 1 corresponds to a read operation, and Logic Level 0 corresponds to a write operation. Address Bit 5 and Address Bit 6 are set by tying the ADDRx pins of the ADAU1442/ADAU1445/ADAU1446 to Logic Level 0 or Logic Level 1. Both SDA and SCL should have pull-up resistors on the lines connected to them (a standard value is 2.0 kΩ, but this can be changed depending on the capacitive load on the line). The voltage on these signal lines should not be greater than the voltage of IOVDD (3.3 V).

Table 13. ADAU1442/ADAU1445/ADAU1446 Address Bit Sequence

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	1	1	1	0	ADDR1	ADDR0	R/$\overline{W}$

Table 14. ADAU1442/ADAU1445/ADAU1446 I²C Slave Addresses

ADDR1	ADDR0	Read/Write[1]	Slave Address
0	0	0	0x70
0	0	1	0x71
0	1	0	0x72
0	1	1	0x73
1	0	0	0x74
1	0	1	0x75
1	1	0	0x76
1	1	1	0x77

[1] 0 = write, 1 = read.

Addressing

Initially, all devices on the I²C bus are in an idle state, in which the devices monitor the SDA and SCL lines for a start condition and the proper address. The I²C master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address or an address and data stream follow. All devices on the bus respond to the start condition and shift the next eight bits (7-bit address + R/$\overline{W}$ bit) MSB first. The device that recognizes the transmitted

Serial Clock Domains

There are 12 clock domains (pairs of LRCLKx and BCLKx pins) available in the ADAU1442/ADAU1445/ADAU1446. Of these, three are available exclusively to the serial data input ports, three are available exclusively to the serial data output ports, and the remaining six can be assigned to clock either input or output ports.

The ADAU1442 contains eight 2-channel ASRCs and the ADAU1445 contains two 8-channel ASRCs, whereas the ADAU1446 contains no ASRCs. However, all clock domain pins are available on every device. In a system with no sample rate conversion and with serial ports in slave mode, at least two pairs of LRCLKx and BCLKx pins must be connected: one pair for the input serial ports and one pair for the output serial ports. If all serial ports are in master mode and synchronous, then only one pair of LRCLKx and BCLKx pins needs to be connected.

Figure 27 shows a simplified view of the assignment of clock domains to the input and output sides of the chip. Note that each clock domain comprises two signals, namely the BCLK (bit clock) and LRCLK (frame clock). Therefore, the 12 clock domains contain a total of 24 clock signals.

Each clock domain is capable of acting as a master or slave. For this reason, all LRCLK and BCLK pins are bidirectional. In slave mode, the LRCLK and BCLK pins receive clock signals from an external source, such as a codec. In master mode, the LRCLK and BCLK pins output clock signals to external slave ICs.

Although a clock domain in slave mode can clock an arbitrary number of serial ports, a clock domain in master mode can only clock a single serial port. For Clock Domains[2:0] and Clock Domains[11:9], the corresponding serial port is fixed as an input or output. For assignable clock domains (Clock Domains[8:3]), the corresponding serial port can be either an input or output, depending on the setting of the clock pad multiplexer register (see Table 20 for more details).

Table 20. Master Mode Clock Domain Assignment

Clock Domain	Chip Pins	Serial Port
0	LRCLK0, BCLK0	SDATA_IN0
1	LRCLK1, BCLK1	SDATA_IN1
2	LRCLK2, BCLK2	SDATA_IN2
3	LRCLK3, BCLK3	SDATA_IN3 or SDATA_OUT3[1]
4	LRCLK4, BCLK4	SDATA_IN4 or SDATA_OUT4[1]
5	LRCLK5, BCLK5	SDATA_IN5 or SDATA_OUT5[1]
6	LRCLK6, BCLK6	SDATA_IN6 or SDATA_OUT6[1]
7	LRCLK7, BCLK7	SDATA_IN7 or SDATA_OUT7[1]
8	LRCLK8, BCLK8	SDATA_IN8 or SDATA_OUT8[1]
9	LRCLK9, BCLK9	SDATA_OUT0
10	LRCLK10, BCLK10	SDATA_OUT1
11	LRCLK11, BCLK11	SDATA_OUT2

[1] Depends on the setting of the clock pad multiplexer register (Address 0xE240).

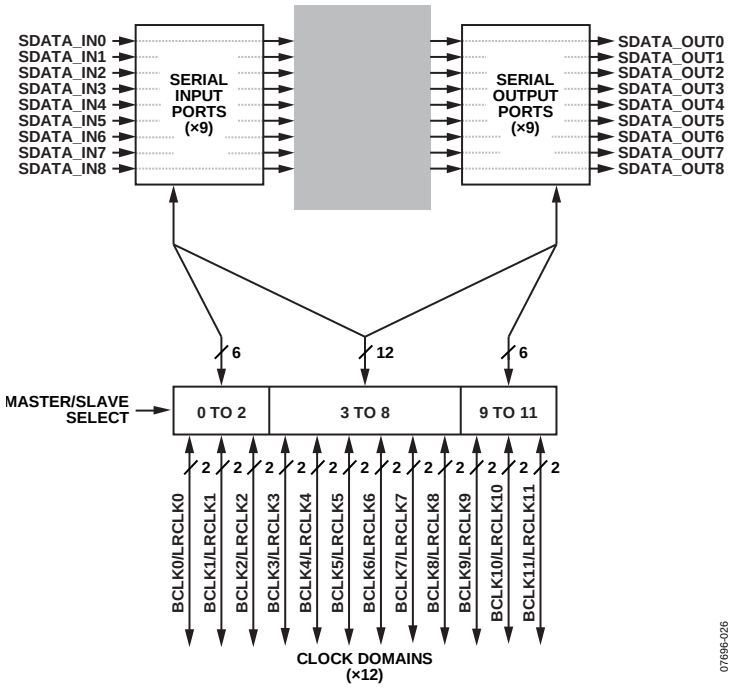


Figure 27. Simplified Serial Clock Domain Assignment

Packed TDM4 Mode

A special TDM mode is available that allows four channels to be fit into a space of 64 bit clock cycles. This mode is called packed TDM4 mode, or MOST™ mode. MOST (Media Oriented Systems Transport) is a networking standard intended for interconnecting multimedia components in automobiles and other vehicles. Many ICs intended to interface with a MOST bus use a packed TDM4 data format.

For this mode to be used, the serial port must be set up with the following register settings:

- Packed TDM4 mode
- Left-justified or delay by 1
- Word length of 16 bits

See Figure 29 for a timing diagram of the packed TDM4 mode. This figure is shown with a negative BCLK polarity, a negative LRCLK polarity, and an MSB delay of 1.

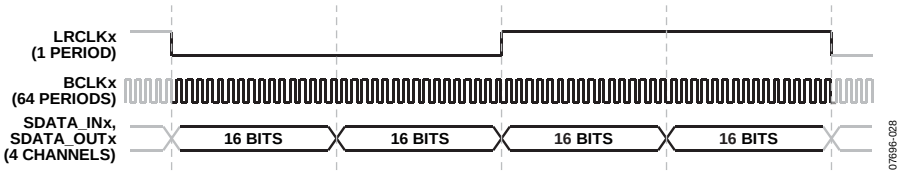


Figure 29. Packed TDM4 Mode

SERIAL INPUT PORTS

The serial input ports convert standard I2S and TDM signals into 16-, 20-, and 24-bit audio signals for input to the audio processor. They support TDM2, TDM4, TDM8, and TDM16 time division multiplexing schemes and I²S, left-justified, right-justified, MSB delay-by-12 and delay-by-16 modes. Different clock polarities and multiple word lengths are supported, as well as the capability to drive in master mode or to be driven in slave mode.

The serial input ports are composed of up to nine clock domains (Clock Domain 0 to Clock Domain 8) and up to nine serial data signals (SDATA_IN0 to SDATA_IN8).

In slave mode, the nine serial input clock domains are driven directly from the corresponding nine pairs of LRCLKx and BCLKx pins on the IC. Three pairs of LRCLKx and BCLKx pins (LRCLK[2:0] and BCLK[2:0]) are hardwired to Clock Domains[2:0], which are serial inputs. The remaining six pairs of LRCLKx and BCLKx pins (LRCLK[8:3] and BCLK[8:3]) are multiplexed to Clock Domains[8:3] as either inputs or outputs. The multiplexer can be set to use these signals as input clock domains by writing to Bits[5:0] of the clock pad multiplexer register (Address 0xE240) as explained in Table 23. This configuration is also valid in master mode.

Figure 30 shows in more detail how the clocks are routed to and from the serial input ports. For the assignable clock domains (Clock Domains[8:3]), the clock pad multiplexer allows them to be routed either to the serial input ports or to the serial output ports independently. In slave mode, the clock domain selector (that is, the 18:2 multiplexer) allows each serial input port to clock from any available clock domain. In master mode, the clock domain selector is bypassed, and the assignments described in Table 24 are used.

The maximum number of audio channels that can be input to SigmaDSP is 24. The serial input ports must be set in a way that respects this (for example, two TDM16 streams is not a valid entry).

Table 23. Input Clock Domain Multiplexing

Clock Domain	Chip Pins	Register 0xE240 Setting
0	LRCLK0, BCLK0	N/A
1	LRCLK1, BCLK1	N/A
2	LRCLK2, BCLK2	N/A
3	LRCLK3, BCLK3	Set Bit 0 to 0
4	LRCLK4, BCLK4	Set Bit 1 to 0
5	LRCLK5, BCLK5	Set Bit 2 to 0
6	LRCLK6, BCLK6	Set Bit 3 to 0
7	LRCLK7, BCLK7	Set Bit 4 to 0
8	LRCLK8, BCLK8	Set Bit 5 to 0

Table 24. Input Clock Domain Assignments in Master Mode

Data Pin	Clock Pins
SDATA_IN0	LRCLK0, BCLK0
SDATA_IN1	LRCLK1, BCLK1
SDATA_IN2	LRCLK2, BCLK2
SDATA_IN3	LRCLK3, BCLK3
SDATA_IN4	LRCLK4, BCLK4
SDATA_IN5	LRCLK5, BCLK5
SDATA_IN6	LRCLK6, BCLK6
SDATA_IN7	LRCLK7, BCLK7
SDATA_IN8	LRCLK8, BCLK8

selector (that is, the 18:2 multiplexer) allows each serial output port to clock from any available clock domain. In master mode, the clock domain selector is bypassed, and the assignments described in Table 28 are used.

Table 28. Output Clock Domain Assignments in Master Mode

Data Pin	Clock Pins
SDATA_OUT0	LRCLK9, BCLK9
SDATA_OUT1	LRCLK10, BCLK10
SDATA_OUT2	LRCLK11, BCLK11
SDATA_OUT3	LRCLK3, BCLK3
SDATA_OUT4	LRCLK4, BCLK4
SDATA_OUT5	LRCLK5, BCLK5
SDATA_OUT6	LRCLK6, BCLK6
SDATA_OUT7	LRCLK7, BCLK7
SDATA_OUT8	LRCLK8, BCLK8

The maximum number of audio channels that can be output from SigmaDSP is 24. The serial output ports must be set in a way that respects this (for example, two TDM16 streams is not a valid entry).

All data is processed in twos complement, MSB-first format, and the left channel always precedes the right channel.

SERIAL OUTPUT PORT MODES AND SETTINGS

Each of the nine serial output ports is controlled by setting an individual 2-byte word in the serial output mode register for each port (see Table 29 for the register addresses). Each serial data signal can be set to use any of the nine clock domains (slave mode) or an internally generated LRCLK signal at $f_{S,NORMAL}$, $f_{S,DUAL}$, or $f_{S,QUAD}$. The default value for each serial port on reset is set to TDM2, I²S, 24-bit, negative LRCLK and BCLK polarity slave mode using a 50% duty cycle LRCLK clock signal (as opposed to a synchronization pulse). This configuration corresponds to a setting of 0x3C00. The serial data uses its corresponding clock domain (for example, SDATA3 uses LRCLK3 and BCLK3).

Restrictions

When the device is in MOST mode, the MSB position of the serial data is delayed by one bit clock from the start of the frame (I²S position) and the data width is restricted to 16 bits.

When the device is in MSB delay-by-12 mode, the serial data can be 16 or 20 bits wide (not 24 bits). When the device is in MSB delay-by-16 mode, the serial data can only be 16 bits wide.

For information on TDM capabilities, refer to Table 18.

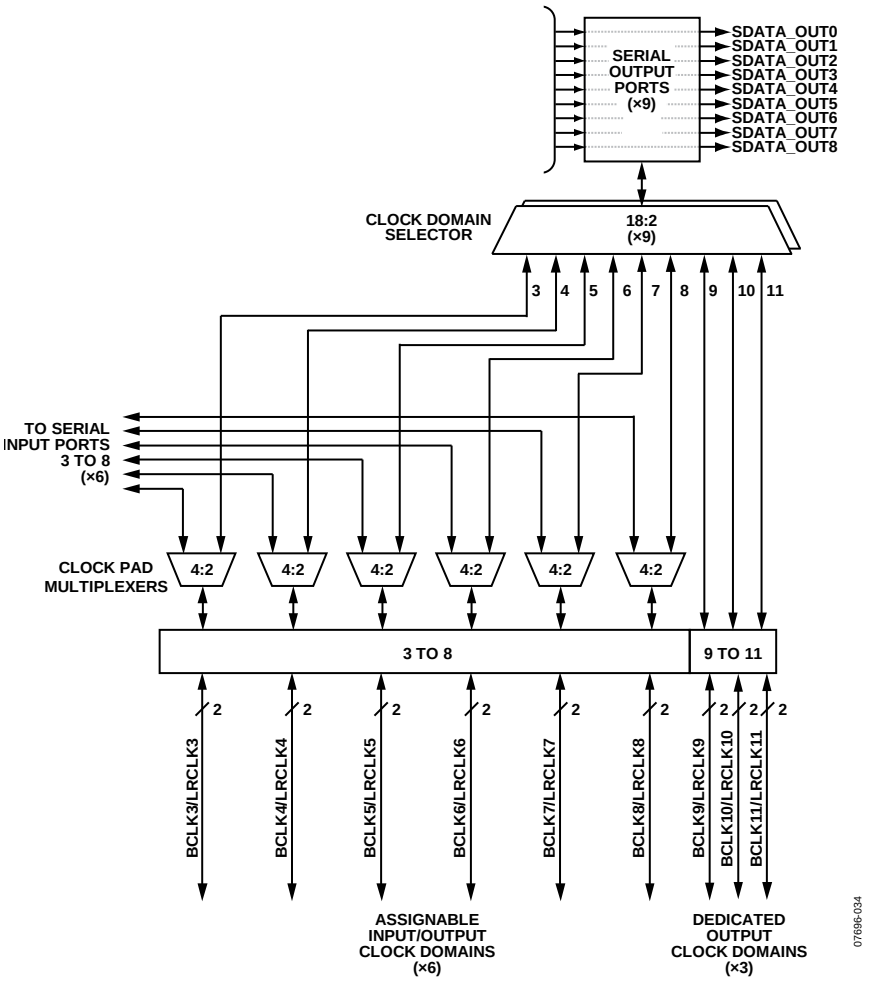


Figure 33. Output Serial Port Clock Multiplexing

Serial Output Data Selector Bits (Bits[5:0])

These bits select where each of the 12 stereo serial output channels comes from. The channels can come either from one of the 12 DSP core stereo outputs or from one of the eight ASRC stereo outputs.

In the case of the ADAU1446, setting the serial output data selector bits to a value corresponding to an ASRC output pair yields no data.

As shown in Figure 50, the stereo output pairs can come from any of the DSP serial or ASRC outputs.

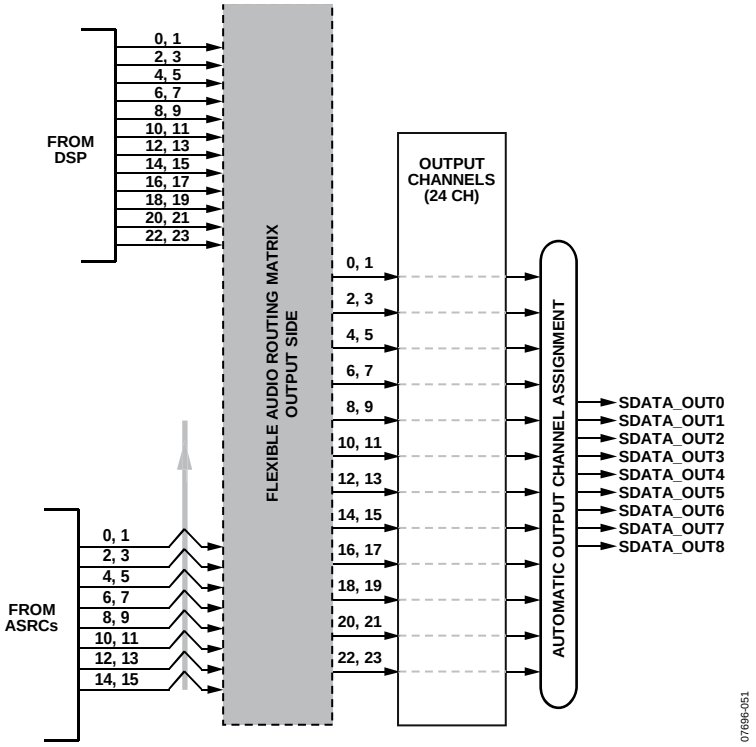


Figure 50. Serial Output Select Pair

Auxiliary Outputs—Set Enable Mode Register (Address 0xE0C8)

Table 59. Bit Descriptions of Register 0xE0C8

Bit Position	Description	Default
[15:2]	Reserved	
[1:0]	Auxiliary outputs enable mode 00 = auxiliary outputs are always off. 01 = auxiliary outputs are always on. 10 = auxiliary outputs are off on reset. (They switch on as soon as the hot enable bit is 1 and switch off as soon as the S/PDIF lock bit is 0.)	01

This register controls when the S/PDIF stream is active on the multipurpose pins when the S/PDIF to I²S mode is active. For more information, see the Enable S/PDIF to I²S Output section.

Setting Bits[1:0] of Register 0xE0C8 to 10 (auxiliary outputs are off on reset) is useful for situations in which the S/PDIF stream may be interrupted unexpectedly. An interruption causes the S/PDIF lock bit to go low, which in turn disables the auxiliary outputs. When the S/PDIF stream is recovered, the hot enable bit must be activated to restore the auxiliary outputs (see the Set Hot Enable Register (Address 0xE0CA) section for more information).

S/PDIF Lock Bit Detection Register (Address 0xE0C9)

Table 60. Bit Descriptions of Register 0xE0C9

Bit Position	Description
[15:1]	Reserved
0	S/PDIF input lock bit (read only) 0 = no valid input stream 1 = successful lock to input stream

This read-only register shows the status of the S/PDIF input lock bit.

Set Hot Enable Register (Address 0xE0CA)

Table 61. Bit Descriptions of Register 0xE0CA

Bit Position	Description	Default
[15:1]	Reserved	
0	Hot enable bit 0 = hot enable inactive 1 = hot enable active	0

This register allows the hot enable bit to be set, which restarts the auxiliary outputs when they are configured so that the auxiliary outputs are off on a reset (that is, Bits[1:0] of Register 0xE0C8 are set to 10). The hot enable bit is set to 0 automatically in the event that the S/PDIF receiver loses lock. For more information, see the Auxiliary Outputs—Set Enable Mode Register (Address 0xE0C8) section.

Read Enable Auxiliary Output Register (Address 0xE0CB)

Table 62. Bit Descriptions of Register 0xE0CB

Bit Position	Description
[15:1]	Reserved
0	Read enable auxiliary output (read only) 0 = S/PDIF auxiliary outputs disabled 1 = S/PDIF auxiliary outputs enabled

This read-only register shows the status of the S/PDIF auxiliary outputs.

S/PDIF Loss-of-Lock Behavior Register (Address 0xE0CC)

Table 63. Bit Descriptions of Register 0xE0CC

Bit Position	Description	Default
[15:1]	Reserved	
0	S/PDIF loss-of-lock behavior 0 = S/PDIF disable on loss of lock 1 = S/PDIF ignore loss of lock	0

This register controls the behavior of the S/PDIF receiver in the event of a loss of lock to the input stream. A loss of lock can arise when there is severe noise or jitter on the S/PDIF input stream, rendering it unrecognizable to the receiver. In the default mode, such an event disables the S/PDIF receiver, causing it to stop outputting frame sync pulses. This in turn causes the target ASRC to be muted. Frame sync pulses do not resume until lock is regained.

When the register is set to 1, the S/PDIF receiver always outputs frame sync pulses, even if the integrity of the S/PDIF stream is compromised and the audio samples cannot be recovered. In such a case, the S/PDIF receiver data output remains at 0 until lock is regained.

The S/PDIF receiver is robust and can recover streams with integrity well below the standards of the AES/EBU specification. Therefore, even in cases of extreme signal degradation, this register should be used only when audio recovery is required. In general, a loss-of-lock event is much shorter than an ASRC mute or unmute ramp.

AUXILIARY ADC

The ADAU1442/ADAU1445/ADAU1446 include a 10-bit auxiliary ADC that can be used for control input signals. There is one ADC with four multiplexed inputs. The ADC samples at a rate of f_{CORE}/896 (192 kHz when based on a 172.032 MHz core clock), which results in an effective sampling rate of f_{CORE}/3584 (48 kHz when based on a 172.032 MHz core clock) per channel.

An ADC filtering function is included in the hardware, and hysteresis is available to reduce the effects of noise on the input. More information on these settings is available in Table 70.

The auxiliary ADC is not designed for audio and, therefore, should not be used as an auxiliary audio input. The sample and bit rates are too low to convert signals for audio applications.

The input can be filtered using several methods. The specific filtering modes can be set as described in Table 70.

AUXILIARY ADC MODES AND SETTINGS

ADC Filter Mode Register (Address 0xE224)

Table 69. Bit Descriptions of Register 0xE224

Bit Position	ADC Channel
[15:8]	Reserved
[7:6]	ADC0
[5:4]	ADC1
[3:2]	ADC2
[1:0]	ADC3

Table 70. Settings of Bits[7:0], Register 0xE224

Mode Setting	Function	Default
00	Filter bypass	00
01	ADC data filtered	
10	Filtered with 1-bit hysteresis	
11	Filtered with 2-bit hysteresis	

INTERFACING WITH OTHER DEVICES

When interfacing the ADAU1442/ADAU1445/ADAU1446 to other devices in the system, it may be necessary to set the drive strength of each pin.

DRIVE STRENGTH MODES AND SETTINGS

Bit Clock Pad Strength Register (Address 0xE247)

This register controls the pad drive strength of all bit clock pins configured in master mode. The default 2 mA setting should be adequate for most applications. The 6 mA setting should be used only when the integrity of the signal is compromised.

Table 71. Bit Descriptions of Bit Clock Pad Strength Register

Bit Position	Description	Default
[15:12]	Reserved	
11	BCLK11 0 = low strength (2 mA) 1 = high strength (6 mA)	0
10	BCLK10 0 = low strength (2 mA) 1 = high strength (6 mA)	0
9	BCLK9 0 = low strength (2 mA) 1 = high strength (6 mA)	0
8	BCLK8 0 = low strength (2 mA) 1 = high strength (6 mA)	0
7	BCLK7 0 = low strength (2 mA) 1 = high strength (6 mA)	0
6	BCLK6 0 = low strength (2 mA) 1 = high strength (6 mA)	0
5	BCLK5 0 = low strength (2 mA) 1 = high strength (6 mA)	0
4	BCLK4 0 = low strength (2 mA) 1 = high strength (6 mA)	0
3	BCLK3 0 = low strength (2 mA) 1 = high strength (6 mA)	0
2	BCLK2 0 = low strength (2 mA) 1 = high strength (6 mA)	0
1	BCLK1 0 = low strength (2 mA) 1 = high strength (6 mA)	0
0	BCLK0 0 = low strength (2 mA) 1 = high strength (6 mA)	0

Other Pad Strength Register (Address 0xE24C)

This register controls the pad drive strength of the communications port, S/PDIF output, and master clock outputs. The default 2 mA setting should be adequate for most applications. The 6 mA setting should be used only when the integrity of the signal is compromised.

Table 75. Bit Descriptions of Other Pad Strength Register

Bit Position	Description	Default
[15:7]	Reserved	
6	SCL/CCLK 0 = low strength (2 mA) 1 = high strength (6 mA)	0
5	CLATCH 0 = low strength (2 mA) 1 = high strength (6 mA)	0
4	ADDR1/CDATA 0 = low strength (2 mA) 1 = high strength (6 mA)	0
3	ADDR0 0 = low strength (2 mA) 1 = high strength (6 mA)	0
2	SDA/COUT 0 = low strength (2 mA) 1 = high strength (6 mA)	0
1	SPDIFO 0 = low strength (2 mA) 1 = high strength (6 mA)	0
0	CLKOUT 0 = low strength (2 mA) 1 = high strength (6 mA)	0

FLEXIBLE TDM MODES

The ADAU1442/ADAU1445/ADAU1446 are able to operate in a flexible TDM mode, which allows them to interface to a wide variety of digital audio devices.

SERIAL INPUT FLEXIBLE TDM INTERFACE MODES AND SETTINGS

The flexible TDM mode is available for the SDATA_IN0 and SDATA_IN1 serial input ports. By using this mode, it is possible to override the default settings of the serial port and flexibly route the contents of an arbitrary TDM input stream to the input channels.

For this mode to be active, the word length bits of the corresponding serial ports must be set to 11 (TDM8 or flexible TDM).

In flexible TDM mode, each flexible TDM stream includes 32 bytes (called slots) of information for every frame on the frame clock. Combining the two serial input ports, this allows for a total of 64 bytes in the flexible stream.

It is important to note that, unlike in the FARM, where signals must be routed as stereo pairs, the data on the flexible TDM stream can be assigned to input channels individually. Each of the 24 input channels is capable of taking data from any slot (or combination of slots) in the flexible TDM stream, as long as data retrieval starts with Input Channel 0 and increases sequentially. This reserves all 24 input channels in the routing matrix for the flexible TDM interface, making them unavailable to the other serial input ports. Because the audio data can be input in 8-, 16-, or 24-bit format, a single channel may occupy more than one slot. An 8-bit channel occupies one slot, a 16-bit channel occupies two slots, and a 24-bit channel occupies three slots. To route flexible TDM data to the input channels, the starting slot number (most significant byte) and the bit depth (number of bytes, or slots, in the stream) must be set in the corresponding input channel register (Flexible TDM to Input Channel[23:0] registers). An example of the input flexible TDM interface mode is shown in Figure 56.

In this example, Input Channel 0 comes from Slot 4, Slot 5, and Slot 6 on the flexible TDM stream (a 24-bit audio channel). Input Channel 1 comes from Slot 12 (an 8-bit audio channel). Input Channel 2 comes from Slot 21 and Slot 22 on the input stream (a 16-bit audio channel). Input Channel 3 comes from Slot 39, Slot 40, and Slot 41 (a 24-bit audio channel). For the audio inputs with a bit depth of less than 24 bits, the LSBs are filled with 0s. Note that the assignment of slots to input channels must be in order, with the lowest slot number starting at Input Channel 0 and increasing sequentially. This is done to ensure compatibility with the automatic input channel assignment (see the Automatic Input Channel Assignment section).

The default setting of all nine bits high (0x01FF) indicates that the input channel is configured in the standard serial input interface mode and does not use the flexible TDM interface mode.

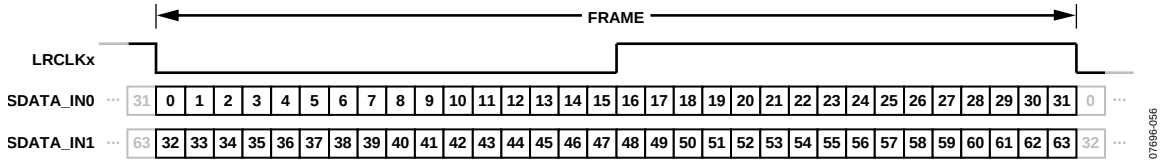


Figure 55. Flexible TDM Interface Mode—Input Streams

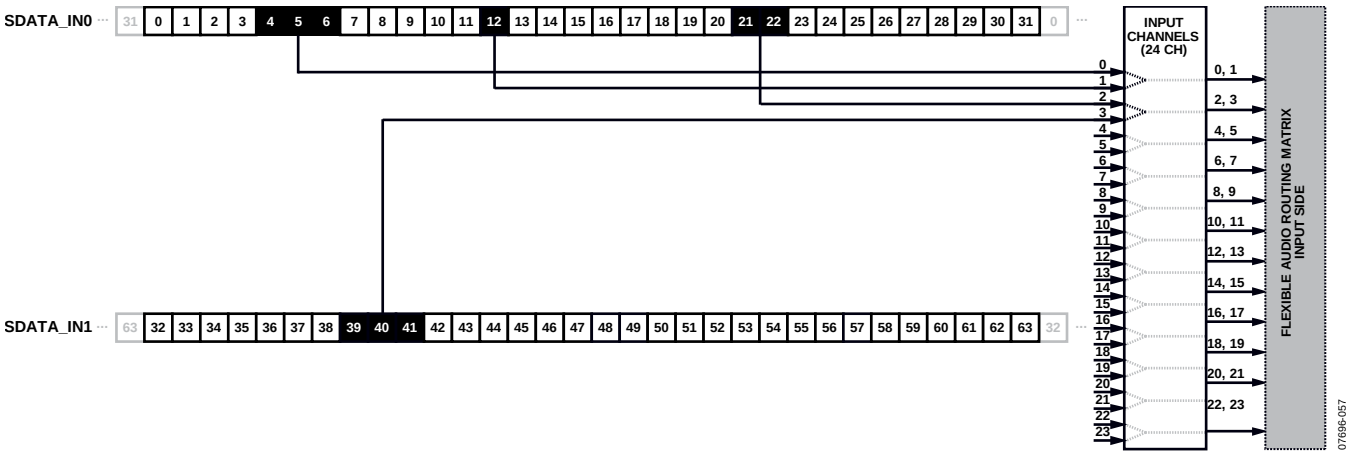


Figure 56. Flexible TDM Interface Mode—Input Routing Example

SOFTWARE FEATURES

SOFTWARE SAFELOAD

To update parameters in real time while avoiding pop and click noises on the output, the ADAU1442/ADAU1445/ADAU1446 use a software safeload mechanism. SigmaStudio automatically sets up the necessary code and parameters for new projects. The safeload code, along with other initialization code, fills the first 36 locations in program RAM. The first eight parameter RAM locations (Address 0x0000 to Address 0x0007) are configured by default in SigmaStudio as described in Table 81.

Table 81. Software Safeload Parameter RAM Defaults

Address (Hex)	Function
0x0000	Modulo RAM size
0x0001	Safeload Data 1
0x0002	Safeload Data 2
0x0003	Safeload Data 3
0x0004	Safeload Data 4
0x0005	Safeload Data 5
0x0006	Safeload target address (offset of −1)
0x0007	Number of words to write/safeload trigger

Address 0x0000, which controls the modulo RAM size, is set by SigmaStudio and is based on the dynamic address generator mode of the project.

Address 0x0001 to Address 0x0005 are the five data slots for storing the safeload data. The safeload parameter space contains five data slots by default because most standard signal processing algorithms have five parameters or fewer.

Address 0x0006 is the target address in parameter RAM (with an offset of −1). This designates the first address to be written. If more than one word is written, the address increments automatically for each data-word. The reason for the target address offset of −1 is that the write address is calculated relative to the address of the data, which starts at Address 0x0001. Therefore, if the intention is to update a parameter at Address 0x000A, the target address should be 0x0009.

Address 0x0007 designates the number of words to be written. For a biquad filter, the number is five. For a simple monogain cell, the number is one. This address also serves as the trigger; when it is written, a safeload write is triggered on the next frame.

The safeload mechanism is software based and executes once per audio frame. Therefore, system designers should take care when designing the communication protocol. A delay equal to or greater than the sampling period (the inverse of sampling frequency) is required between each safeload write. At a sample rate of 48 kHz, this equates to a delay of greater than or equal to 20.83 µs. If this delay is not observed, the downloaded data will be corrupted.

SOFTWARE SLEW

When the values of signal processing parameters are changed abruptly in real time, they sometimes cause pop and click sounds to appear on the audio outputs. To avoid this, some algorithms in SigmaStudio implement a software slew functionality. Software slew algorithms set a target value for the parameter and continuously update the parameter's value until it reaches the target.

The target value takes an additional space in parameter RAM, and the current value of the parameter is updated in the nonmodulo section of data RAM. Assignment of parameters and nonmodulo data RAM is handled by the SigmaStudio compiler and does not need to be programmed manually.

Slew parameters can follow several different curves, including an RC-type curve and a linear curve. These curve types are coded into each algorithm and cannot be modified by the user.

Because algorithms that use software slew generally require more RAM than their nonslew equivalents, they should be used only in situations in which a parameter is expected to change during operation of the device.

Figure 59 shows an example of a volume slew applied to a sine wave.

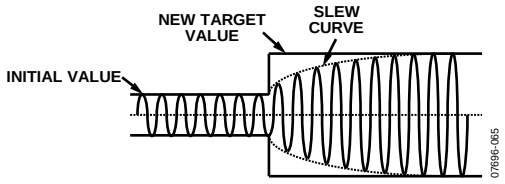


Figure 59. Example of Volume Slew

Table 86. Serial Input Port Modes Registers

Address			
Decimal	**Hex**	**Name**	**Read/Write Word Length**
57344	E000	Serial Input Port 0 modes	16 bits (2 bytes)
57345	E001	Serial Input Port 1 modes	16 bits (2 bytes)
57346	E002	Serial Input Port 2 modes	16 bits (2 bytes)
57347	E003	Serial Input Port 3 modes	16 bits (2 bytes)
57348	E004	Serial Input Port 4 modes	16 bits (2 bytes)
57349	E005	Serial Input Port 5 modes	16 bits (2 bytes)
57350	E006	Serial Input Port 6 modes	16 bits (2 bytes)
57351	E007	Serial Input Port 7 modes	16 bits (2 bytes)
57352	E008	Serial Input Port 8 modes	16 bits (2 bytes)

Table 87. Serial Output Port Modes Registers

Address			
Decimal	**Hex**	**Name**	**Read/Write Word Length**
57408	E040	Serial Output Port 0 modes	16 bits (2 bytes)
57409	E041	Serial Output Port 1 modes	16 bits (2 bytes)
57410	E042	Serial Output Port 2 modes	16 bits (2 bytes)
57411	E043	Serial Output Port 3 modes	16 bits (2 bytes)
57412	E044	Serial Output Port 4 modes	16 bits (2 bytes)
57413	E045	Serial Output Port 5 modes	16 bits (2 bytes)
57414	E046	Serial Output Port 6 modes	16 bits (2 bytes)
57415	E047	Serial Output Port 7 modes	16 bits (2 bytes)
57416	E048	Serial Output Port 8 modes	16 bits (2 bytes)
57417	E049	High speed slave interface mode	16 bit (2 bytes)

Table 88. Flexible Audio Routing Matrix Modes Registers

Address			
Decimal	**Hex**	**Name**	**Read/Write Word Length**
57472	E080	ASRC input select, Pair 0 (Channel 0, Channel 1)	16 bits (2 bytes)
57473	E081	ASRC input select, Pair 1 (Channel 2, Channel 3)	16 bits (2 bytes)
57474	E082	ASRC input select, Pair 2 (Channel 4, Channel 5)	16 bits (2 bytes)
57475	E083	ASRC input select, Pair 3 (Channel 6, Channel 7)	16 bits (2 bytes)
57476	E084	ASRC input select, Pair 4 (Channel 8, Channel 9)	16 bits (2 bytes)
57477	E085	ASRC input select, Pair 5 (Channel 10, Channel 11)	16 bits (2 bytes)
57478	E086	ASRC input select, Pair 6 (Channel 12, Channel 13)	16 bits (2 bytes)
57479	E087	ASRC input select, Pair 7 (Channel 14, Channel 15)	16 bits (2 bytes)
57480	E088	ASRC output rate select, Pair 0 (Channel 0, Channel 1)	16 bits (2 bytes)
57481	E089	ASRC output rate select, Pair 1 (Channel 2, Channel 3)	16 bits (2 bytes)
57482	E08A	ASRC output rate select, Pair 2 (Channel 4, Channel 5)	16 bits (2 bytes)
57483	E08B	ASRC output rate select, Pair 3 (Channel 6, Channel 7)	16 bits (2 bytes)
57484	E08C	ASRC output rate select, Pair 4 (Channel 8, Channel 9)	16 bits (2 bytes)
57485	E08D	ASRC output rate select, Pair 5 (Channel 10, Channel 11)	16 bits (2 bytes)
57486	E08E	ASRC output rate select, Pair 6 (Channel 12, Channel 13)	16 bits (2 bytes)
57487	E08F	ASRC output rate select, Pair 7 (Channel 14, Channel 15)	16 bits (2 bytes)
57488	E090	Serial output select, Pair 0 (Channel 0, Channel 1)	16 bits (2 bytes)
57489	E091	Serial output select, Pair 1 (Channel 2, Channel 3)	16 bits (2 bytes)
57490	E092	Serial output select, Pair 2 (Channel 4, Channel 5)	16 bits (2 bytes)