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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-TSSOP, 8-MSOP (0.118", 3.00mm Width)
Supplier Device Package	8-MSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f1501-i-ms

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## 2.0 ENHANCED MID-RANGE CPU

This family of devices contain an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- · Automatic Interrupt Context Saving
- · 16-level Stack with Overflow and Underflow
- · File Select Registers
- Instruction Set



#### FIGURE 2-1: CORE BLOCK DIAGRAM

#### 3.6.1 TRADITIONAL DATA MEMORY

The traditional data memory is a region from FSR address 0x000 to FSR address 0xFFF. The addresses correspond to the absolute addresses of all SFR, GPR and common registers.

#### FIGURE 3-9: TRADITIONAL DATA MEMORY MAP



		R/P-1	U-1	R/P-1	R/P-1	R/P-1	U-1
		LVP <sup>(1)</sup>	—	LPBOR	BORV <sup>(2)</sup>	STVREN	—
		bit 13					bit 8
U-1	U-1	U-1	U-1	U-1	U-1	R/P-1	R/P-1
_	—	—	_	—	—	WRT<	<1:0>
bit 7	·				·		bit 0
Legend:							
R = Read	able bit	P = Programm	able bit	U = Unimplem	nented bit, read	as '1'	
'0' = Bit is	cleared	'1' = Bit is set		-n = Value wh	en blank or afte	er Bulk Erase	
bit 13	LVP: Low-Vol	Itage Programm	ning Enable bit	(1)			
	1 = Low-volta 0 = High-volta	age on MCLR m	ust be used fo	or programming	1		
bit 12	Unimplemen	Unimplemented: Read as '1'					
bit 11	LPBOR: Low	-Power BOR Er	nable bit				
	1 = Low-Powe 0 = Low-Powe	<ul> <li>1 = Low-Power Brown-out Reset is disabled</li> <li>0 = Low-Power Brown-out Reset is enabled</li> </ul>					
bit 10	BORV: Browr 1 = Brown-ou 0 = Brown-ou	<b>BORV:</b> Brown-Out Reset Voltage Selection bit <sup>(2)</sup> 1 = Brown-out Reset voltage (VBOR), low trip point selected 0 = Brown-out Reset voltage (VBOR), high trip point selected					
bit 9	STVREN: Stack Overflow/Underflow Reset Enable bit 1 = Stack Overflow or Underflow will cause a Reset 0 = Stack Overflow or Underflow will not cause a Reset						
bit 8-2	Unimplemen	ted: Read as '1	,				
bit 1-0	bit 1-0 WRT<1:0>: Flash Memory Self-Write Protection bits <u>1 kW Flash memory (PIC12(L)F1501 only</u> ): 11 = Write protection off 10 = 000h to 0FFh write-protected, 100h to 3FFh may be modified 01 = 000h to 1FFh write-protected, 200h to 3FFh may be modified 00 = 000h to 3FFh write-protected, no addresses may be modified						
Note 1:	The LVP bit canne	ot be programm	ned to '0' wher	n Programming	mode is entere	ed via LVP.	

#### REGISTER 4-2: CONFIG2: CONFIGURATION WORD 2

2: See VBOR parameter for specific trip point voltages.

#### 7.3 Interrupts During Sleep

Some interrupts can be used to wake from Sleep. To wake from Sleep, the peripheral must be able to operate without the system clock. The interrupt source must have the appropriate Interrupt Enable bit(s) set prior to entering Sleep.

On waking from Sleep, if the GIE bit is also set, the processor will branch to the interrupt vector. Otherwise, the processor will continue executing instructions after the SLEEP instruction. The instruction directly after the SLEEP instruction will always be executed before branching to the ISR. Refer to **Section 8.0 "Power-Down Mode (Sleep)"** for more details.

## 7.4 INT Pin

The INT pin can be used to generate an asynchronous edge-triggered interrupt. This interrupt is enabled by setting the INTE bit of the INTCON register. The INTEDG bit of the OPTION\_REG register determines on which edge the interrupt will occur. When the INTEDG bit is set, the rising edge will cause the interrupt. When the INTEDG bit is clear, the falling edge will cause the interrupt. The INTF bit of the INTCON register will be set when a valid edge appears on the INT pin. If the GIE and INTE bits are also set, the processor will redirect program execution to the interrupt vector.

## 7.5 Automatic Context Saving

Upon entering an interrupt, the return PC address is saved on the stack. Additionally, the following registers are automatically saved in the shadow registers:

- W register
- STATUS register (except for TO and PD)
- BSR register
- FSR registers
- PCLATH register

Upon exiting the Interrupt Service Routine, these registers are automatically restored. Any modifications to these registers during the ISR will be lost. If modifications to any of these registers are desired, the corresponding shadow register should be modified and the value will be restored when exiting the ISR. The shadow registers are available in Bank 31 and are readable and writable. Depending on the user's application, other registers may also need to be saved.

## 10.0 FLASH PROGRAM MEMORY CONTROL

The Flash program memory is readable and writable during normal operation over the full VDD range. Program memory is indirectly addressed using Special Function Registers (SFRs). The SFRs used to access program memory are:

- PMCON1
- PMCON2
- PMDATL
- PMDATH
- PMADRL
- PMADRH

When accessing the program memory, the PMDATH:PMDATL register pair forms a 2-byte word that holds the 14-bit data for read/write, and the PMADRH:PMADRL register pair forms a 2-byte word that holds the 15-bit address of the program memory location being read.

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the operating voltage range of the device.

The Flash program memory can be protected in two ways; by code protection (CP bit in Configuration Words) and write protection (WRT<1:0> bits in Configuration Words).

Code protection ( $\overline{CP} = 0$ )<sup>(1)</sup>, disables access, reading and writing, to the Flash program memory via external device programmers. Code protection does not affect the self-write and erase functionality. Code protection can only be reset by a device programmer performing a Bulk Erase to the device, clearing all Flash program memory, Configuration bits and User IDs.

Write protection prohibits self-write and erase to a portion or all of the Flash program memory, as defined by the bits WRT<1:0>. Write protection does not affect a device programmers ability to read, write or erase the device.

**Note 1:** Code protection of the entire Flash program memory array is enabled by clearing the CP bit of Configuration Words.

## 10.1 PMADRL and PMADRH Registers

The PMADRH:PMADRL register pair can address up to a maximum of 32K words of program memory. When selecting a program address value, the MSB of the address is written to the PMADRH register and the LSB is written to the PMADRL register.

#### 10.1.1 PMCON1 AND PMCON2 REGISTERS

PMCON1 is the control register for Flash program memory accesses.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set, in software. They are cleared by hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation to occur. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit and execute the appropriate error handling routine.

The PMCON2 register is a write-only register. Attempting to read the PMCON2 register will return all '0's.

To enable writes to the program memory, a specific pattern (the unlock sequence), must be written to the PMCON2 register. The required unlock sequence prevents inadvertent writes to the program memory write latches and Flash program memory.

## 10.2 Flash Program Memory Overview

It is important to understand the Flash program memory structure for erase and programming operations. Flash program memory is arranged in rows. A row consists of a fixed number of 14-bit program memory words. A row is the minimum size that can be erased by user software.

After a row has been erased, the user can reprogram all or a portion of this row. Data to be written into the program memory row is written to 14-bit wide data write latches. These write latches are not directly accessible to the user, but may be loaded via sequential writes to the PMDATH:PMDATL register pair.

Note:	If the user wants to modify only a portion of a previously programmed row, then the contents of the entire row must be read and saved in RAM prior to the erase. Then, new data and retained data can be written into the write latches to reprogram the row of Flash program memory. How- ever, any unprogrammed locations can be written without first erasing the row. In this case, it is not necessary to save and
	written without first erasing the row. In this case, it is not necessary to save and
	rewrite the other previously programmed locations.

See Table 10-1 for Erase Row size and the number of write latches for Flash program memory.

#### TABLE 10-1: FLASH MEMORY ORGANIZATION BY DEVICE

Device	Row Erase (words)	Write Latches (words)	
PIC12(L)F1501	16	16	

## 13.0 FIXED VOLTAGE REFERENCE (FVR)

The Fixed Voltage Reference (FVR) is a stable voltage reference, independent of VDD, with a nominal output level (VFVR) of 1.024V. The output of the FVR can be configured to supply a reference voltage to the following:

- ADC input channel
- Comparator positive input
- · Comparator negative input

The FVR can be enabled by setting the FVREN bit of the FVRCON register.

#### 13.1 Independent Gain Amplifier

The output of the FVR supplied to the peripherals, (listed above), is routed through a programmable gain amplifier. Each amplifier can be programmed for a gain of 1x, 2x or 4x, to produce the three possible voltage levels.

The ADFVR<1:0> bits of the FVRCON register are used to enable and configure the gain amplifier settings for the reference supplied to the ADC module. Reference **Section 15.0 "Analog-to-Digital Converter** (ADC) Module" for additional information.

The CDAFVR<1:0> bits of the FVRCON register are used to enable and configure the gain amplifier settings for the reference supplied to the comparator modules. Reference **Section 17.0 "Comparator Module**" for additional information.

To minimize current consumption when the FVR is disabled, the FVR buffers should be turned off by clearing the Buffer Gain Selection bits.

## 13.2 FVR Stabilization Period

When the Fixed Voltage Reference module is enabled, it requires time for the reference and amplifier circuits to stabilize. Once the circuits stabilize and are ready for use, the FVRRDY bit of the FVRCON register will be set. See the FVR Stabilization Period characterization graph, Figure 28-52.

## FIGURE 13-1: VOLTAGE REFERENCE BLOCK DIAGRAM



Peripheral	Conditions	Description
HFINTOSC	FOSC<2:0> = 010 and IRCF<3:0> = 000x	INTOSC is active and device is not in Sleep.
	BOREN<1:0> = 11	BOR always enabled.
BOR	BOREN<1:0> = 10 and BORFS = 1	BOR disabled in Sleep mode, BOR Fast Start enabled.
	BOREN<1:0> = 01 and BORFS = 1	BOR under software control, BOR Fast Start enabled.
LDO	All PIC12F1501 devices, when VREGPM = 1 and not in Sleep	The device runs off of the Low-Power Regulator when in Sleep mode.

## TABLE 13-1: PERIPHERALS REQUIRING THE FIXED VOLTAGE REFERENCE (FVR)

## 14.0 TEMPERATURE INDICATOR MODULE

This family of devices is equipped with a temperature circuit designed to measure the operating temperature of the silicon die. The circuit's range of operating temperature falls between -40°C and +85°C. The output is a voltage that is proportional to the device temperature. The output of the temperature indicator is internally connected to the device ADC.

The circuit may be used as a temperature threshold detector or a more accurate temperature indicator, depending on the level of calibration performed. A one-point calibration allows the circuit to indicate a temperature closely surrounding that point. A two-point calibration allows the circuit to sense the entire range of temperature more accurately. Reference Application Note AN1333, "Use and Calibration of the Internal Temperature Indicator" (DS01333) for more details regarding the calibration process.

#### 14.1 Circuit Operation

Figure 14-1 shows a simplified block diagram of the temperature circuit. The proportional voltage output is achieved by measuring the forward voltage drop across multiple silicon junctions.

Equation 14-1 describes the output characteristics of the temperature indicator.

#### EQUATION 14-1: VOUT RANGES

High Range: VOUT = VDD - 4VT

Low Range: VOUT = VDD - 2VT

The temperature sense circuit is integrated with the Fixed Voltage Reference (FVR) module. See **Section 13.0 "Fixed Voltage Reference (FVR)"** for more information.

The circuit is enabled by setting the TSEN bit of the FVRCON register. When disabled, the circuit draws no current.

The circuit operates in either high or low range. The high range, selected by setting the TSRNG bit of the FVRCON register, provides a wider output voltage. This provides more resolution over the temperature range, but may be less consistent from part to part. This range requires a higher bias voltage to operate and thus, a higher VDD is needed.

The low range is selected by clearing the TSRNG bit of the FVRCON register. The low range generates a lower voltage drop and thus, a lower bias voltage is needed to operate the circuit. The low range is provided for low voltage operation.

## FIGURE 14-1: TEMPERATURE CIRCUIT DIAGRAM



## 14.2 Minimum Operating VDD

When the temperature circuit is operated in low range, the device may be operated at any operating voltage that is within specifications.

When the temperature circuit is operated in high range, the device operating voltage, VDD, must be high enough to ensure that the temperature circuit is correctly biased.

Table 14-1 shows the recommended minimum VDD vs. range setting.

TABLE 14-1: RECOMMENDED VDD VS. RANGE

Min. Vdd, TSRNG = 1	Min. VDD, TSRNG = 0
3.6V	1.8V

## 14.3 Temperature Output

The output of the circuit is measured using the internal Analog-to-Digital Converter. A channel is reserved for the temperature circuit output. Refer to **Section 15.0 "Analog-to-Digital Converter (ADC) Module**" for detailed information.

## 14.4 ADC Acquisition Time

To ensure accurate temperature measurements, the user must wait at least 200  $\mu$ s after the ADC input multiplexer is connected to the temperature indicator output before the conversion is performed. In addition, the user must wait 200  $\mu$ s between sequential conversions of the temperature indicator output.

#### 15.1.5 INTERRUPTS

The ADC module allows for the ability to generate an interrupt upon completion of an Analog-to-Digital conversion. The ADC Interrupt Flag is the ADIF bit in the PIR1 register. The ADC Interrupt Enable is the ADIE bit in the PIE1 register. The ADIF bit must be cleared in software.

Note 1:	The ADIF bit is set at the completion of
	every conversion, regardless of whether
	or not the ADC interrupt is enabled.

**2:** The ADC operates during Sleep only when the FRC oscillator is selected.

This interrupt can be generated while the device is operating or while in Sleep. If the device is in Sleep, the interrupt will wake-up the device. Upon waking from Sleep, the next instruction following the SLEEP instruction is always executed. If the user is attempting to wake-up from Sleep and resume in-line code execution, the GIE and PEIE bits of the INTCON register must be disabled. If the GIE and PEIE bits of the INTCON register are enabled, execution will switch to the Interrupt Service Routine.

#### 15.1.6 RESULT FORMATTING

The 10-bit ADC conversion result can be supplied in two formats, left justified or right justified. The ADFM bit of the ADCON1 register controls the output format.

Figure 15-3 shows the two output formats.

#### FIGURE 15-3: 10-BIT ADC CONVERSION RESULT FORMAT



## PIC12(L)F1501

## 15.3 Register Definitions: ADC Control

#### REGISTER 15-1: ADCON0: ADC CONTROL REGISTER 0

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
_			CHS<4:0>			GO/DONE	ADON
bit 7							bit 0
Legend:							
R = Reada	ıble bit	W = Writable	bit	U = Unimpler	nented bit, rea	d as '0'	
u = Bit is u	nchanged	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	DR/Value at all o	other Resets
'1' = Bit is :	set	'0' = Bit is cle	ared				
bit 7	Unimpleme	nted: Read as '	0'				
bit 6-2	CHS<4:0>:	Analog Channel	Select bits				
	00000 = AN	10					
	00001 = AN	N1					
	00010 = AP	N2					
	00011 = Ar	NO Served No cha	nnel connecte	d			
	•			u.			
	•						
	•						
	11100 <b>= Re</b>	eserved. No cha	nnel connecte	d.			
	11101 <b>= Te</b>	mperature Indica	ator <sup>(1)</sup>	(2)			
	11110 = DA	C (Digital-to-An	alog Converte	r)(3)	2)		
	11111 = FV	R (Fixed Voltage	e Reference) E		_)		
bit 1	GO/DONE:	ADC Conversion	n Status bit				
	1 = ADC col	nversion cycle ir	n progress. Se	tting this bit sta	rts an ADC co	nversion cycle.	
		s automatically	cleared by har	dware when the	e ADC convers	sion has comple	eted.
				Jiess			
bit 0		Enable bit					
	1 = ADC is c	disabled and cor		erating current			
Note 1.	See Section 14		Indicator Me	dule" for more	information		
1101E 1. 2.	See Section 13	0 "Fixed Voltage	- Reference	(EVR)" for more	information		
2.	Occ Section 13.					a a na infanna atian	_

3: See Section 16.0 "5-Bit Digital-to-Analog Converter (DAC) Module" for more information.

#### **19.6** Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit of the PIR1 register is set. To enable the interrupt on rollover, you must set these bits:

- TMR10N bit of the T1CON register
- TMR1IE bit of the PIE1 register
- · PEIE bit of the INTCON register
- GIE bit of the INTCON register

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

**Note:** The TMR1H:TMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

## 19.7 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- TMR1ON bit of the T1CON register must be set
- TMR1IE bit of the PIE1 register must be set
- PEIE bit of the INTCON register must be set
- T1SYNC bit of the T1CON register must be set
- TMR1CS bits of the T1CON register must be configured

The device will wake-up on an overflow and execute the next instructions. If the GIE bit of the INTCON register is set, the device will call the Interrupt Service Routine.

Timer1 oscillator will continue to operate in Sleep regardless of the T1SYNC bit setting.

#### FIGURE 19-2: TIMER1 INCREMENTING EDGE



#### 19.7.1 ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function register, APFCON. To determine which pins can be moved and what their default locations are upon a Reset, see **Section 11.1 "Alternate Pin Function"** for more information.

## 24.10 Operation During Sleep

The CWG module operates independently from the system clock and will continue to run during Sleep, provided that the clock and input sources selected remain active.

The HFINTOSC remains active during Sleep, provided that the CWG module is enabled, the input source is active, and the HFINTOSC is selected as the clock source, regardless of the system clock source selected.

In other words, if the HFINTOSC is simultaneously selected as the system clock and the CWG clock source, when the CWG is enabled and the input source is active, the CPU will go idle during Sleep, but the CWG will continue to operate and the HFINTOSC will remain active.

This will have a direct effect on the Sleep mode current.

## 24.11 Configuring the CWG

The following steps illustrate how to properly configure the CWG to ensure a synchronous start:

- 1. Ensure that the TRIS control bits corresponding to CWGxA and CWGxB are set so that both are configured as inputs.
- 2. Clear the GxEN bit, if not already cleared.
- 3. Set desired dead-band times with the CWGxDBR and CWGxDBF registers.
- 4. Setup the following controls in CWGxCON2 auto-shutdown register:
  - · Select desired shutdown source.
  - Select both output overrides to the desired levels (this is necessary even if not using auto-shutdown because start-up will be from a shutdown state).
  - Set the GxASE bit and clear the GxARSEN bit.
- 5. Select the desired input source using the CWGxCON1 register.
- 6. Configure the following controls in CWGxCON0 register:
  - · Select desired clock source.
  - Select the desired output polarities.
  - Set the output enables for the outputs to be used.
- 7. Set the GxEN bit.
- Clear TRIS control bits corresponding to CWGxA and CWGxB to be used to configure those pins as outputs.
- If auto-restart is to be used, set the GxARSEN bit and the GxASE bit will be cleared automatically. Otherwise, clear the GxASE bit to start the CWG.

#### 24.11.1 PIN OVERRIDE LEVELS

The levels driven to the output pins, while the shutdown input is true, are controlled by the GxASDLA and GxASDLB bits of the CWGxCON1 register (Register 24-3). GxASDLA controls the CWG1A override level and GxASDLB controls the CWG1B override level. The control bit logic level corresponds to the output logic drive level while in the shutdown state. The polarity control does not apply to the override level.

#### 24.11.2 AUTO-SHUTDOWN RESTART

After an auto-shutdown event has occurred, there are two ways to have resume operation:

- Software controlled
- Auto-restart

The restart method is selected with the GxARSEN bit of the CWGxCON2 register. Waveforms of software controlled and automatic restarts are shown in Figure 24-5 and Figure 24-6.

#### 24.11.2.1 Software Controlled Restart

When the GxARSEN bit of the CWGxCON2 register is cleared, the CWG must be restarted after an auto-shut-down event by software.

Clearing the shutdown state requires all selected shutdown inputs to be low, otherwise the GxASE bit will remain set. The overrides will remain in effect until the first rising edge event after the GxASE bit is cleared. The CWG will then resume operation.

#### 24.11.2.2 Auto-Restart

When the GxARSEN bit of the CWGxCON2 register is set, the CWG will restart from the auto-shutdown state automatically.

The GxASE bit will clear automatically when all shutdown sources go low. The overrides will remain in effect until the first rising edge event after the GxASE bit is cleared. The CWG will then resume operation.

MOVIW	Move INDFn to W
Syntax:	[ <i>label</i> ] MOVIW ++FSRn [ <i>label</i> ] MOVIWFSRn [ <i>label</i> ] MOVIW FSRn++ [ <i>label</i> ] MOVIW FSRn [ <i>label</i> ] MOVIW k[FSRn]
Operands:	n ∈ [0,1] mm ∈ [00,01, 10, 11] -32 ≤ k ≤ 31
Operation:	$\begin{split} &\text{INDFn} \rightarrow W \\ &\text{Effective address is determined by} \\ &\text{FSR + 1 (preincrement)} \\ &\text{FSR - 1 (predecrement)} \\ &\text{FSR + k (relative offset)} \\ &\text{After the Move, the FSR value will be either:} \\ &\text{FSR + 1 (all increments)} \\ &\text{FSR - 1 (all decrements)} \\ &\text{Unchanged} \end{split}$
Status Affected:	Z

Mode	Syntax	mm
Preincrement	++FSRn	00
Predecrement	FSRn	01
Postincrement	FSRn++	10
Postdecrement	FSRn	11

This instruction is used to move data between W and one of the indirect registers (INDFn). Before/after this move, the pointer (FSRn) is updated by pre/post incrementing/decrementing it.

> **Note:** The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the FSRn.

FSRn is limited to the range 0000h -FFFFh. Incrementing/decrementing it beyond these bounds will cause it to wrap-around.

#### MOVLB Move literal to BSR

Description:

Syntax:	[ <i>label</i> ]MOVLB k
Operands:	$0 \leq k \leq 31$
Operation:	$k \rightarrow BSR$
Status Affected:	None
Description:	The 5-bit literal 'k' is loaded into the Bank Select Register (BSR).

MOVLP	Move literal to PCLATH
Syntax:	[ <i>label</i> ]MOVLP k
Operands:	$0 \le k \le 127$
Operation:	$k \rightarrow PCLATH$
Status Affected:	None
Description:	The 7-bit literal 'k' is loaded into the PCLATH register.
MOVLW	Move literal to W
Syntax:	[ <i>label</i> ] MOVLW k
Operands:	$0 \leq k \leq 255$
Operation:	$k \rightarrow (W)$
Status Affected:	None
Description:	The 8-bit literal 'k' is loaded into W reg- ister. The "don't cares" will assemble as '0's.
Words:	1
Cycles:	1
Example:	MOVLW 0x5A
	After Instruction W = 0x5A
MOVWF	Move W to f
Syntax:	[ <i>label</i> ] MOVWF f
Operands:	$0 \leq f \leq 127$
Operation:	$(W) \rightarrow (f)$
Status Affected:	None
Description:	Move data from W register to register 'f'.
Words:	1
Cycles:	1
Example:	MOVWF OPTION_REG
	Before Instruction OPTION_REG = 0xFF W = 0x4F After Instruction OPTION_REG = 0x4F W = 0x4F

# PIC12(L)F1501

RRF	Rotate Right f through Carry								
Syntax:	[ <i>label</i> ] RRF f,d								
Operands:	$0 \le f \le 127$ $d \in [0,1]$								
Operation:	See description below								
Status Affected:	С								
Description:	The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.								



SUBLW	Subtract W from literal							
Syntax:	[label] SL	[ <i>label</i> ] SUBLW k						
Operands:	$0 \leq k \leq 255$							
Operation:	$k \operatorname{-}(W) \operatorname{\rightarrow}(W$	/)						
Status Affected:	C, DC, Z							
Description:	The W regist plement met 'k'. The resul ter.	The W register is subtracted (2's com- plement method) from the 8-bit literal 'k'. The result is placed in the W regis- ter.						
	<b>C</b> = 0	W > k						
	$C = 1$ $W \le k$							
	DC = 0 W<3:0> > k<3:0>							

DC = 1

 $W<3:0> \le k<3:0>$ 

SLEEP	Enter Sleep mode
Syntax:	[label] SLEEP
Operands:	None
Operation:	$\begin{array}{l} \text{O0h} \rightarrow \text{WDT,} \\ 0 \rightarrow \underline{\text{WDT}} \text{ prescaler,} \\ 1 \rightarrow \underline{\text{TO}}, \\ 0 \rightarrow \overline{\text{PD}} \end{array}$
Status Affected:	TO, PD
Description:	The power-down Status bit, $\overline{\text{PD}}$ is cleared. Time-out Status bit, $\overline{\text{TO}}$ is set. Watchdog Timer and its pres- caler are cleared. The processor is put into Sleep mode with the oscillator stopped.

SUBWF	Subtract W	from f				
Syntax:	[label] SL	IBWF f,d				
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d  \in  [0,1] \end{array}$					
Operation:	(f) - (W) $\rightarrow$ (d	estination)				
Status Affected:	C, DC, Z					
Description:	Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f.					
	<b>C =</b> 0	W > f				
	<b>C =</b> 1	$W \leq f$				
	DC = 0	W<3:0> > f<3:0>				
	DC = 1	W<3:0> ≤ f<3:0>				

SUBWFB	Subtract W from f with Borrow					
Syntax:	SUBWFB f {,d}					
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d  \in  [0,1] \end{array}$					
Operation:	$(f) - (W) - (\overline{B}) \rightarrow dest$					
Status Affected:	C, DC, Z					
Description:	Subtract W and the BORROW flag (CARRY) from register 'f' (2's comple- ment method). If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.					





TAB	LE	27-12	2: C	ONF	IGUR/	ATIC	)N L	.OGIC	CEL	L (CL	-C)	CHAR	ACTI	ERIS	TICS
•				-											

Standard Operating Conditions (unless otherwise stated)								
Param. No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions	
CLC01*	TCLCIN	CLC input time	—	7	_	ns		
CLC02*	TCLC	CLC module input to output propagation time	_	24 12		ns ns	VDD = 1.8V VDD > 3.6V	
CLC03*	TCLCOUT	CLC output time Rise Time		OS18			(Note 1)	
		Fall Time		OS19	_		(Note 1)	
CLC04*	FCLCMAX	CLC maximum switching frequency		45	—	MHz		
* These parameters are characterized but not tested								

These parameters are characterized but not tested.

Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance t only and are not tested.

Note 1:See Table 27-9 for OS18 and OS19 rise and fall times.

# PIC12(L)F1501







## 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-111C Sheet 1 of 2

#### 8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS					
Dimension	Limits	MIN	NOM	MAX		
Number of Pins	N		8			
Pitch	е		0.65 BSC	_		
Overall Height	A	0.80	0.90	1.00		
Standoff	A1	0.00	0.02	0.05		
Contact Thickness	A3	0.20 REF				
Overall Length	D	3.00 BSC				
Exposed Pad Width	E2	1.34 - 1.60				
Overall Width	E	3.00 BSC				
Exposed Pad Length	D2	1.60	-	2.40		
Contact Width	b	0.25	0.30	0.35		
Contact Length	L	0.20 0.30 0.55				
Contact-to-Exposed Pad	K	0.20	-	-		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package may have one or more exposed tie bars at ends.

3. Package is saw singulated

4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-062C Sheet 2 of 2

## **PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	$\begin{bmatrix} [X]^{(1)} & - & X \\ T & T \end{bmatrix}$	/XX Package	XXX	Exa	mple	<b>PS:</b> 121 E1501T - 1/SN
	Option Range			b)	Tape Indu SOI PIC	strial temperature, C package 12F1501 - I/P
Device:	PIC12LF1501, PIC12F1501				Indu PDI	strial temperature P package
Tape and Reel Option:	Blank = Standard packaging T = Tape and Reel <sup>(1)</sup>	(tube or tray)		с)	Exte DFN	nded temperature, package
Temperature Range:	$ \begin{array}{rcl} I & = -40^{\circ}C \ to & +85^{\circ}C \\ E & = -40^{\circ}C \ to & +125^{\circ}C \end{array} \end{array} $	(Industrial) (Extended)				
Package:	MC = Micro Lead Frame MF = Micro Lead Frame MS = MSOP MU = Micro Lead Frame P = Plastic DIP SN = SOIC	DFN) 2x3 DFN) 3x3 UDFN) 2x3		Note	9 1:	Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
Pattern:	QTP, SQTP, Code or Special F (blank otherwise)	Requirements			2:	For other small form-factor package availability and marking information, please visit www.microchip.com/packaging or contact your local sales office.