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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-DFN (2x3)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12lf1501-i-mc

5.4 Register Definitions: Oscillator Control

REGISTER 5-1: OSCCON: OSCILLATOR CONTROL REGISTER

U-0	R/W-0/0	R/W-1/1	R/W-1/1	R/W-1/1	U-0	R/W-0/0	R/W-0/0
—	IRCF<3:0>				—	SCS<1:0>	
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7 **Unimplemented:** Read as '0'

bit 6-3 **IRCF<3:0>:** Internal Oscillator Frequency Select bits

1111 = 16 MHz

1110 = 8 MHz

1101 = 4 MHz

1100 = 2 MHz

1011 = 1 MHz

1010 = 500 kHz⁽¹⁾

1001 = 250 kHz⁽¹⁾

1000 = 125 kHz⁽¹⁾

0111 = 500 kHz (default upon Reset)

0110 = 250 kHz

0101 = 125 kHz

0100 = 62.5 kHz

001x = 31.25 kHz

000x = 31 kHz LF

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **SCS<1:0>:** System Clock Select bits

1x = Internal oscillator block

01 = Reserved

00 = Clock determined by FOSC<1:0> in Configuration Words.

Note 1: Duplicate frequency derived from HFINTOSC.

6.0 RESETS

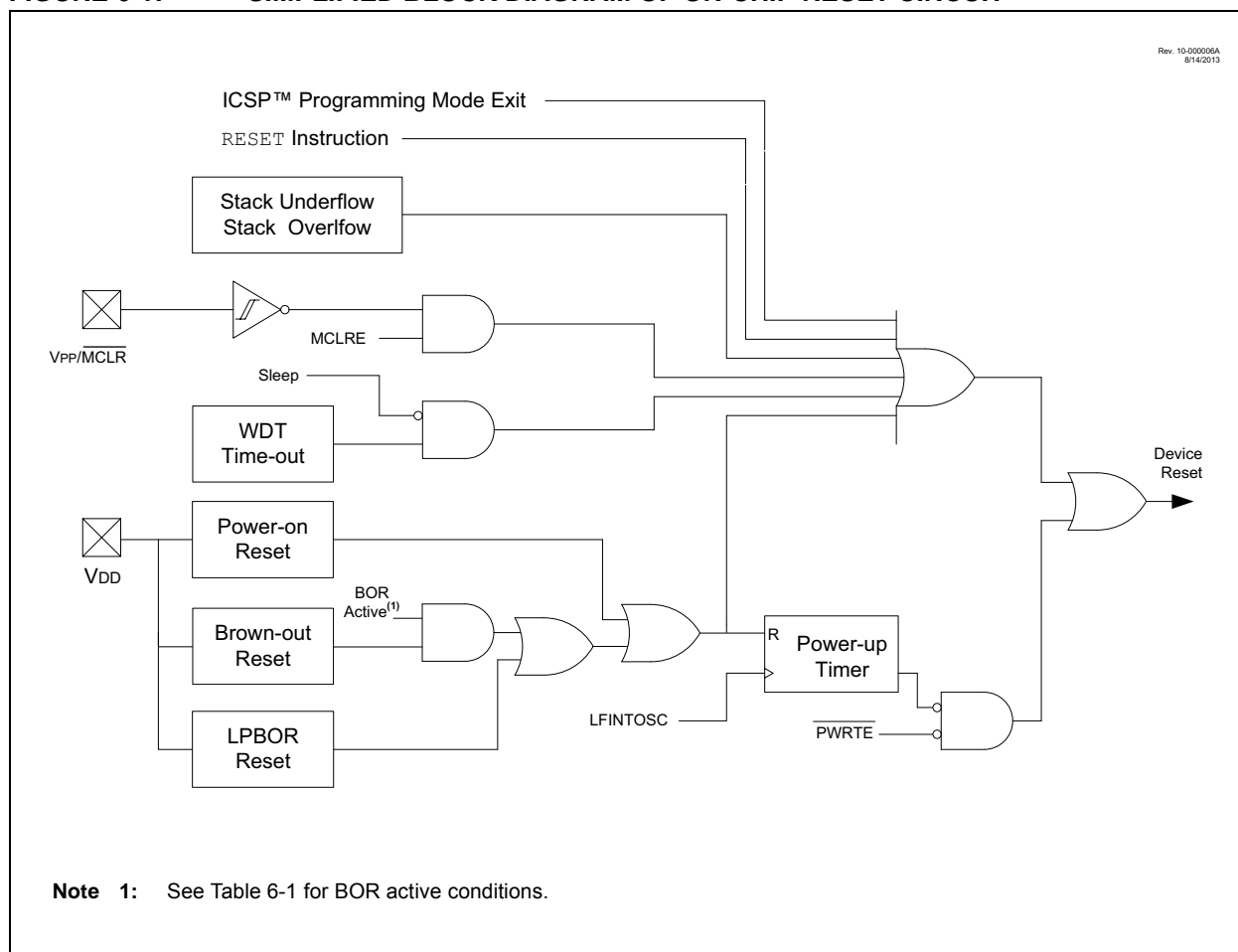
There are multiple ways to reset this device:

- Power-on Reset (POR)
- Brown-out Reset (BOR)
- Low-Power Brown-out Reset (LPBOR)
- MCLR Reset
- WDT Reset
- RESET instruction
- Stack Overflow
- Stack Underflow
- Programming mode exit

To allow VDD to stabilize, an optional power-up timer can be enabled to extend the Reset time after a BOR or POR event.

A simplified block diagram of the On-chip Reset Circuit is shown in Figure 6-1.

FIGURE 6-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



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6.1 Power-On Reset (POR)

The POR circuit holds the device in Reset until VDD has reached an acceptable level for minimum operation. Slow rising VDD, fast operating speeds or analog performance may require greater than minimum VDD. The PWRT, BOR or MCLR features can be used to extend the start-up period until all device operation conditions have been met.

6.1.1 POWER-UP TIMER (PWRT)

The Power-up Timer provides a nominal 64 ms time-out on POR or Brown-out Reset.

The device is held in Reset as long as PWRT is active. The PWRT delay allows additional time for the VDD to rise to an acceptable level. The Power-up Timer is enabled by clearing the PWRT bit in Configuration Words.

The Power-up Timer starts after the release of the POR and BOR.

For additional information, refer to Application Note AN607, "Power-up Trouble Shooting" (DS00607).

6.2 Brown-Out Reset (BOR)

The BOR circuit holds the device in Reset when VDD reaches a selectable minimum level. Between the POR and BOR, complete voltage range coverage for execution protection can be implemented.

The Brown-out Reset module has four operating modes controlled by the BOREN<1:0> bits in Configuration Words. The four operating modes are:

- BOR is always on
- BOR is off when in Sleep
- BOR is controlled by software
- BOR is always off

Refer to Table 6-1 for more information.

The Brown-out Reset voltage level is selectable by configuring the BORV bit in Configuration Words.

A VDD noise rejection filter prevents the BOR from triggering on small events. If VDD falls below Vpor for a duration greater than parameter TBORDC, the device will reset. See Figure 6-2 for more information.

TABLE 6-1: BOR OPERATING MODES

BOREN<1:0>	SBOREN	Device Mode	BOR Mode	Instruction Execution upon: Release of POR or Wake-up from Sleep
11	X	X	Active	Waits for BOR ready ⁽¹⁾ (BORRDY = 1)
10	X	Awake	Active	Waits for BOR ready (BORRDY = 1)
		Sleep	Disabled	
01	1	X	Active	Waits for BOR ready ⁽¹⁾ (BORRDY = 1)
	0	X	Disabled	Begins immediately (BORRDY = x)
00	X	X	Disabled	

Note 1: In these specific cases, "release of POR" and "wake-up from Sleep," there is no delay in start-up. The BOR ready flag, (BORRDY = 1), will be set before the CPU is ready to execute instructions because the BOR circuit is forced on by the BOREN<1:0> bits.

6.2.1 BOR IS ALWAYS ON

When the BOREN bits of Configuration Words are programmed to '11', the BOR is always on. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is active during Sleep. The BOR does not delay wake-up from Sleep.

6.2.2 BOR IS OFF IN SLEEP

When the BOREN bits of Configuration Words are programmed to '10', the BOR is on, except in Sleep. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is not active during Sleep. The device wake-up will be delayed until the BOR is ready.

6.2.3 BOR CONTROLLED BY SOFTWARE

When the BOREN bits of Configuration Words are programmed to '01', the BOR is controlled by the SBOREN bit of the BORCON register. The device start-up is not delayed by the BOR ready condition or the VDD level.

BOR protection begins as soon as the BOR circuit is ready. The status of the BOR circuit is reflected in the BORRDY bit of the BORCON register.

BOR protection is unchanged by Sleep.

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6.12 Determining the Cause of a Reset

Upon any Reset, multiple bits in the STATUS and PCON registers are updated to indicate the cause of the Reset. Table 6-3 and Table 6-4 show the Reset conditions of these registers.

TABLE 6-3: RESET STATUS BITS AND THEIR SIGNIFICANCE

STKOVF	STKUNF	RWDT	RMCLR	RI	POR	BOR	TO	PD	Condition
0	0	1	1	1	0	x	1	1	Power-on Reset
0	0	1	1	1	0	x	0	x	Illegal, \overline{TO} is set on \overline{POR}
0	0	1	1	1	0	x	x	0	Illegal, \overline{PD} is set on \overline{POR}
0	0	u	1	1	u	0	1	1	Brown-out Reset
u	u	0	u	u	u	u	0	u	WDT Reset
u	u	u	u	u	u	u	0	0	WDT Wake-up from Sleep
u	u	u	u	u	u	u	1	0	Interrupt Wake-up from Sleep
u	u	u	0	u	u	u	u	u	\overline{MCLR} Reset during normal operation
u	u	u	0	u	u	u	1	0	\overline{MCLR} Reset during Sleep
u	u	u	u	0	u	u	u	u	RESET Instruction Executed
1	u	u	u	u	u	u	u	u	Stack Overflow Reset (STVREN = 1)
u	1	u	u	u	u	u	u	u	Stack Underflow Reset (STVREN = 1)

TABLE 6-4: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	0000h	---1 1000	00-- 110x
\overline{MCLR} Reset during normal operation	0000h	---u muumuu	uu-- 0uuu
\overline{MCLR} Reset during Sleep	0000h	---1 0uuu	uu-- 0uuu
WDT Reset	0000h	---0 muumuu	uu-- uuuu
WDT Wake-up from Sleep	PC + 1	---0 0uuu	uu-- uuuu
Brown-out Reset	0000h	---1 1uuu	00-- 11u0
Interrupt Wake-up from Sleep	PC + 1 ⁽¹⁾	---1 0uuu	uu-- uuuu
RESET Instruction Executed	0000h	---u uuuu	uu-- u0uu
Stack Overflow Reset (STVREN = 1)	0000h	---u uuuu	1u-- uuuu
Stack Underflow Reset (STVREN = 1)	0000h	---u uuuu	u1-- uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and the Global Interrupt Enable bit (GIE) is set, the return address is pushed on the stack and PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

12.6 Register Definitions: Interrupt-on-Change Control

REGISTER 12-1: IOCAP: INTERRUPT-ON-CHANGE PORTA POSITIVE EDGE REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
 '1' = Bit is set '0' = Bit is cleared

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **IOCAP<5:0>:** Interrupt-on-Change PORTA Positive Edge Enable bits

- 1 = Interrupt-on-Change enabled on the pin for a positive going edge. IOCAFx bit and IOCIF flag will be set upon detecting an edge.
- 0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 12-2: IOCAN: INTERRUPT-ON-CHANGE PORTA NEGATIVE EDGE REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
 '1' = Bit is set '0' = Bit is cleared

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **IOCAN<5:0>:** Interrupt-on-Change PORTA Negative Edge Enable bits

- 1 = Interrupt-on-Change enabled on the pin for a negative going edge. IOCAFx bit and IOCIF flag will be set upon detecting an edge.
- 0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 12-3: IOCAF: INTERRUPT-ON-CHANGE PORTA FLAG REGISTER

U-0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
—	—	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
 '1' = Bit is set '0' = Bit is cleared HS - Bit is set in hardware

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **IOCAF<5:0>:** Interrupt-on-Change PORTA Flag bits

- 1 = An enabled change was detected on the associated pin.
Set when IOCAPx = 1 and a rising edge was detected on RAX, or when IOCANx = 1 and a falling edge was detected on RAX.
- 0 = No change was detected, or the user cleared the detected change.

15.2.6 ADC CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

1. Configure Port:
 - Disable pin output driver (Refer to the TRIS register)
 - Configure pin as analog (Refer to the ANSEL register)
 - Disable weak pull-ups either globally (Refer to the OPTION_REG register) or individually (Refer to the appropriate WPUx register).
2. Configure the ADC module:
 - Select ADC conversion clock
 - Configure voltage reference
 - Select ADC input channel
 - Turn on ADC module
3. Configure ADC interrupt (optional):
 - Clear ADC interrupt flag
 - Enable ADC interrupt
 - Enable peripheral interrupt
 - Enable global interrupt⁽¹⁾
4. Wait the required acquisition time⁽²⁾.
5. Start conversion by setting the GO/DONE bit.
6. Wait for ADC conversion to complete by one of the following:
 - Polling the GO/DONE bit
 - Waiting for the ADC interrupt (interrupts enabled)
7. Read ADC Result.
8. Clear the ADC interrupt flag (required if interrupt is enabled).

Note 1: The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

2: Refer to **Section 15.4 “ADC Acquisition Requirements”**.

EXAMPLE 15-1: ADC CONVERSION

```

;This code block configures the ADC
;for polling, Vdd and Vss references, FRC
;oscillator and AN0 input.
;
;Conversion start & polling for completion
; are included.
;
BANKSEL    ADCON1        ;
MOVLW     B'11110000'    ;Right justify, FRC
                                ;oscillator
MOVWF     ADCON1        ;Vdd and Vss Vref+
BANKSEL    TRISA         ;
BSF       TRISA,0        ;Set RA0 to input
BANKSEL    ANSEL         ;
BSF       ANSEL,0        ;Set RA0 to analog
BANKSEL    WPUA          ;
BCF       WPUA,0         ;Disable weak
                                pull-up on RA0
BANKSEL    ADCON0        ;
MOVLW     B'00000001'    ;Select channel AN0
MOVWF     ADCON0        ;Turn ADC On
CALL      SampleTime     ;Acquisition delay
BSF       ADCON0,ADGO    ;Start conversion
BTFSC     ADCON0,ADGO    ;Is conversion done?
GOTO      $-1            ;No, test again
BANKSEL    ADRESH        ;
MOVF      ADRESH,W       ;Read upper 2 bits
MOVWF     RESULTHI       ;store in GPR space
BANKSEL    ADRESL        ;
MOVF      ADRESL,W       ;Read lower 8 bits
MOVWF     RESULTLO       ;Store in GPR space

```

TABLE 17-3: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	99
CM1CON0	C1ON	C1OUT	C1OE	C1POL	—	C1SP	C1HYS	C1SYNC	131
CM1CON1	C1NTP	C1INTN	C1PCH<1:0>		—	C1NCH<2:0>			132
CMOUT	—	—	—	—	—	—	—	MC1OUT	132
DAC1CON0	DACEN	—	DACOE1	DACOE2	—	DACPSS	—	—	126
DAC1CON1	—	—	—	DACR<4:0>					126
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		107
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	64
PIE2	—	—	C1IE	—	—	NCO1IE	—	—	66
PIR2	—	—	C1IF	—	—	NCO1IF	—	—	69
PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	98
LATA	—	—	LATA5	LATA4	—	LATA2	LATA1	LATA0	99
TRISA	—	—	TRISA5	TRISA4	— ⁽¹⁾	TRISA2	TRISA1	TRISA0	98

Legend: — = unimplemented location, read as '0'. Shaded cells are unused by the comparator module.

Note 1: Unimplemented, read as '1'.

21.2 Register Definitions: PWM Control

REGISTER 21-1: PWMxCON: PWM CONTROL REGISTER

R/W-0/0	R/W-0/0	R-0/0	R/W-0/0	U-0	U-0	U-0	U-0
PWMxEN	PWMxOE	PWMxOUT	PWMxPOL	—	—	—	—
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

- bit 7 **PWMxEN:** PWM Module Enable bit
 1 = PWM module is enabled
 0 = PWM module is disabled
- bit 6 **PWMxOE:** PWM Module Output Enable bit
 1 = Output to PWMx pin is enabled
 0 = Output to PWMx pin is disabled
- bit 5 **PWMxOUT:** PWM Module Output Value bit
- bit 4 **PWMxPOL:** PWMx Output Polarity Select bit
 1 = PWM output is active-low
 0 = PWM output is active-high
- bit 3-0 **Unimplemented:** Read as '0'

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REGISTER 22-6: CLCxGLS1: GATE 2 LOGIC SELECT REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LCxG2D4T	LCxG2D4N	LCxG2D3T	LCxG2D3N	LCxG2D2T	LCxG2D2N	LCxG2D1T	LCxG2D1N
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7	LCxG2D4T: Gate 2 Data 4 True (non-inverted) bit 1 = lcx4T is gated into lcxg2 0 = lcx4T is not gated into lcxg2
bit 6	LCxG2D4N: Gate 2 Data 4 Negated (inverted) bit 1 = lcx4N is gated into lcxg2 0 = lcx4N is not gated into lcxg2
bit 5	LCxG2D3T: Gate 2 Data 3 True (non-inverted) bit 1 = lcx3T is gated into lcxg2 0 = lcx3T is not gated into lcxg2
bit 4	LCxG2D3N: Gate 2 Data 3 Negated (inverted) bit 1 = lcx3N is gated into lcxg2 0 = lcx3N is not gated into lcxg2
bit 3	LCxG2D2T: Gate 2 Data 2 True (non-inverted) bit 1 = lcx2T is gated into lcxg2 0 = lcx2T is not gated into lcxg2
bit 2	LCxG2D2N: Gate 2 Data 2 Negated (inverted) bit 1 = lcx2N is gated into lcxg2 0 = lcx2N is not gated into lcxg2
bit 1	LCxG2D1T: Gate 2 Data 1 True (non-inverted) bit 1 = lcx1T is gated into lcxg2 0 = lcx1T is not gated into lcxg2
bit 0	LCxG2D1N: Gate 2 Data 1 Negated (inverted) bit 1 = lcx1N is gated into lcxg2 0 = lcx1N is not gated into lcxg2

REGISTER 22-9: CLCDATA: CLC DATA OUTPUT

U-0	U-0	U-0	U-0	U-0	U-0	R-0	R-0
—	—	—	—	—	—	MLC2OUT	MLC1OUT
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-2 Unimplemented: Read as '0'

bit 1 MLC2OUT: Mirror copy of LC2OUT bit

bit 0 MLC1OUT: Mirror copy of LC1OUT bit

24.0 COMPLEMENTARY WAVEFORM GENERATOR (CWG) MODULE

The Complementary Waveform Generator (CWG) produces a complementary waveform with dead-band delay from a selection of input sources.

The CWG module has the following features:

- Selectable dead-band clock source control
- Selectable input sources
- Output enable control
- Output polarity control
- Dead-band control with independent 6-bit rising and falling edge dead-band counters
- Auto-shutdown control with:
 - Selectable shutdown sources
 - Auto-restart enable
 - Auto-shutdown pin override control

24.1 Fundamental Operation

The CWG generates two output waveforms from the selected input source.

The off-to-on transition of each output can be delayed from the on-to-off transition of the other output, thereby, creating a time delay immediately where neither output is driven. This is referred to as dead time and is covered in **Section 24.5 “Dead-Band Control”**. A typical operating waveform, with dead band, generated from a single input signal is shown in Figure 24-2.

It may be necessary to guard against the possibility of circuit faults or a feedback event arriving too late or not at all. In this case, the active drive must be terminated before the Fault condition causes damage. This is referred to as auto-shutdown and is covered in **Section 24.9 “Auto-Shutdown Control”**.

24.2 Clock Source

The CWG module allows the following clock sources to be selected:

- Fosc (system clock)
- HFINTOSC (16 MHz only)

The clock sources are selected using the G1CS0 bit of the CWGxCON0 register (Register 24-1).

24.3 Selectable Input Sources

The CWG generates the output waveforms from the input sources in Table 24-1.

TABLE 24-1: SELECTABLE INPUT SOURCES

Source Peripheral	Signal Name
Comparator C1	C1OUT_sync
PWM1	PWM1_out
PWM2	PWM2_out
PWM3	PWM3_out
PWM4	PWM4_out
NCO1	NCO1_out
CLC1	LC1_out

The input sources are selected using the GxIS<2:0> bits in the CWGxCON1 register (Register 24-2).

24.4 Output Control

Immediately after the CWG module is enabled, the complementary drive is configured with both CWGxA and CWGxB drives cleared.

24.4.1 OUTPUT ENABLES

Each CWG output pin has individual output enable control. Output enables are selected with the GxOEA and GxOEB bits of the CWGxCON0 register. When an output enable control is cleared, the module asserts no control over the pin. When an output enable is set, the override value or active PWM waveform is applied to the pin per the port priority selection. The output pin enables are dependent on the module enable bit, GxEN. When GxEN is cleared, CWG output enables and CWG drive levels have no effect.

24.4.2 POLARITY CONTROL

The polarity of each CWG output can be selected independently. When the output polarity bit is set, the corresponding output is active-high. Clearing the output polarity bit configures the corresponding output as active-low. However, polarity does not affect the override levels. Output polarity is selected with the GxPOLA and GxPOLB bits of the CWGxCON0 register.

TABLE 27-3: POWER-DOWN CURRENTS (I_{PD})^(1,2) (CONTINUED)

PIC12LF1501		Operating Conditions: (unless otherwise stated) Low-Power Sleep Mode						
PIC12F1501		Low-Power Sleep Mode, VREGPM = 1						
Param. No.	Device Characteristics	Min.	Typ†	Max. +85°C	Max. +125°C	Units	Conditions	
							V _{DD}	Note
D026		—	0.11	1.5	9.0	μA	1.8	ADC Current (Note 3), No conversion in progress
		—	0.12	2.7	12	μA	3.0	
D026		—	0.30	4.0	11	μA	2.3	ADC Current (Note 3), No conversion in progress
		—	0.35	5.0	13	μA	3.0	
		—	0.45	8.0	16	μA	5.0	
D026A*		—	250	—	—	μA	1.8	ADC Current (Note 3), Conversion in progress
		—	250	—	—	μA	3.0	
D026A*		—	280	—	—	μA	2.3	ADC Current (Note 3), Conversion in progress
		—	280	—	—	μA	3.0	
		—	280	—	—	μA	5.0	
D027		—	7	22	25	μA	1.8	Comparator, CxSP = 0
		—	8	23	27	μA	3.0	
D027		—	17	35	37	μA	2.3	Comparator, CxSP = 0
		—	18	37	38	μA	3.0	
		—	19	38	40	μA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** The peripheral Δ current can be determined by subtracting the base I_{PD} current from this limit. Max. values should be used when calculating total current consumption.
- Note 2:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{SS}.
- Note 3:** ADC clock source is FRC.

FIGURE 27-12: ADC CONVERSION TIMING (ADC CLOCK Fosc-BASED)

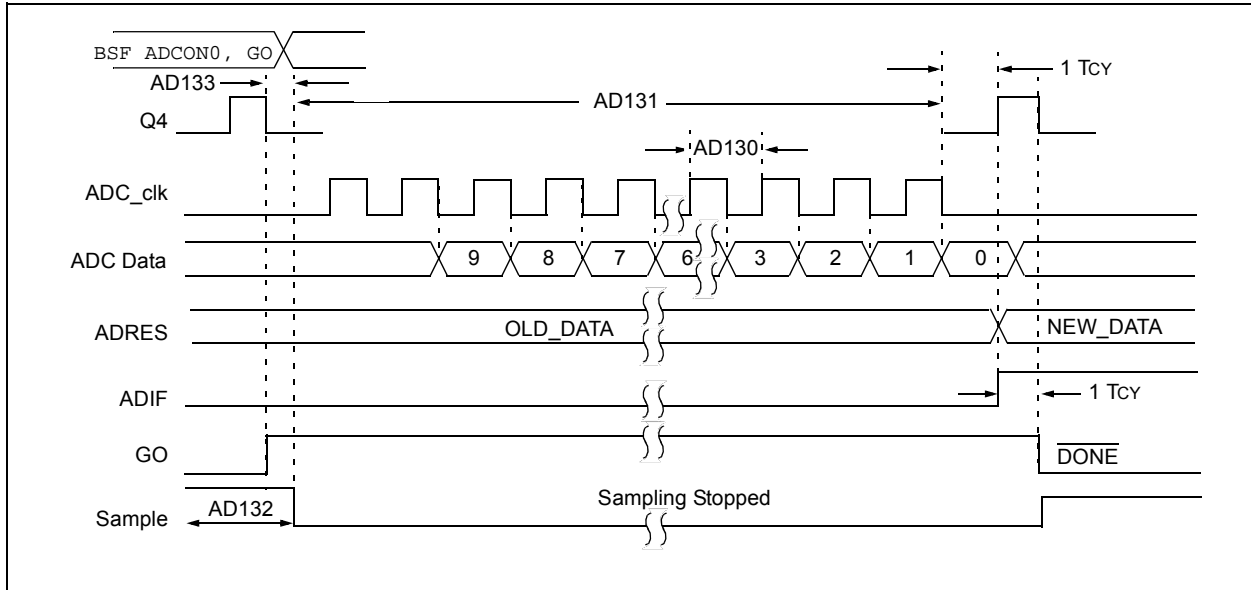
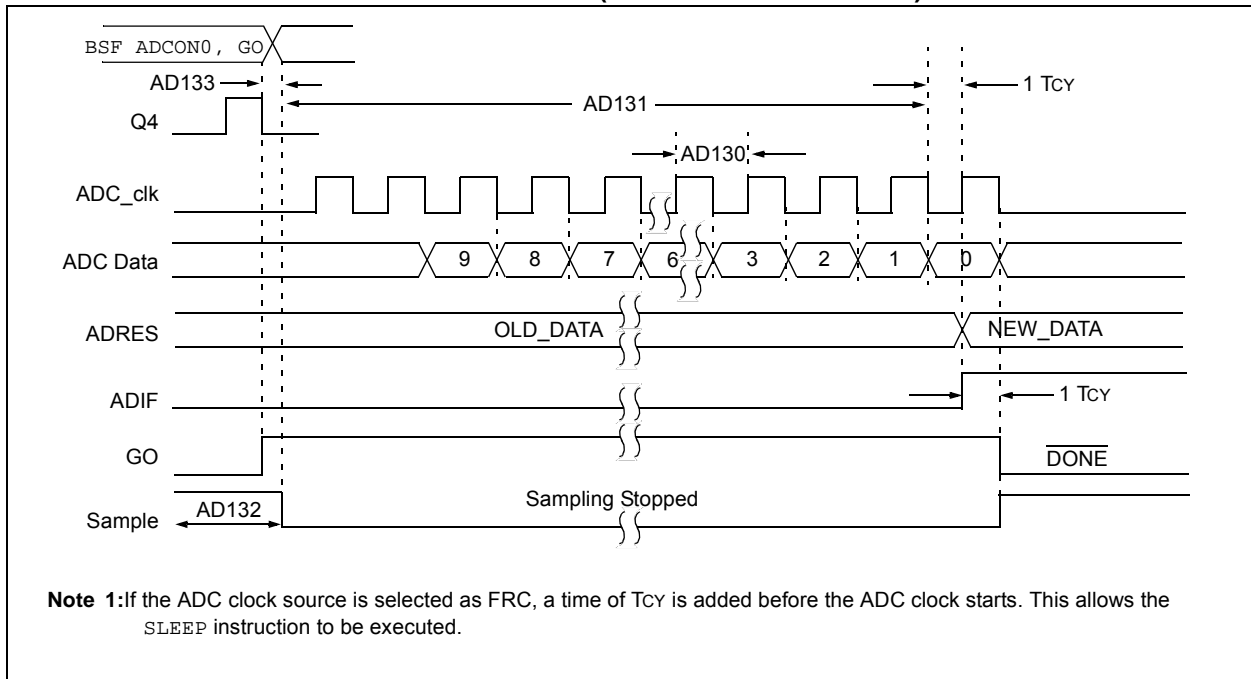


FIGURE 27-13: ADC CONVERSION TIMING (ADC CLOCK FROM FRC)



PIC12(L)F1501

FIGURE 28-3: I_{DD}, EXTERNAL CLOCK (ECL), LOW-POWER MODE, F_{osc} = 500 kHz, PIC12LF1501 ONLY

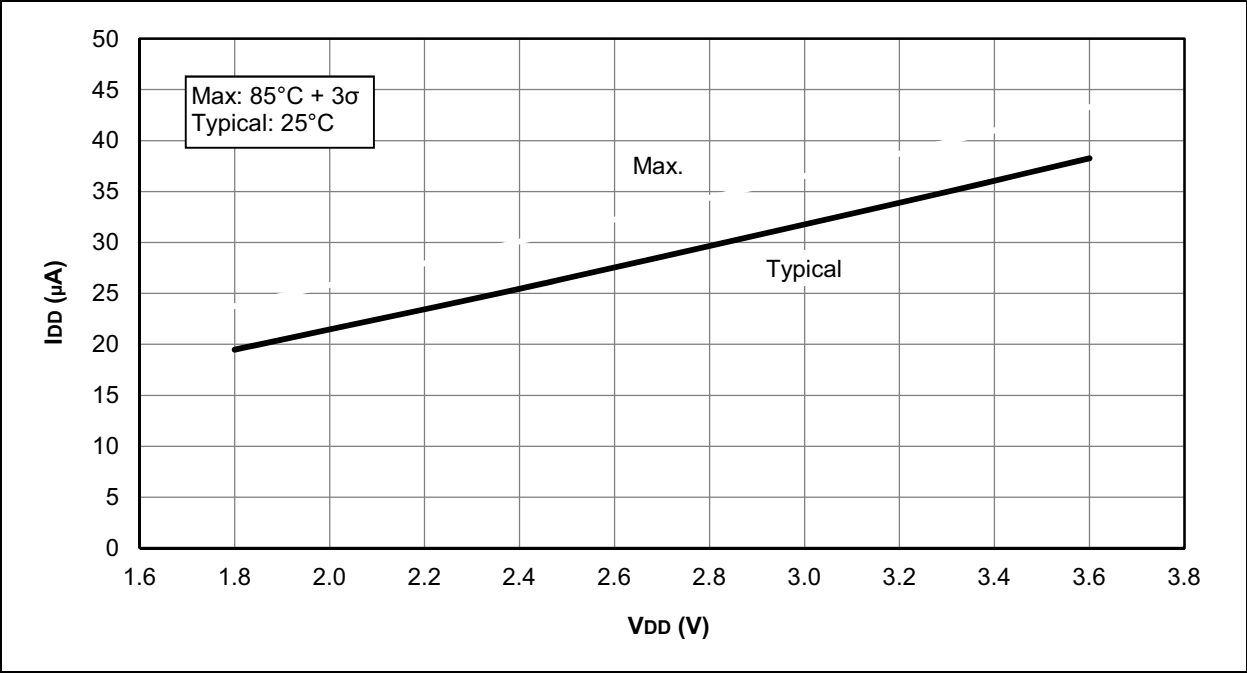


FIGURE 28-4: I_{DD}, EXTERNAL CLOCK (ECL), LOW-POWER MODE, F_{osc} = 500 kHz, PIC12F1501 ONLY

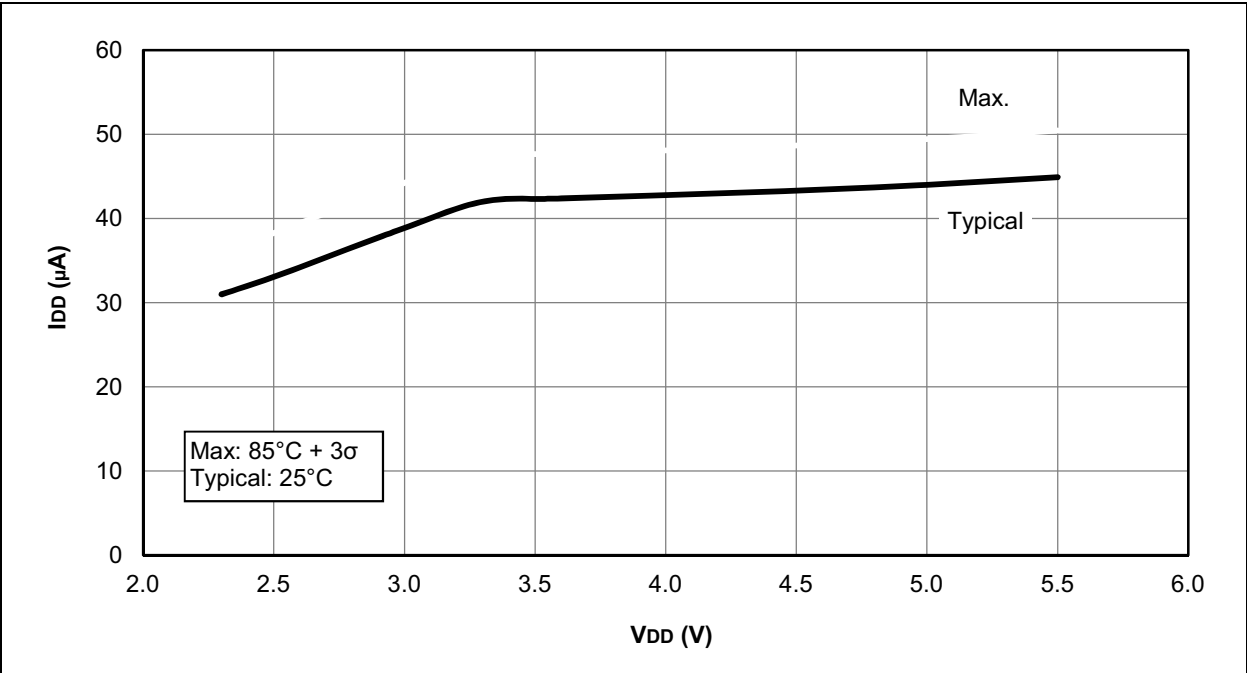


FIGURE 28-5: I_{DD} TYPICAL, EXTERNAL CLOCK (ECM), MEDIUM POWER MODE, PIC12LF1501 ONLY

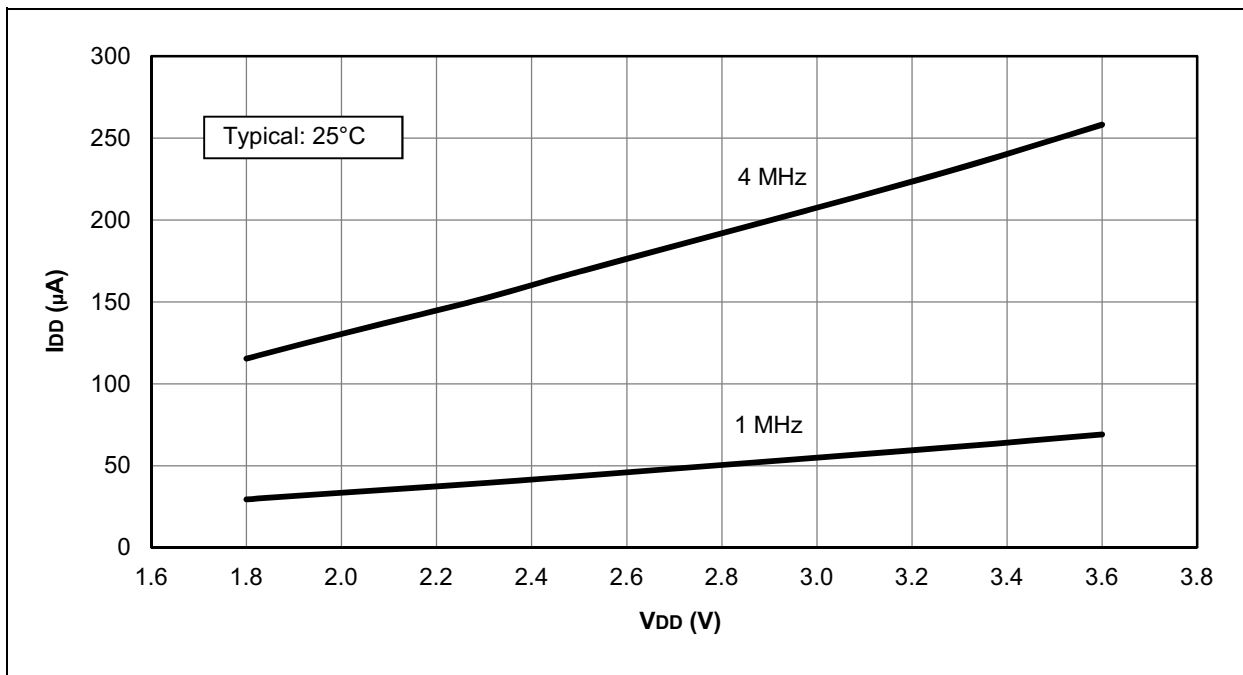
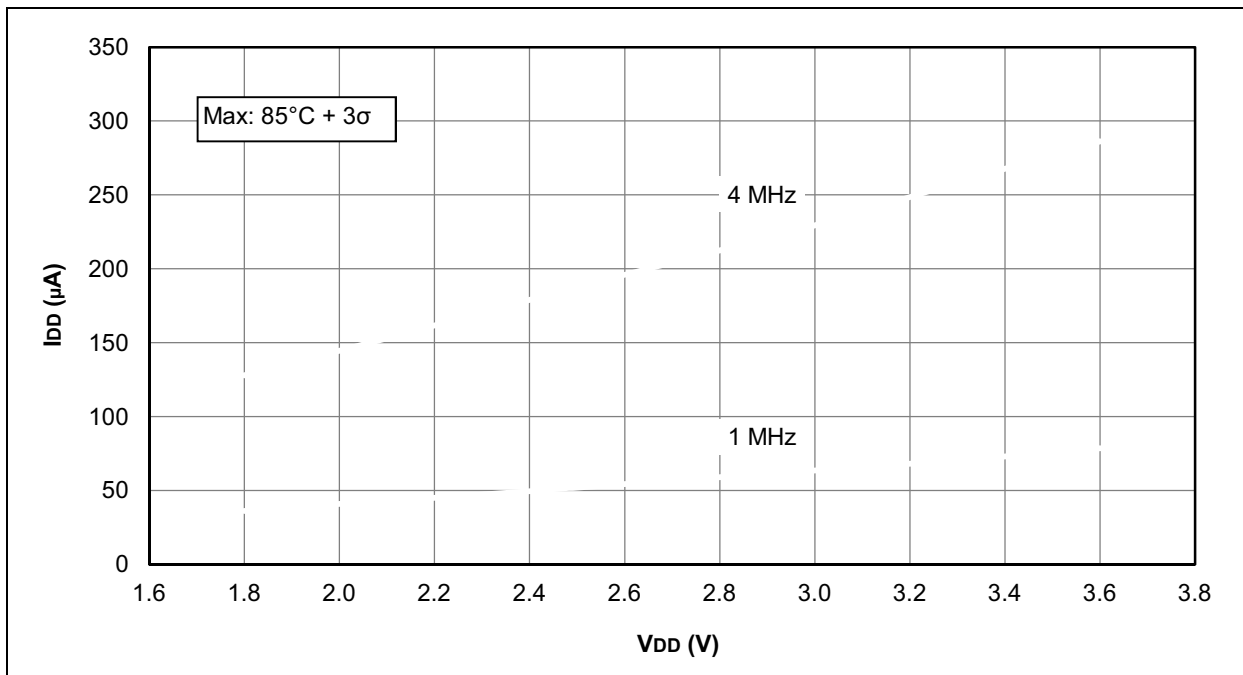


FIGURE 28-6: I_{DD} MAXIMUM, EXTERNAL CLOCK (ECM), MEDIUM POWER MODE, PIC12LF1501 ONLY



PIC12(L)F1501

FIGURE 28-23: I_{PD}, WATCHDOG TIMER (WDT), PIC12LF1501 ONLY

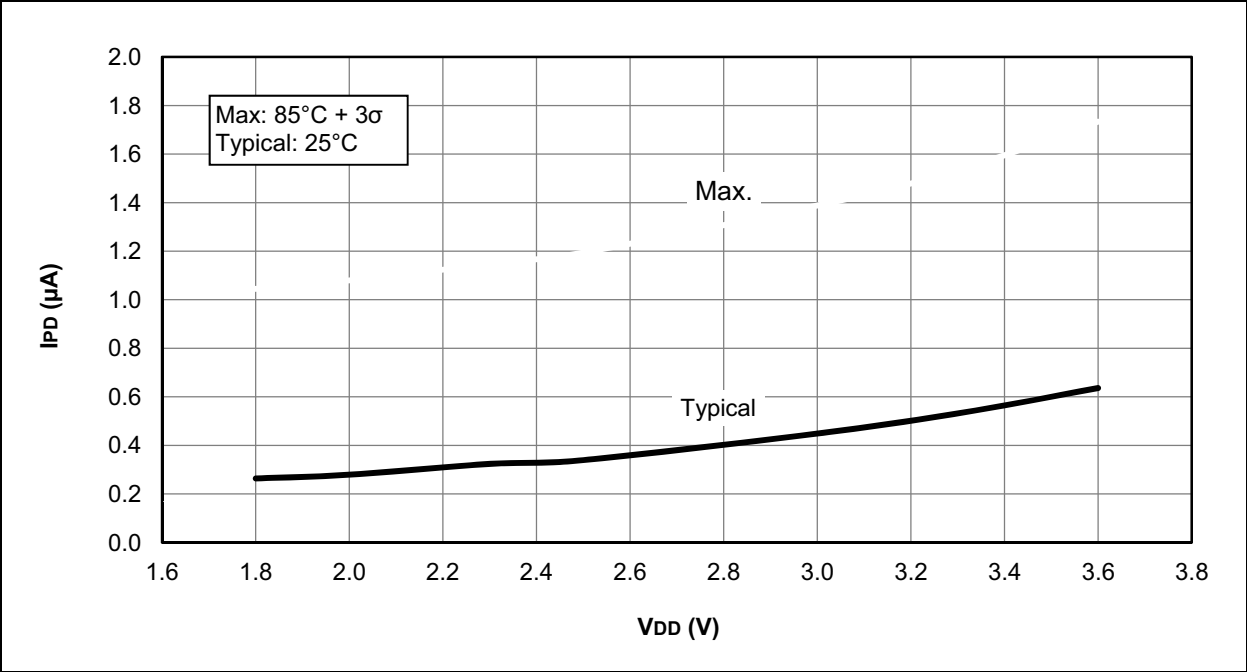
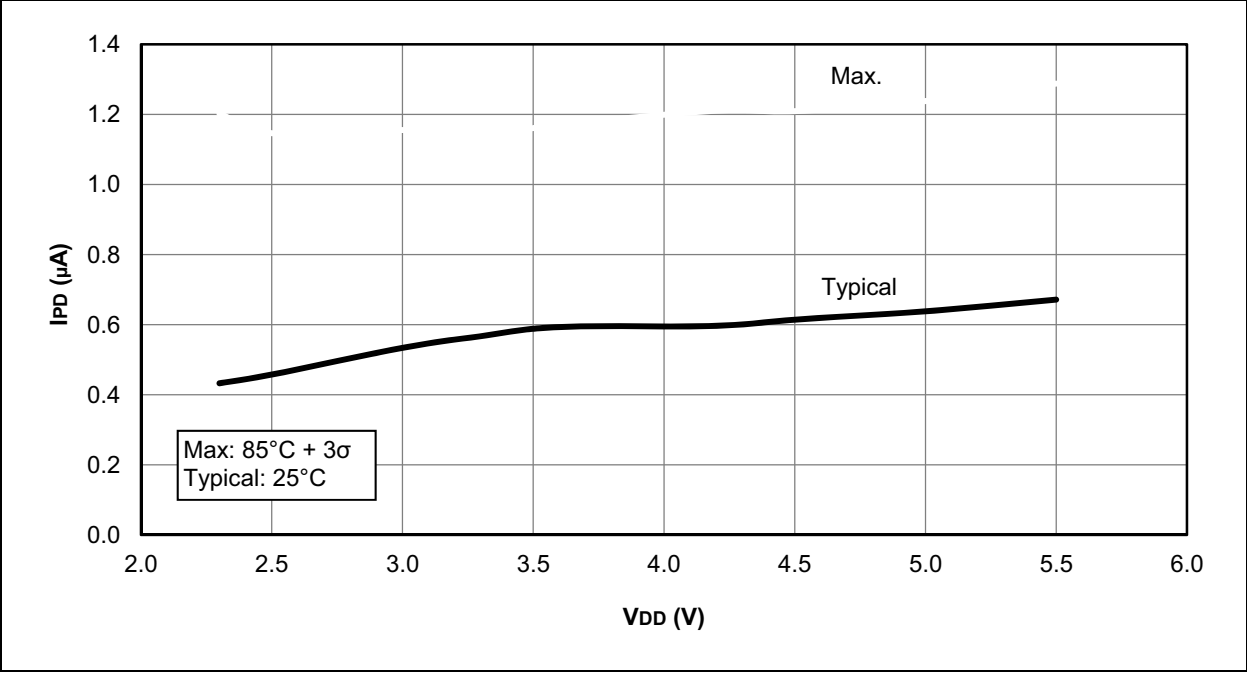


FIGURE 28-24: I_{PD}, WATCHDOG TIMER (WDT), PIC12F1501 ONLY



29.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

29.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

29.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

29.9 PICKit 3 In-Circuit Debugger/Programmer

The MPLAB PICKit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICKit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

29.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

29.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

29.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

TABLE 30-1: 8-LEAD 2x3 DFN (MC) TOP MARKING

Part Number	Marking
PIC12F1501-E/MC	BAK
PIC12F1501-I/MC	BAL
PIC12LF1501-E/MC	BAM
PIC12LF1501-I/MC	BAP

TABLE 30-2: 8-LEAD 3x3 DFN (MF) TOP MARKING

Part Number	Marking
PIC12F1501-E/MF	MFA1
PIC12F1501-I/MF	MFB1
PIC12LF1501-E/MF	MFC1
PIC12LF1501-I/MF	MFD1

TABLE 30-3: 8-LEAD 2X3 UDFN (MU) TOP MARKING

Part Number	Marking
PIC12F1501-E/MU	BAR
PIC12F1501-I/MU	BAQ
PIC12LF1501-E/MU	BAT
PIC12LF1501-I/MU	BAS

PIC12(L)F1501

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>[X]⁽¹⁾</u>	-	<u>X</u>	<u>/XX</u>	<u>XXX</u>																																																																								
Device	Tape and Reel Option		Temperature Range	Package	Pattern																																																																								
<table><tr><td>Device:</td><td colspan="5">PIC12LF1501, PIC12F1501</td></tr><tr><td>Tape and Reel Option:</td><td>Blank</td><td>= Standard packaging (tube or tray)</td><td></td><td></td><td></td></tr><tr><td></td><td>T</td><td>= Tape and Reel⁽¹⁾</td><td></td><td></td><td></td></tr><tr><td>Temperature Range:</td><td>I</td><td>= -40°C to +85°C (Industrial)</td><td></td><td></td><td></td></tr><tr><td></td><td>E</td><td>= -40°C to +125°C (Extended)</td><td></td><td></td><td></td></tr><tr><td>Package:</td><td>MC</td><td>= Micro Lead Frame (DFN) 2x3</td><td></td><td></td><td></td></tr><tr><td></td><td>MF</td><td>= Micro Lead Frame (DFN) 3x3</td><td></td><td></td><td></td></tr><tr><td></td><td>MS</td><td>= MSOP</td><td></td><td></td><td></td></tr><tr><td></td><td>MU</td><td>= Micro Lead Frame (UDFN) 2x3</td><td></td><td></td><td></td></tr><tr><td></td><td>P</td><td>= Plastic DIP</td><td></td><td></td><td></td></tr><tr><td></td><td>SN</td><td>= SOIC</td><td></td><td></td><td></td></tr><tr><td>Pattern:</td><td colspan="5">QTP, SQTP, Code or Special Requirements (blank otherwise)</td></tr></table>						Device:	PIC12LF1501, PIC12F1501					Tape and Reel Option:	Blank	= Standard packaging (tube or tray)					T	= Tape and Reel ⁽¹⁾				Temperature Range:	I	= -40°C to +85°C (Industrial)					E	= -40°C to +125°C (Extended)				Package:	MC	= Micro Lead Frame (DFN) 2x3					MF	= Micro Lead Frame (DFN) 3x3					MS	= MSOP					MU	= Micro Lead Frame (UDFN) 2x3					P	= Plastic DIP					SN	= SOIC				Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)				
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	SN	= SOIC																																																																											
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)																																																																												
<p>Examples:</p> <p>a) PIC12LF1501T - I/SN Tape and Reel, Industrial temperature, SOIC package</p> <p>b) PIC12F1501 - I/P Industrial temperature PDIP package</p> <p>c) PIC12F1501 - E/MF Extended temperature, DFN package</p> <p>Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.</p> <p>2: For other small form-factor package availability and marking information, please visit www.microchip.com/packaging or contact your local sales office.</p>																																																																													