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### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-DFN (3x3)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic12lf1501t-i-mf">https://www.e-xfl.com/product-detail/microchip-technology/pic12lf1501t-i-mf</a>

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### 3.3.5 DEVICE MEMORY MAPS

The memory maps for Bank 0 through Bank 31 are shown in the tables in this section.

**TABLE 3-3: PIC12(L)F1501 MEMORY MAP**

BANK 0		BANK 1		BANK 2		BANK 3		BANK 4		BANK 5		BANK 6		BANK 7	
000h	Core Registers (Table 3-2)	080h	Core Registers (Table 3-2)	100h	Core Registers (Table 3-2)	180h	Core Registers (Table 3-2)	200h	Core Registers (Table 3-2)	280h	Core Registers (Table 3-2)	300h	Core Registers (Table 3-2)	380h	Core Registers (Table 3-2)
00Bh		08Bh		10Bh		18Bh		20Bh		28Bh		30Bh		38Bh	
00Ch	PORTA	08Ch	TRISA	10Ch	LATA	18Ch	ANSELA	20Ch	WPUA	28Ch	—	30Ch	—	38Ch	—
00Dh	—	08Dh	—	10Dh	—	18Dh	—	20Dh	—	28Dh	—	30Dh	—	38Dh	—
00Eh	—	08Eh	—	10Eh	—	18Eh	—	20Eh	—	28Eh	—	30Eh	—	38Eh	—
00Fh	—	08Fh	—	10Fh	—	18Fh	—	20Fh	—	28Fh	—	30Fh	—	38Fh	—
010h	—	090h	—	110h	—	190h	—	210h	—	290h	—	310h	—	390h	—
011h	PIR1	091h	PIE1	111h	CM1CON0	191h	PMADRL	211h	—	291h	—	311h	—	391h	IOCAP
012h	PIR2	092h	PIE2	112h	CM1CON1	192h	PMADRH	212h	—	292h	—	312h	—	392h	IOCAN
013h	PIR3	093h	PIE3	113h	—	193h	PMDATL	213h	—	293h	—	313h	—	393h	IOCAF
014h	—	094h	—	114h	—	194h	PMDATH	214h	—	294h	—	314h	—	394h	—
015h	TMR0	095h	OPTION_REG	115h	CMOUT	195h	PMCON1	215h	—	295h	—	315h	—	395h	—
016h	TMR1L	096h	PCON	116h	BORCON	196h	PMCON2	216h	—	296h	—	316h	—	396h	—
017h	TMR1H	097h	WDTCON	117h	FVRCON	197h	VREGCON	217h	—	297h	—	317h	—	397h	—
018h	T1CON	098h	—	118h	DACCON0	198h	—	218h	—	298h	—	318h	—	398h	—
019h	T1GCON	099h	OSCCON	119h	DACCON1	199h	—	219h	—	299h	—	319h	—	399h	—
01Ah	TMR2	09Ah	OSCSTAT	11Ah	—	19Ah	—	21Ah	—	29Ah	—	31Ah	—	39Ah	—
01Bh	PR2	09Bh	ADRESL	11Bh	—	19Bh	—	21Bh	—	29Bh	—	31Bh	—	39Bh	—
01Ch	T2CON	09Ch	ADRESH	11Ch	—	19Ch	—	21Ch	—	29Ch	—	31Ch	—	39Ch	—
01Dh	—	09Dh	ADCON0	11Dh	APFCON	19Dh	—	21Dh	—	29Dh	—	31Dh	—	39Dh	—
01Eh	—	09Eh	ADCON1	11Eh	—	19Eh	—	21Eh	—	29Eh	—	31Eh	—	39Eh	—
01Fh	—	09Fh	ADCON2	11Fh	—	19Fh	—	21Fh	—	29Fh	—	31Fh	—	39Fh	—
020h	General Purpose Register 48 Bytes	0A0h	Unimplemented Read as '0'	120h	Unimplemented Read as '0'	1A0h	Unimplemented Read as '0'	220h	Unimplemented Read as '0'	2A0h	Unimplemented Read as '0'	320h	Unimplemented Read as '0'	3A0h	Unimplemented Read as '0'
04Fh															
050h															
06Fh	Common RAM	0EFh	Common RAM (Accesses 70h – 7Fh)	16Fh	Common RAM (Accesses 70h – 7Fh)	1EFh	Common RAM (Accesses 70h – 7Fh)	26Fh	Common RAM (Accesses 70h – 7Fh)	2EFh	Common RAM (Accesses 70h – 7Fh)	36Fh	Common RAM (Accesses 70h – 7Fh)	3EFh	Common RAM (Accesses 70h – 7Fh)
070h		0F0h		170h		1F0h		270h		2F0h		370h		3F0h	
07Fh		0FFh		17Fh		1FFh		27Fh		2FFh		37Fh		3FFh	

**Legend:**  = Unimplemented data memory locations, read as '0'

**TABLE 3-3: PIC12(L)F1501 MEMORY MAP (CONTINUED)**

BANK 8		BANK 9		BANK 10		BANK 11		BANK 12		BANK 13		BANK 14		BANK 15	
400h	Core Registers (Table 3-2)	480h	Core Registers (Table 3-2)	500h	Core Registers (Table 3-2)	580h	Core Registers (Table 3-2)	600h	Core Registers (Table 3-2)	680h	Core Registers (Table 3-2)	700h	Core Registers (Table 3-2)	780h	Core Registers (Table 3-2)
40Bh	—	48Bh	—	50Bh	—	58Bh	—	60Bh	—	68Bh	—	70Bh	—	78Bh	—
40Ch	—	48Ch	—	50Ch	—	58Ch	—	60Ch	—	68Ch	—	70Ch	—	78Ch	—
40Dh	—	48Dh	—	50Dh	—	58Dh	—	60Dh	—	68Dh	—	70Dh	—	78Dh	—
40Eh	—	48Eh	—	50Eh	—	58Eh	—	60Eh	—	68Eh	—	70Eh	—	78Eh	—
40Fh	—	48Fh	—	50Fh	—	58Fh	—	60Fh	—	68Fh	—	70Fh	—	78Fh	—
410h	—	490h	—	510h	—	590h	—	610h	—	690h	—	710h	—	790h	—
411h	—	491h	—	511h	—	591h	—	611h	PWM1DCL	691h	CWG1DBR	711h	—	791h	—
412h	—	492h	—	512h	—	592h	—	612h	PWM1DCH	692h	CWG1DBF	712h	—	792h	—
413h	—	493h	—	513h	—	593h	—	613h	PWM1CON	693h	CWG1CON0	713h	—	793h	—
414h	—	494h	—	514h	—	594h	—	614h	PWM2DCL	694h	CWG1CON1	714h	—	794h	—
415h	—	495h	—	515h	—	595h	—	615h	PWM2DCH	695h	CWG1CON2	715h	—	795h	—
416h	—	496h	—	516h	—	596h	—	616h	PWM2CON	696h	—	716h	—	796h	—
417h	—	497h	—	517h	—	597h	—	617h	PWM3DCL	697h	—	717h	—	797h	—
418h	—	498h	NCO1ACCL	518h	—	598h	—	618h	PWM3DCH	698h	—	718h	—	798h	—
419h	—	499h	NCO1ACCH	519h	—	599h	—	619h	PWM3CON	699h	—	719h	—	799h	—
41Ah	—	49Ah	NCO1ACCU	51Ah	—	59Ah	—	61Ah	PWM4DCL	69Ah	—	71Ah	—	79Ah	—
41Bh	—	49Bh	NCO1INCL	51Bh	—	59Bh	—	61Bh	PWM4DCH	69Bh	—	71Bh	—	79Bh	—
41Ch	—	49Ch	NCO1INCH	51Ch	—	59Ch	—	61Ch	PWM4CON	69Ch	—	71Ch	—	79Ch	—
41Dh	—	49Dh	—	51Dh	—	59Dh	—	61Dh	—	69Dh	—	71Dh	—	79Dh	—
41Eh	—	49Eh	NCO1CON	51Eh	—	59Eh	—	61Eh	—	69Eh	—	71Eh	—	79Eh	—
41Fh	—	49Fh	NCO1CLK	51Fh	—	59Fh	—	61Fh	—	69Fh	—	71Fh	—	79Fh	—
420h	Unimplemented Read as '0'	4A0h	Unimplemented Read as '0'	520h	Unimplemented Read as '0'	5A0h	Unimplemented Read as '0'	620h	Unimplemented Read as '0'	6A0h	Unimplemented Read as '0'	720h	Unimplemented Read as '0'	7A0h	Unimplemented Read as '0'
46Fh	Common RAM (Accesses 70h – 7Fh)	4EFh	Common RAM (Accesses 70h – 7Fh)	56Fh	Common RAM (Accesses 70h – 7Fh)	5EFh	Common RAM (Accesses 70h – 7Fh)	66Fh	Common RAM (Accesses 70h – 7Fh)	6EFh	Common RAM (Accesses 70h – 7Fh)	76Fh	Common RAM (Accesses 70h – 7Fh)	7EFh	Common RAM (Accesses 70h – 7Fh)
470h	—	4F0h	—	570h	—	5F0h	—	670h	—	6F0h	—	770h	—	7F0h	—
47Fh	—	4FFh	—	57Fh	—	5FFh	—	67Fh	—	6FFh	—	77Fh	—	7FFh	—

BANK 16		BANK 17		BANK 18		BANK 19		BANK 20		BANK 21		BANK 22		BANK 23	
800h	Core Registers (Table 3-2)	880h	Core Registers (Table 3-2)	900h	Core Registers (Table 3-2)	980h	Core Registers (Table 3-2)	A00h	Core Registers (Table 3-2)	A80h	Core Registers (Table 3-2)	B00h	Core Registers (Table 3-2)	B80h	Core Registers (Table 3-2)
80Bh	—	88Bh	—	90Bh	—	98Bh	—	A0Bh	—	A8Bh	—	B0Bh	—	B8Bh	—
80Ch	Unimplemented Read as '0'	88Ch	Unimplemented Read as '0'	90Ch	Unimplemented Read as '0'	98Ch	Unimplemented Read as '0'	A0Ch	Unimplemented Read as '0'	A8Ch	Unimplemented Read as '0'	B0Ch	Unimplemented Read as '0'	B8Ch	Unimplemented Read as '0'
86Fh	Common RAM (Accesses 70h – 7Fh)	8EFh	Common RAM (Accesses 70h – 7Fh)	96Fh	Common RAM (Accesses 70h – 7Fh)	9EFh	Common RAM (Accesses 70h – 7Fh)	A6Fh	Common RAM (Accesses 70h – 7Fh)	A6Fh	Common RAM (Accesses 70h – 7Fh)	B6Fh	Common RAM (Accesses 70h – 7Fh)	BEFh	Common RAM (Accesses 70h – 7Fh)
870h	—	8F0h	—	970h	—	9F0h	—	A70h	—	AF0h	—	B70h	—	BF0h	—
87Fh	—	8FFh	—	97Fh	—	9FFh	—	A7Fh	—	AFh	—	B7Fh	—	BFh	—

**Legend:**  = Unimplemented data memory locations, read as '0'

# PIC12(L)F1501

---

## 4.3 Code Protection

Code protection allows the device to be protected from unauthorized access. Internal access to the program memory is unaffected by any code protection setting.

### 4.3.1 PROGRAM MEMORY PROTECTION

The entire program memory space is protected from external reads and writes by the  $\overline{CP}$  bit in Configuration Words. When  $\overline{CP} = 0$ , external reads and writes of program memory are inhibited and a read will return all '0's. The CPU can continue to read program memory, regardless of the protection bit settings. Writing the program memory is dependent upon the write protection setting. See **Section 4.4 "Write Protection"** for more information.

## 4.4 Write Protection

Write protection allows the device to be protected from unintended self-writes. Applications, such as bootloader software, can be protected while allowing other regions of the program memory to be modified.

The WRT<1:0> bits in Configuration Words define the size of the program memory block that is protected.

## 4.5 User ID

Four memory locations (8000h-8003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are readable and writable during normal execution. See **Section 10.4 "User ID, Device ID and Configuration Word Access"** for more information on accessing these memory locations. For more information on checksum calculation, see the *"PIC12(L)F1501/PIC16(L)F150X Memory Programming Specification"* (DS41573).

# PIC12(L)F1501

**REGISTER 5-2: OSCSTAT: OSCILLATOR STATUS REGISTER**

U-0	U-0	U-0	R-0/q	U-0	U-0	R-0/q	R-0/q
—	—	—	HFIOFR	—	—	LFIOFR	HFIOFS
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
u = Bit is unchanged                      x = Bit is unknown                      -n/n = Value at POR and BOR/Value at all other Resets  
'1' = Bit is set                      '0' = Bit is cleared                      q = Conditional

bit 7-5                      **Unimplemented:** Read as '0'  
bit 4                      **HFIOFR:** High-Frequency Internal Oscillator Ready bit  
                                1 = HFINTOSC is ready  
                                0 = HFINTOSC is not ready  
bit 3-2                      **Unimplemented:** Read as '0'  
bit 1                      **LFIOFR:** Low-Frequency Internal Oscillator Ready bit  
                                1 = LFINTOSC is ready  
                                0 = LFINTOSC is not ready  
bit 0                      **HFIOFS:** High-Frequency Internal Oscillator Stable bit  
                                1 = HFINTOSC 16 MHz Oscillator is stable and is driving the INTOSC  
                                0 = HFINTOSC 16 MHz is not stable, the Start-up Oscillator is driving INTOSC

**TABLE 5-3: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	—	IRCF<3:0>				—	SCS<1:0>		49
OSCSTAT	—	—	—	HFIOFR	—	—	LFIOFR	HFIOFS	50

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

**TABLE 5-4: SUMMARY OF CONFIGURATION WORD WITH CLOCK SOURCES**

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	—	—	CLKOUTEN	BOREN<1:0>		—	38
	7:0	CP	MCLRE	PWRTE	WDTE<1:0>		—	FOSC<1:0>		

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

# PIC12(L)F1501

## REGISTER 7-5: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0
TMR1GIF	ADIF	—	—	—	—	TMR2IF	TMR1IF
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

- bit 7      **TMR1GIF:** Timer1 Gate Interrupt Flag bit  
1 = Interrupt is pending  
0 = Interrupt is not pending
- bit 6      **ADIF:** ADC Interrupt Flag bit  
1 = Interrupt is pending  
0 = Interrupt is not pending
- bit 5-2    **Unimplemented:** Read as '0'
- bit 1      **TMR2IF:** Timer2 to PR2 Interrupt Flag bit  
1 = Interrupt is pending  
0 = Interrupt is not pending
- bit 0      **TMR1IF:** Timer1 Overflow Interrupt Flag bit  
1 = Interrupt is pending  
0 = Interrupt is not pending

**Note:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Interrupt Enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

## 10.2.2 FLASH MEMORY UNLOCK SEQUENCE

The unlock sequence is a mechanism that protects the Flash program memory from unintended self-write programming or erasing. The sequence must be executed and completed without interruption to successfully complete any of the following operations:

- Row Erase
- Load program memory write latches
- Write of program memory write latches to program memory
- Write of program memory write latches to User IDs

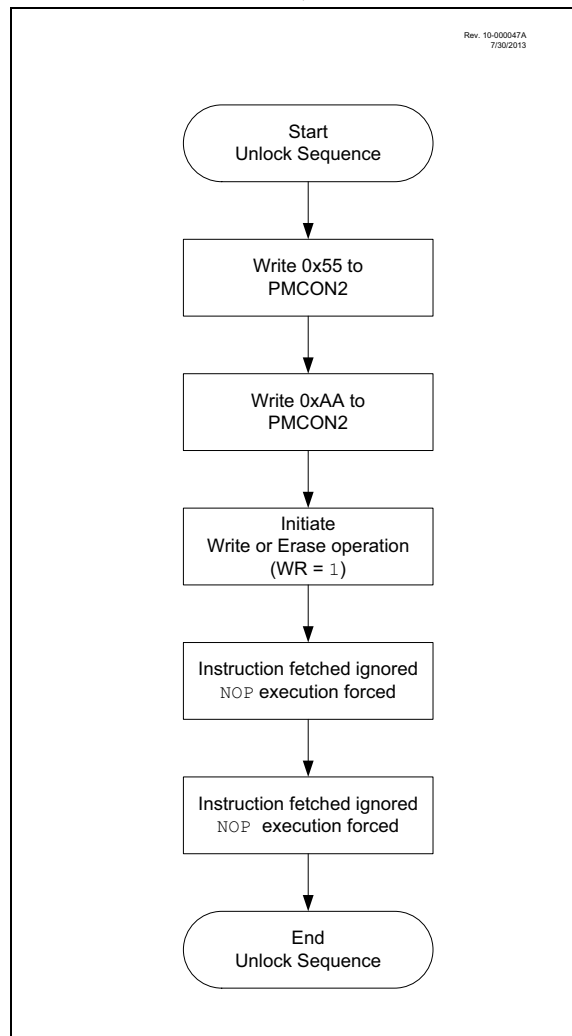
The unlock sequence consists of the following steps:

1. Write 55h to PMCON2
2. Write AAh to PMCON2
3. Set the WR bit in PMCON1
4. NOP instruction
5. NOP instruction

Once the WR bit is set, the processor will always force two NOP instructions. When an Erase Row or Program Row operation is being performed, the processor will stall internal operations (typical 2 ms), until the operation is complete and then resume with the next instruction. When the operation is loading the program memory write latches, the processor will always force the two NOP instructions and continue uninterrupted with the next instruction.

Since the unlock sequence must not be interrupted, global interrupts should be disabled prior to the unlock sequence and re-enabled after the unlock sequence is completed.

**FIGURE 10-3: FLASH PROGRAM MEMORY UNLOCK SEQUENCE FLOWCHART**





# PIC12(L)F1501

## EXAMPLE 10-2: ERASING ONE ROW OF PROGRAM MEMORY

```
; This row erase routine assumes the following:
; 1. A valid address within the erase row is loaded in ADDRH:ADDRL
; 2. ADDRH and ADDRL are located in shared data memory 0x70 - 0x7F (common RAM)

        BCF      INTCON,GIE      ; Disable ints so required sequences will execute properly
        BANKSEL  PMADRL
        MOVF     ADDRL,W         ; Load lower 8 bits of erase address boundary
        MOVWF    PMADRL
        MOVF     ADDRH,W        ; Load upper 6 bits of erase address boundary
        MOVWF    PMADRH
        BCF      PMCON1,CFGSR    ; Not configuration space
        BSF      PMCON1,FREE     ; Specify an erase operation
        BSF      PMCON1,WREN     ; Enable writes

        MOVLW    55h            ; Start of required sequence to initiate erase
        MOVWF    PMCON2         ; Write 55h
        MOVLW    0AAh          ;
        MOVWF    PMCON2         ; Write AAh
        BSF      PMCON1,WR      ; Set WR bit to begin erase
        NOP      ; NOP instructions are forced as processor starts
        NOP      ; row erase of program memory.
        ;
        ; The processor stalls until the erase process is complete
        ; after erase processor continues with 3rd instruction

        BCF      PMCON1,WREN    ; Disable writes
        BSF      INTCON,GIE     ; Enable interrupts
```

Required  
Sequence

## 15.2.6 ADC CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

1. Configure Port:
  - Disable pin output driver (Refer to the TRIS register)
  - Configure pin as analog (Refer to the ANSEL register)
  - Disable weak pull-ups either globally (Refer to the OPTION\_REG register) or individually (Refer to the appropriate WPUx register).
2. Configure the ADC module:
  - Select ADC conversion clock
  - Configure voltage reference
  - Select ADC input channel
  - Turn on ADC module
3. Configure ADC interrupt (optional):
  - Clear ADC interrupt flag
  - Enable ADC interrupt
  - Enable peripheral interrupt
  - Enable global interrupt<sup>(1)</sup>
4. Wait the required acquisition time<sup>(2)</sup>.
5. Start conversion by setting the GO/DONE bit.
6. Wait for ADC conversion to complete by one of the following:
  - Polling the GO/DONE bit
  - Waiting for the ADC interrupt (interrupts enabled)
7. Read ADC Result.
8. Clear the ADC interrupt flag (required if interrupt is enabled).

**Note 1:** The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

**2:** Refer to **Section 15.4 “ADC Acquisition Requirements”**.

## EXAMPLE 15-1: ADC CONVERSION

```

;This code block configures the ADC
;for polling, Vdd and Vss references, FRC
;oscillator and AN0 input.
;
;Conversion start & polling for completion
; are included.
;
BANKSEL    ADCON1    ;
MOVLW     B'11110000' ;Right justify, FRC
                                ;oscillator
MOVWF     ADCON1    ;Vdd and Vss Vref+
BANKSEL    TRISA      ;
BSF       TRISA,0    ;Set RA0 to input
BANKSEL    ANSEL      ;
BSF       ANSEL,0    ;Set RA0 to analog
BANKSEL    WPUA      ;
BCF       WPUA,0     ;Disable weak
                                pull-up on RA0
BANKSEL    ADCON0    ;
MOVLW     B'00000001' ;Select channel AN0
MOVWF     ADCON0    ;Turn ADC On
CALL      SampleTime ;Acquisition delay
BSF       ADCON0,ADGO ;Start conversion
BTFSCL    ADCON0,ADGO ;Is conversion done?
GOTO      $-1        ;No, test again
BANKSEL    ADRESH     ;
MOVF      ADRESH,W    ;Read upper 2 bits
MOVWF     RESULTHI    ;store in GPR space
BANKSEL    ADRESL     ;
MOVF      ADRESL,W    ;Read lower 8 bits
MOVWF     RESULTLO    ;Store in GPR space

```

## 23.2 Fixed Duty Cycle (FDC) Mode

In Fixed Duty Cycle (FDC) mode, every time the accumulator overflows (NCO\_overflow), the output is toggled. This provides a 50% duty cycle, provided that the increment value remains constant. For more information, see Figure 23-2.

The FDC mode is selected by clearing the NxPFM bit in the NCOxCON register.

## 23.3 Pulse Frequency (PF) Mode

In Pulse Frequency (PF) mode, every time the accumulator overflows (NCO\_overflow), the output becomes active for one or more clock periods. Once the clock period expires, the output returns to an inactive state. This provides a pulsed output.

The output becomes active on the rising clock edge immediately following the overflow event. For more information, see Figure 23-2.

The value of the active and inactive states depends on the polarity bit, NxPOL in the NCOxCON register.

The PF mode is selected by setting the NxPFM bit in the NCOxCON register.

### 23.3.1 OUTPUT PULSE WIDTH CONTROL

When operating in PF mode, the active state of the output can vary in width by multiple clock periods. Various pulse widths are selected with the NxPWS<2:0> bits in the NCOxCLK register.

When the selected pulse width is greater than the accumulator overflow time frame, the output of the NCOx operation is indeterminate.

## 23.4 Output Polarity Control

The last stage in the NCOx module is the output polarity. The NxPOL bit in the NCOxCON register selects the output polarity. Changing the polarity while the interrupts are enabled will cause an interrupt for the resulting output transition.

The NCOx output can be used internally by source code or other peripherals. Accomplish this by reading the NxOUT (read-only) bit of the NCOxCON register.

The NCOx output signal is available to the following peripherals:

- CLC
- CWG

## 23.5 Interrupts

When the accumulator overflows (NCO\_overflow), the NCOx Interrupt Flag bit, NCOxIF, of the PIRx register is set. To enable the interrupt event (NCO\_interrupt), the following bits must be set:

- NxEN bit of the NCOxCON register
- NCOxIE bit of the PIEx register
- PEIE bit of the INTCON register
- GIE bit of the INTCON register

The interrupt must be cleared by software by clearing the NCOxIF bit in the Interrupt Service Routine.

## 23.6 Effects of a Reset

All of the NCOx registers are cleared to zero as the result of a Reset.

## 23.7 Operation In Sleep

The NCO module operates independently from the system clock and will continue to run during Sleep, provided that the clock source selected remains active.

The HFINTOSC remains active during Sleep when the NCO module is enabled and the HFINTOSC is selected as the clock source, regardless of the system clock source selected.

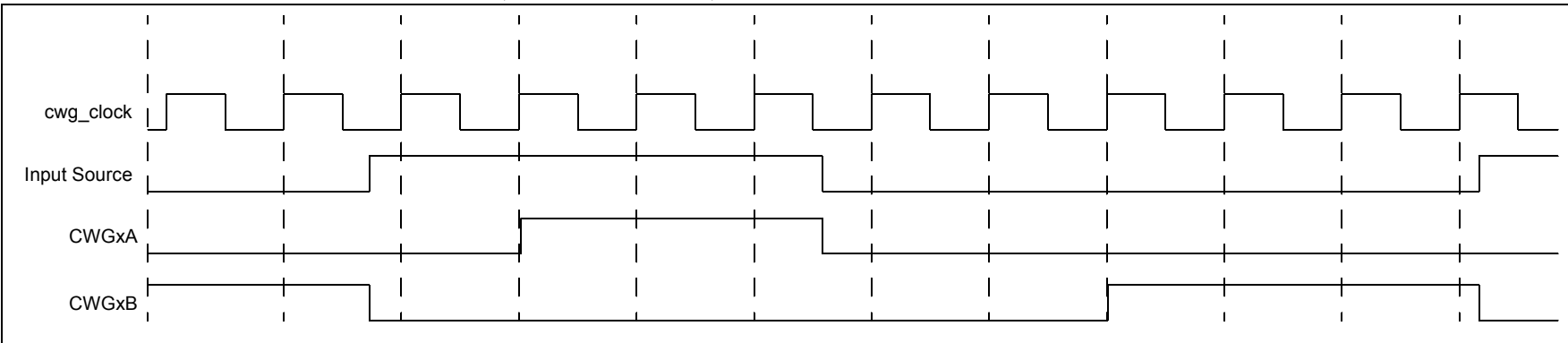
In other words, if the HFINTOSC is simultaneously selected as the system clock and the NCO clock source, when the NCO is enabled, the CPU will go idle during Sleep, but the NCO will continue to operate and the HFINTOSC will remain active.

This will have a direct effect on the Sleep mode current.

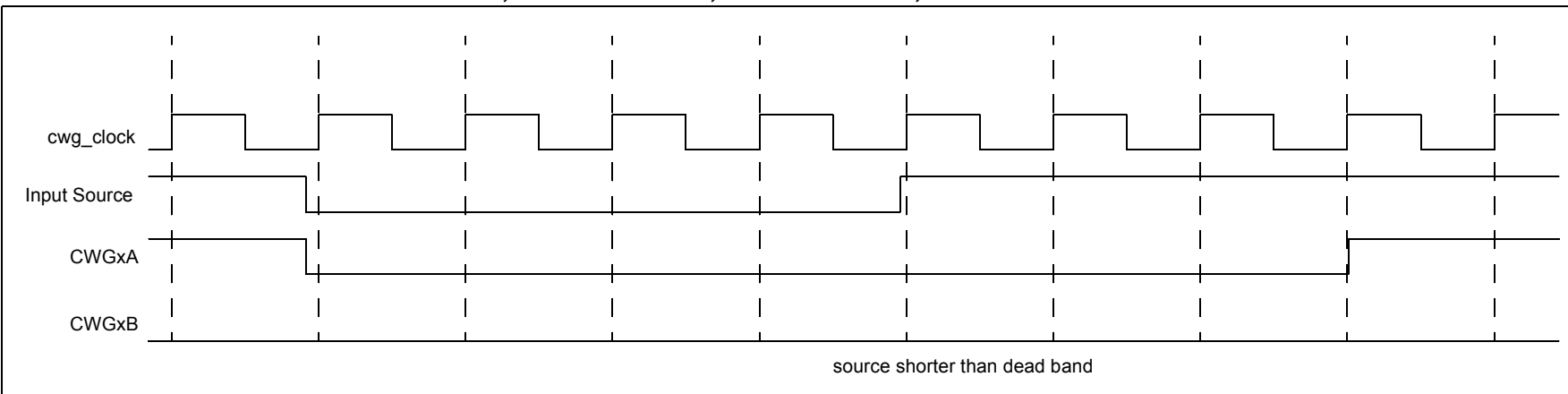
## 23.8 Alternate Pin Locations

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function register, APFCON. To determine which pins can be moved and what their default locations are upon a Reset, see **Section 11.1 “Alternate Pin Function”** for more information.

**FIGURE 24-3: DEAD-BAND OPERATION, CWGxDBR = 01H, CWGxDBF = 02H**



**FIGURE 24-4: DEAD-BAND OPERATION, CWGxDBR = 03H, CWGxDBF = 04H, SOURCE SHORTER THAN DEAD BAND**



## 27.0 ELECTRICAL SPECIFICATIONS

### 27.1 Absolute Maximum Ratings<sup>(†)</sup>

Ambient temperature under bias .....	-40°C to +125°C
Storage temperature .....	-65°C to +150°C
Voltage on pins with respect to V <sub>SS</sub>	
on V <sub>DD</sub> pin	
PIC12F1501 .....	-0.3V to +6.5V
PIC12LF1501 .....	-0.3V to +4.0V
on $\overline{\text{MCLR}}$ pin .....	-0.3V to +9.0V
on all other pins .....	-0.3V to (V <sub>DD</sub> + 0.3V)
Maximum current	
on V <sub>SS</sub> pin <sup>(1)</sup>	
-40°C ≤ T <sub>A</sub> ≤ +85°C .....	250 mA
+85°C ≤ T <sub>A</sub> ≤ +125°C .....	85 mA
on V <sub>DD</sub> pin <sup>(1)</sup>	
-40°C ≤ T <sub>A</sub> ≤ +85°C .....	250 mA
+85°C ≤ T <sub>A</sub> ≤ +125°C .....	85 mA
Sunk by any standard I/O pin .....	50 mA
Sourced by any standard I/O pin .....	50 mA
Clamp current, I <sub>K</sub> (V <sub>PIN</sub> < 0 or V <sub>PIN</sub> > V <sub>DD</sub> ) .....	±20 mA
Total power dissipation <sup>(2)</sup> .....	800 mW

**Note 1:** Maximum current rating requires even load distribution across I/O pins. Maximum current rating may be limited by the device package power dissipation characterizations, see Table 27-6 to calculate device specifications.

**2:** Power dissipation is calculated as follows:  $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$ .

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

# PIC12(L)F1501

**TABLE 27-2: SUPPLY CURRENT (IDD)<sup>(1,2)</sup>**

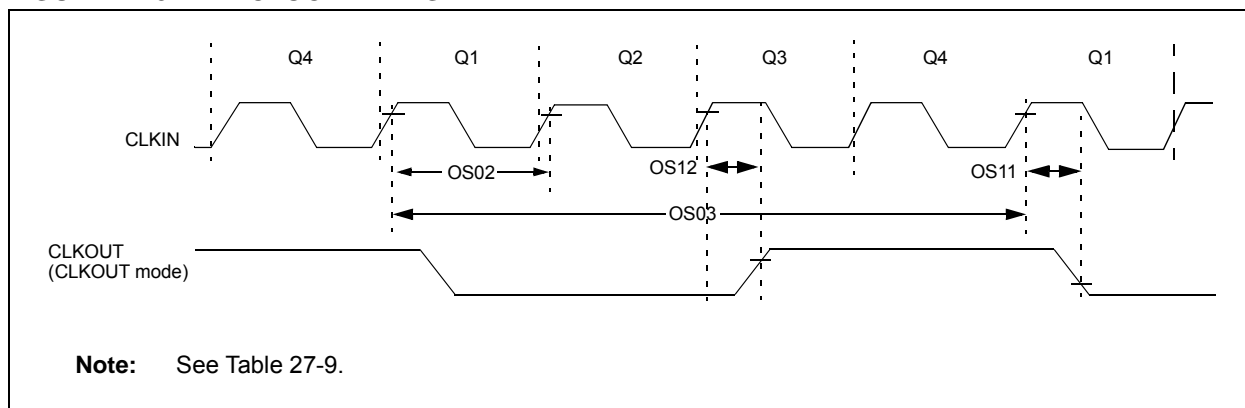
PIC12LF1501		Standard Operating Conditions (unless otherwise stated)					
PIC12F1501							
Param. No.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions	
						VDD	Note
D013		—	30	65	μA	1.8	Fosc = 1 MHz, External Clock (ECM), Medium Power mode
		—	55	100	μA	3.0	
D013		—	65	110	μA	2.3	Fosc = 1 MHz, External Clock (ECM), Medium Power mode
		—	85	140	μA	3.0	
		—	115	190	μA	5.0	
D014		—	115	190	μA	1.8	Fosc = 4 MHz, External Clock (ECM), Medium Power mode
		—	210	310	μA	3.0	
D014		—	180	270	μA	2.3	Fosc = 4 MHz, External Clock (ECM), Medium Power mode
		—	240	365	μA	3.0	
		—	295	460	μA	5.0	
D015		—	3.2	12	μA	1.8	Fosc = 31 kHz, LFINTOSC, -40°C ≤ TA ≤ +85°C
		—	5.4	20	μA	3.0	
D015		—	13	28	μA	2.3	Fosc = 31 kHz, LFINTOSC, -40°C ≤ TA ≤ +85°C
		—	15	30	μA	3.0	
		—	17	36	μA	5.0	
D016		—	215	360	μA	1.8	Fosc = 500 kHz, HFINTOSC
		—	275	480	μA	3.0	
D016		—	270	450	μA	2.3	Fosc = 500 kHz, HFINTOSC
		—	300	500	μA	3.0	
		—	350	620	μA	5.0	
D017*		—	410	660	μA	1.8	Fosc = 8 MHz, HFINTOSC
		—	630	970	μA	3.0	
D017*		—	530	750	μA	2.3	Fosc = 8 MHz, HFINTOSC
		—	660	1100	μA	3.0	
		—	730	1200	μA	5.0	
D018		—	600	940	μA	1.8	Fosc = 16 MHz, HFINTOSC
		—	970	1400	μA	3.0	
D018		—	780	1200	μA	2.3	Fosc = 16 MHz, HFINTOSC
		—	1000	1550	μA	3.0	
		—	1090	1700	μA	5.0	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VSS; MCLR = VDD; WDT disabled.
- 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

**FIGURE 27-5: CLOCK TIMING**



**TABLE 27-7: CLOCK OSCILLATOR TIMING REQUIREMENTS**

Standard Operating Conditions (unless otherwise stated)							
Param. No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
OS01	Fosc	External CLKIN Frequency <sup>(1)</sup>	DC	—	0.5	MHz	External Clock (ECL)
			DC	—	4	MHz	External Clock (ECM)
			DC	—	20	MHz	External Clock (ECH)
OS02	Tosc	External CLKIN Period <sup>(1)</sup>	50	—	∞	ns	External Clock (EC)
OS03	Tcy	Instruction Cycle Time <sup>(1)</sup>	200	Tcy	DC	ns	Tcy = 4/Fosc

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Instruction cycle period (Tcy) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to CLKIN pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

# PIC12(L)F1501

FIGURE 28-35:  $V_{OH}$  vs.  $I_{OH}$  OVER TEMPERATURE,  $V_{DD} = 5.5V$ , PIC12F1501 ONLY

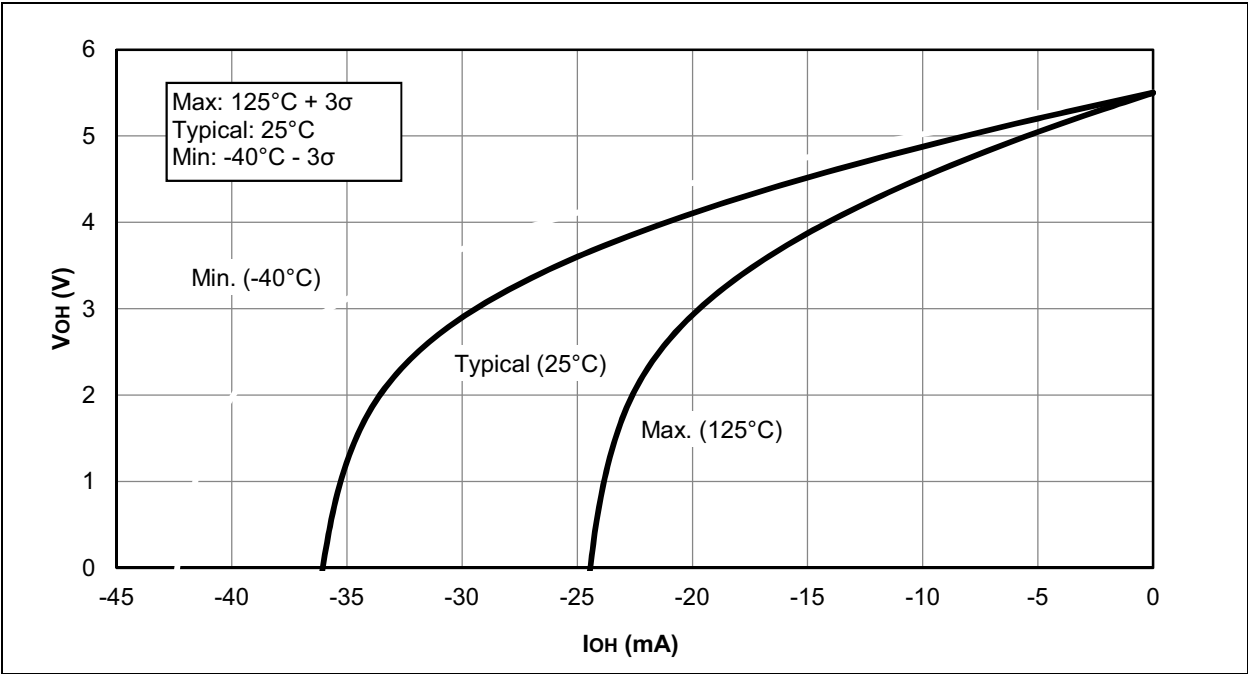
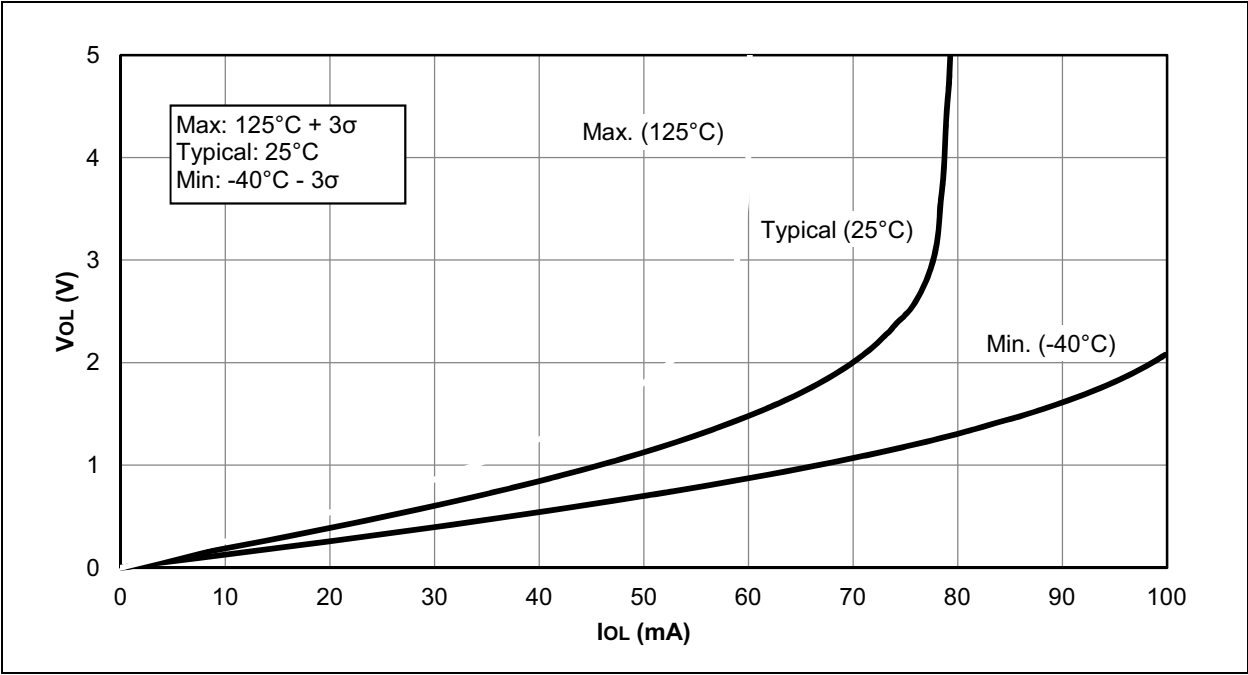


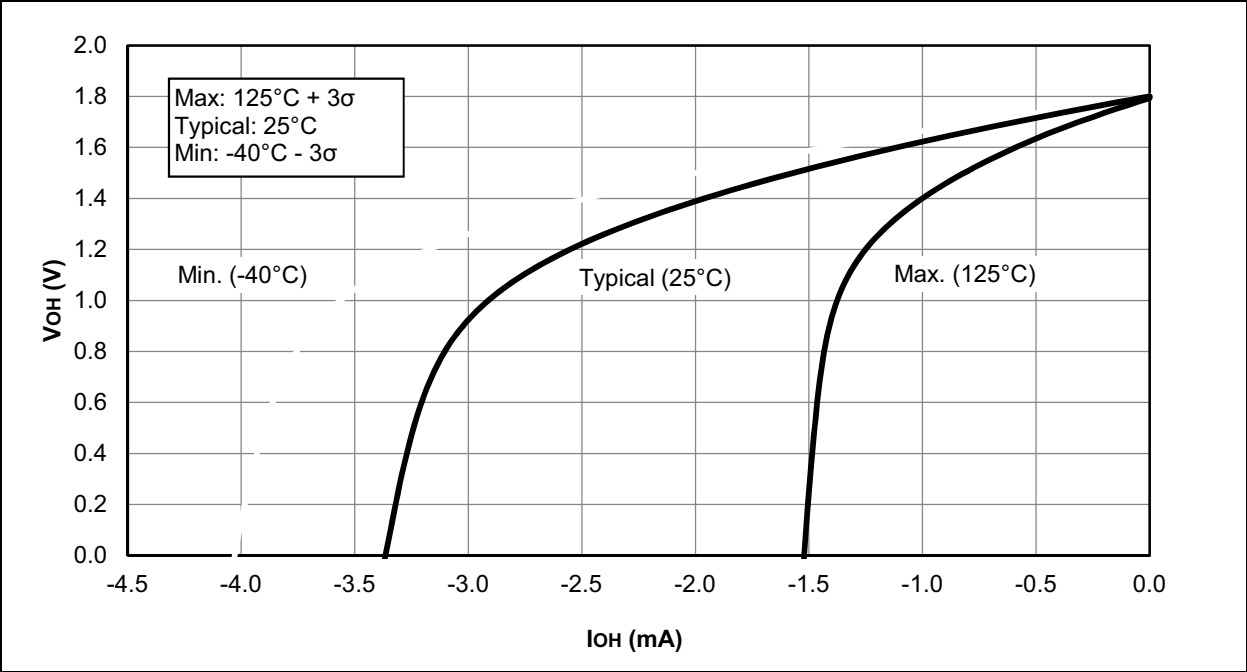
FIGURE 28-36:  $V_{OL}$  vs.  $I_{OL}$  OVER TEMPERATURE,  $V_{DD} = 5.5V$ , PIC12F1501 ONLY



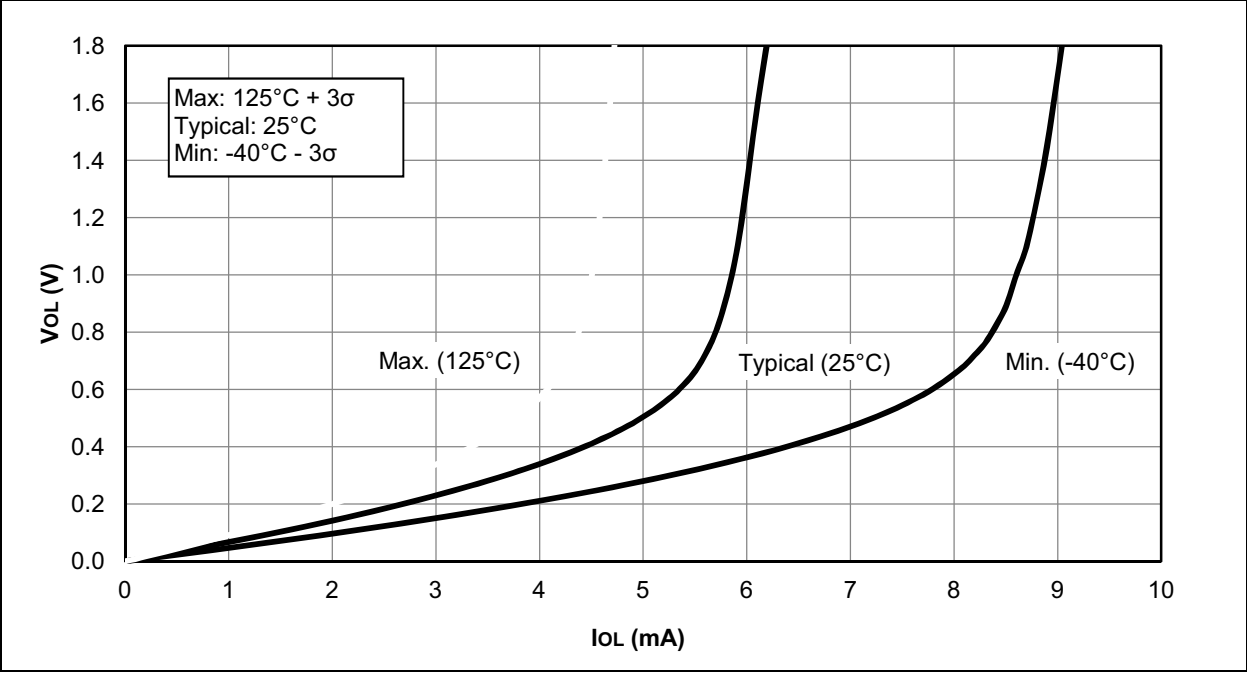


# PIC12(L)F1501

**FIGURE 28-39:  $V_{OH}$  vs.  $I_{OH}$  OVER TEMPERATURE,  $V_{DD} = 1.8V$ , PIC12LF1501 ONLY**



**FIGURE 28-40:  $V_{OL}$  vs.  $I_{OL}$  OVER TEMPERATURE,  $V_{DD} = 1.8V$ , PIC12LF1501 ONLY**



# PIC12(L)F1501

FIGURE 28-43: BROWN-OUT RESET VOLTAGE, BORV = 1, PIC12LF1501 ONLY

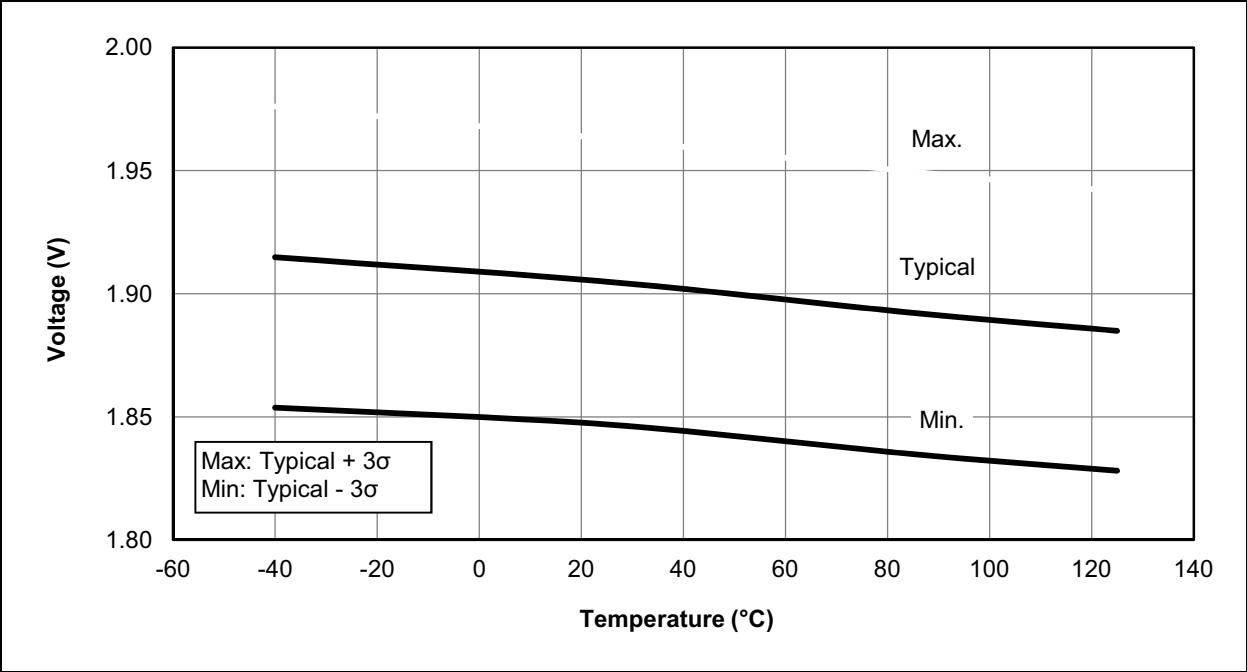
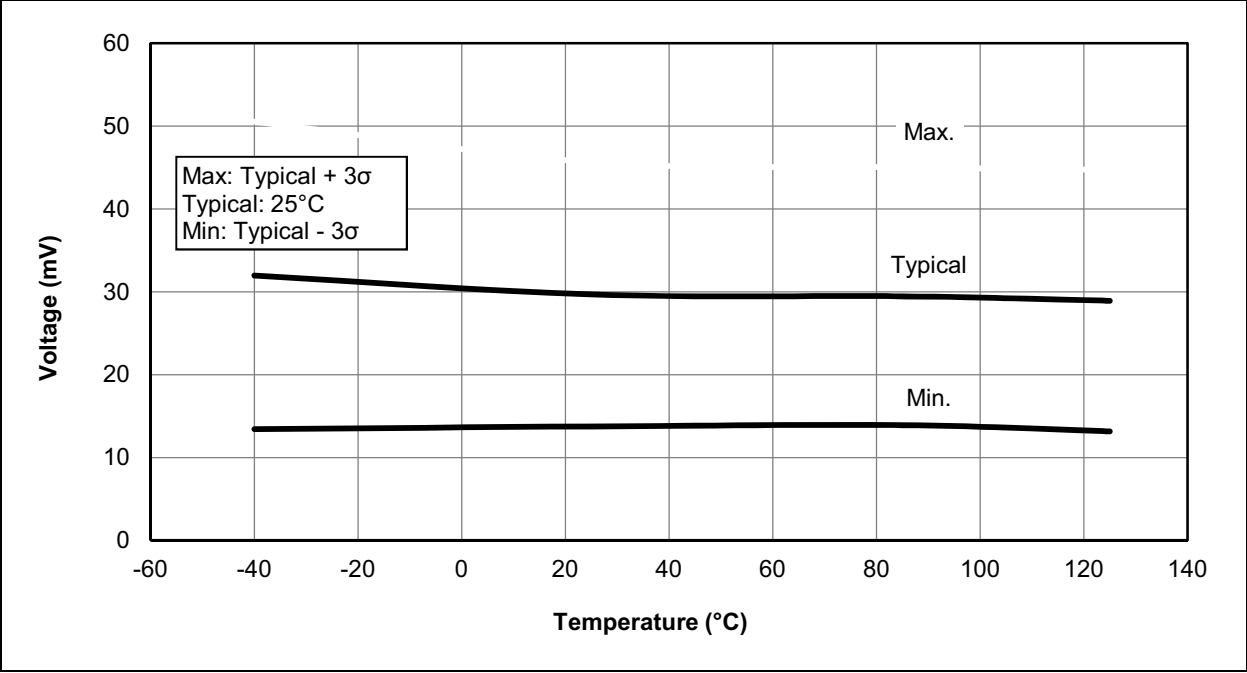
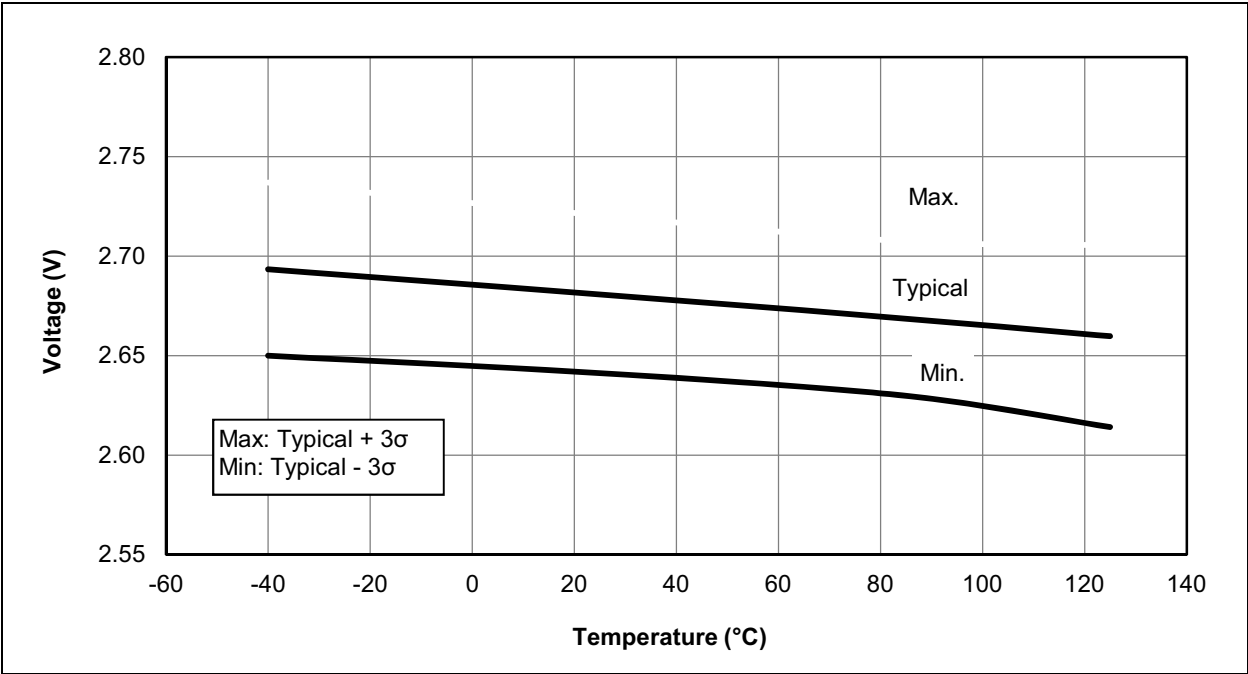


FIGURE 28-44: BROWN-OUT RESET HYSTERESIS, BORV = 1, PIC12LF1501 ONLY



# PIC12(L)F1501

FIGURE 28-47: BROWN-OUT RESET VOLTAGE, BORV = 0



## 29.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page ([www.microchip.com](http://www.microchip.com)) for the complete list of demonstration, development and evaluation kits.

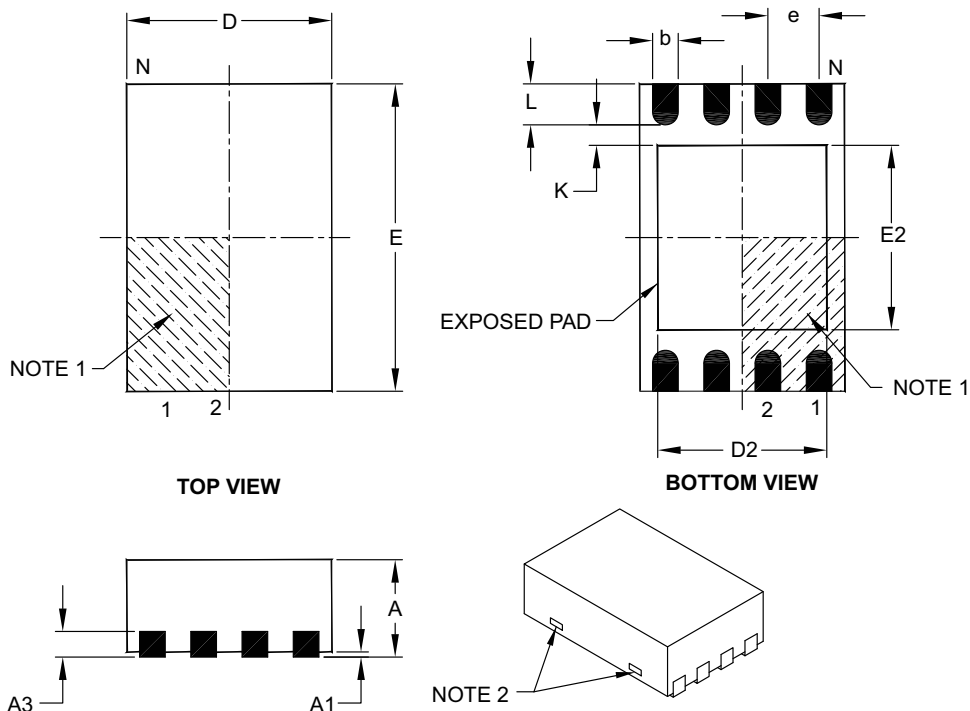
## 29.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

## 8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	2.00 BSC		
Overall Width	E	3.00 BSC		
Exposed Pad Length	D2	1.30	–	1.55
Exposed Pad Width	E2	1.50	–	1.75
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package may have one or more exposed tie bars at ends.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123C