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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	11
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-UQFN Exposed Pad
Supplier Device Package	16-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1824-i-jq

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3.5.2 LINEAR DATA MEMORY

The linear data memory is the region from FSR address 0x2000 to FSR address 0x29AF. This region is a virtual region that points back to the 80-byte blocks of GPR memory in all the banks.

Unimplemented memory reads as 0x00. Use of the linear data memory region allows buffers to be larger than 80 bytes because incrementing the FSR beyond one bank will go directly to the GPR memory of the next bank.

The 16 bytes of common memory are not included in the linear data memory region.

FIGURE 3-10: LINEAR DATA MEMORY MAP



3.5.3 PROGRAM FLASH MEMORY

To make constant data access easier, the entire program Flash memory is mapped to the upper half of the FSR address space. When the MSB of FSRnH is set, the lower 15 bits are the address in program memory which will be accessed through INDF. Only the lower eight bits of each memory location is accessible via INDF. Writing to the program Flash memory cannot be accomplished via the FSR/INDF interface. All instructions that access program Flash memory via the FSR/INDF interface will require one additional instruction cycle to complete.

FIGURE 3-11: PROGRAM FLASH MEMORY MAP



REGISTER 4-1: CONFIGURATION WORD 1

		R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1	
		FCMEN	IESO	CLKOUTEN	BORE	N<1:0>	CPD	
		bit 13					bit 8	
R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1	R/P-1/1	
CP	CP MCLRE PWRTE WDTE<1:0> FOSC<2:0>							
DIL 7							DIL U	
Legend:								
R = Readable bit P = Programmable bit U = Unimplemented bit, read as '1'								
'0' = Bit is clear	red	'1' = Bit is set		-n = Value when	blank or after E	3ulk Erase		
<u></u>								
bit 13	FCMEN: Fail-S	Safe Clock Monito	or Enable bit					
	1 = Fail-Safe C	Clock Monitor is e	nabled					
hit 12	IFSO: Internal	External Switcho	ver hit					
SIT 12	1 = Internal/Ex 0 = Internal/Ex	ternal Switchover	mode is enable mode is disabl	ed				
bit 11	CLKOUTEN: C	Clock Out Enable	bit					
	If FOSC Config	uration bits are s	et to LP, XT, HS	<u>S modes</u> :				
	All other FOSC	ignorea, CLKOU ; modes:	i tunction is disa	abled. Oscillator fur	iction on the C	LKOUT pin.		
	1 = CLKC	OUT function is di	sabled. I/O fund	tion on the CLKOU	IT pin.			
	0 = CLKC	OUT function is er	nabled on the C	LKOUT pin				
bit 10-9	BOREN<1:0>: 11 = BOR enal	Brown-out Rese	t Enable bits					
	10 = BOR enal	bled during opera	tion and disable	ed in Sleep				
	01 = BOR cont	rolled by SBORE	N bit of the BO	RCON register				
bit 8	CPD: Data Coo	de Protection bit ⁽²	2)					
	1 = Data memo	ory code protection	on is disabled					
	0 = Data memo	ory code protectio	on is enabled					
bit 7	CP: Code Prote	ection bit ⁽³⁾	action is disable	h				
	0 = Program m	emory code prot	ection is enable	d				
bit 6	MCLRE: RA3/	MCLR/VPP Pin Fu	unction Select b	it				
	$\frac{\text{If LVP bit} = 1}{\text{This bit is i}}$	anored						
	$\frac{\text{If LVP bit} = 0}{\text{If LVP bit} = 0}$	gnorea.						
	1 = MCLR	NPP pin function i	s MCLR; Weak	pull-up enabled.				
bit 5		VPP pin function i	s digitai input; ivi o bit(1)	CLR Internally disad	led; weak pull-	under control of	r wpua register.	
bit 5	1 = PWRT dis	abled	e bit					
	0 = PWRT en	abled						
bit 4-3	WDTE<1:0>: V	Vatchdog Timer E	Enable bit					
	11 = VUU enabled 10 = WDT enabled while running and disabled in Sleep							
	01 = WDT controlled by the SWDTEN bit in the WDTCON register							
	00 = WDT disa	abled						
Note 1: En	abling Brown-ou	t Reset does not	automatically e	nable Power-up Tin	ner.			

- 2: The entire data EEPROM will be erased when the code protection is turned off during an erase.
- 3: The entire program memory will be erased when the code protection is turned off.

FIGURE 5-3:

QUARTZ CRYSTAL OPERATION (LP, XT OR HS MODE)



- manufacturer data sheets for specifications and recommended application.2: Always verify oscillator performance over
 - the VDD and temperature range that is expected for the application.
- **3:** For oscillator design assistance, reference the following Microchip Applications Notes:
 - AN826, "Crystal Oscillator Basics and Crystal Selection for rfPIC[®] and PIC[®] Devices" (DS00826)
 - AN849, "Basic PIC[®] Oscillator Design" (DS00849)
 - AN943, "Practical PIC[®] Oscillator Analysis and Design" (DS00943)
 - AN949, "Making Your Oscillator Work" (DS00949)

FIGURE 5-4: CERAMIC RESONATOR OPERATION (XT OR HS MODE)



3: An additional parallel feedback resistor (RP) may be required for proper ceramic resonator operation.

5.2.1.3 Oscillator Start-up Timer (OST)

If the oscillator module is configured for LP, XT or HS modes, the Oscillator Start-up Timer (OST) counts 1024 oscillations from OSC1. This occurs following a Power-on Reset (POR) and when the Power-up Timer (PWRT) has expired (if configured), or a wake-up from Sleep. During this time, the program counter does not increment and program execution is suspended unless either FSCM or Two-Speed Start-up are enabled. In this case, the code will continue to execute at the selected INTOSC frequency while the OST is counting. The OST ensures that the oscillator circuit, using a quartz crystal resonator or ceramic resonator, has started and is providing a stable system clock to the oscillator module.

In order to minimize latency between external oscillator start-up and code execution, the Two-Speed Clock Start-up mode can be selected (see **Section 5.4 "Two-Speed Clock Start-up Mode"**).

R/W-0/0	R/W-0/0	R/W-0/0	R/W/HC-0/0	R/W-x/q	R/W-0/0	R/S/HC-0/0	R/S/HC-0/0	
EEPGD	CFGS	LWLO	FREE	WRERR	WREN	WR	RD	
bit 7						-	bit 0	
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimple	mented bit, read	1 as '0'		
S = Bit can onl	y be set	x = Bit is unknown		-n/n = Value at POR and BOR/Value at all other Resets				
'1' = Bit is set		'0' = Bit is cle	ared	HC = Bit is c	leared by hardw	/are		
bit 7	EEPGD: Has	h Program/Dat	ta EEPROM M	emory Select	bit			
	1 = Accesses 0 = Accesses	s data EEPRO	M memory	лу				
bit 6	CFGS: Flash	Program/Data	EEPROM or C	Configuration	Select bit			
	1 = Accesses	s Configuratior	, User ID and	Device ID Re	gisters			
	0 = Accesses	s Flash Progra	m or data EEP	ROM Memory	Ý			
bit 5	LWLO: Load	Write Latches	Only bit					
	$\frac{\text{If CFGS} = 1}{1 - 1}$	Configuration s	<u>space)</u> OR <u>CF(</u>	<u>GS = 0 and E</u>	EPGD = 1 (proc	<u>gram Flash)</u> :		
	⊥ = ⊺ne upda	next wrk com ated.	imand does no	ot initiate a w	nite; only the p	rogram memor	ry latches are	
	0 = The	next WR comm	nand writes a v	alue from EE	DATH:EEDATL	into program m	emory latches	
	and	initiates a write	e of all the data	stored in the	program memo	ry latches.		
	If CFGS = 0 a	and FFPGD =	0: (Accessing o	data FFPRON	<i>(</i> 1)			
	LWLO is igno	red. The next \	NR command i	initiates a writ	to the data El	EPROM.		
bit 4	FREE: Progra	am Flash Erase	e Enable bit					
	If CFGS = <u>1</u> (Configuration space) OR CFGS = <u>0</u> and EEPGD = <u>1</u> (program Flash):							
	1 = Performs an erase operation on the next WR command (cleared by hardware after comple-							
	tion of erase). 0 = Performs a write operation on the next WR command.							
	· · · ·							
	$\frac{\text{If EEPGD} = 0}{\text{EDEE} \text{ is imposed.}}$	and CFGS =	0: (Accessing	data EEPRO	M)			
hit 2			VR command v	will initiate do	in a erase cycle	and a write cyc	cie.	
DIL 3	1 = Condition	indicates an	ay bil improper prog	ram or erase	sequence atte	mot or termina	tion (hit is set	
	automatio	cally on any se	t attempt (write	e '1') of the W	R bit).			
	0 = The prog	ram or erase o	peration comp	leted normall	y			
bit 2	WREN: Progr	am/Erase Ena	ible bit					
	1 = Allows pr	ogram/erase c	ycles	am Flach and				
bit 1	WP: Write Co	ntrol bit	asing of progra	ann Fiash anu				
DIT I	1 = Initiates a	a program Flas	h or data EEP	ROM program	v/erase operatio	n		
	The oper	ation is self-tin	ned and the bit	is cleared by	hardware once	operation is co	mplete.	
	The WR	bit can only be	set (not cleare	ed) in software	e.			
hit 0		erase operation	In to the Flash	or data EEPF	convirus complete	e and inactive.		
DILU	$\mathbf{R}\mathbf{U}$: Read CO	nil UI DIL an program E	lach or data E		d Read takes		is cleared in	
	hardware	e. The RD bit c	an only be set	(not cleared)	in software.	one cycle. RD		
	0 = Does not	initiate a prog	ram Flash or d	ata EEPROM	data read			

REGISTER 11-5: EECON1: EEPROM CONTROL 1 REGISTER

12.4.3 PORTC FUNCTIONS AND OUTPUT PRIORITIES

Each PORTC pin is multiplexed with other functions. The pins, their combined functions and their output priorities are briefly described here. For additional information, refer to the appropriate section in this data sheet.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the lowest number in the following lists.

Analog input and some digital input functions are not included in the list below. These input functions can remain active when the pin is configured as an output. Certain digital input functions override other port functions and are included in the priority list.

<u>RC0</u>

- 1. SCL (MSSP) (PIC16(L)F1824 only)
- 2. SCK (MSSP) (PIC16(L)F1824 only)
- 3. P1D

<u>RC1</u>

- 1. SDA (MSSP) (PIC16(L)F1824 only)
- 2. P1C
- 3. CCP4 (PIC16(L)F1828 only)

<u>RC2</u>

- 1. SDO (MSSP) (PIC16(L)F1824 only)
- 2. P1D
- 3. P2B

<u>RC3</u>

- 1. SS (MSSP) (PIC16(L)F1824 only)
- 2. CCP2
- 3. P1C
- 4. P2A

<u>RC4</u>

- 1. MDOUT
- 2. SRNQ
- 3. C2OUT
- 4. TX/CK
- 5. P1B

<u>RC5</u>

- 1. RX/DT
- 2. CCP1/P1A

RC6 (PIC16(L)F1828 only)

- 1. SS (MSSP)
- 2. CCP4

RC7 (PIC16(L)F1828 only)

1. SDO (MSSP)

TABLE 18-2: SUMMARY OF REGISTERS ASSOCIATED WITH SR LATCH MOD

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	122
INLVLA	—	—	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	123
INLVLC	INLVLC7 ⁽¹⁾	INLVLC6 ⁽¹⁾	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	134
SRCON0	SRLEN	9	SRCLK<2:0>		SRQEN	SRNQEN	SRPS	SRPR	163
SRCON1	SRSPE	SRSCKE	SRSC2E	SRSC1E	SRRPE	SRRCKE	SRRC2E	SRRC1E	163
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	121
TRISC	TRISC7 ⁽¹⁾	TRISC6 ⁽¹⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	132

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the SR latch module.

Note 1: PIC16(L)F1828 only.

19.2 Comparator Control

Each comparator has two control registers: CMxCON0 and CMxCON1.

The CMxCON0 registers (see Register 19-1) contain Control and Status bits for the following:

- Enable
- Output selection
- Output polarity
- Speed/Power selection
- · Hysteresis enable
- Output synchronization

The CMxCON1 registers (see Register 19-2) contain Control bits for the following:

- Interrupt enable
- Interrupt edge polarity
- · Positive input channel selection
- · Negative input channel selection

19.2.1 COMPARATOR ENABLE

Setting the CxON bit of the CMxCON0 register enables the comparator for operation. Clearing the CxON bit disables the comparator resulting in minimum current consumption.

19.2.2 COMPARATOR OUTPUT SELECTION

The output of the comparator can be monitored by reading either the CxOUT bit of the CMxCON0 register or the MCxOUT bit of the CMOUT register. In order to make the output available for an external connection, the following conditions must be true:

- CxOE bit of the CMxCON0 register must be set
- · Corresponding TRIS bit must be cleared
- · CxON bit of the CMxCON0 register must be set

Note 1:	The CxOE bit of the CMxCON0 register
	overrides the PORT data latch. Setting
	the CxON bit of the CMxCON0 register
	has no impact on the port override.

2: The internal output of the comparator is latched with each instruction cycle. Unless otherwise specified, external outputs are not latched.

19.2.3 COMPARATOR OUTPUT POLARITY

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CxPOL bit of the CMxCON0 register. Clearing the CxPOL bit results in a non-inverted output.

Table 19-1 shows the output state versus input conditions, including polarity control.

TABLE 19-1: COMPARATOR OUTPUT STATE VS. INPUT CONDITIONS

Input Condition	CxPOL	CxOUT
CxVN > CxVP	0	0
CxVN < CxVP	0	1
CxVN > CxVP	1	1
CxVN < CxVP	1	0

19.2.4 COMPARATOR SPEED/POWER SELECTION

The trade-off between speed or power can be optimized during program execution with the CxSP control bit. The default state for this bit is '1' which selects the Normal Speed mode. Device power consumption can be optimized at the cost of slower comparator propagation delay by clearing the CxSP bit to '0'.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CM1CON0	C10N	C1OUT	C10E	C1POL		C1SP	C1HYS	C1SYNC	171
CM2CON0	C2ON	C2OUT	C2OE	C2POL	—	C2SP	C2HYS	C2SYNC	171
CM1CON1	C1NTP	C1INTN	C1PCI	H<1:0>	—	—	C1NCI	H<1:0>	172
CM2CON1	C2NTP	C2INTN	C2PCI	H<1:0>	—	—	C2NCI	H<1:0>	172
CMOUT	_	_	—	_	—	—	MC2OUT	MC10UT	172
DACCON0	DACEN	DACLPS	DACOE	_	DACPS	S<1:0>	—	DACNSS	159
DACCON1	_	—	—		DACR<4:0>				159
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFV	′R<1:0>	ADFV	R<1:0>	141
INLVLA	_	—	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	123
INLVLC	INLVLC7 ⁽¹⁾	INLVLC6 ⁽¹⁾	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	134
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	89
PIE2	OSFIE	C2IE	C1IE	EEIE	BCLIE	—	—	CCP2IE	91
PIR2	OSFIF	C2IF	C1IF	EEIF	BCLIF	—	—	CCP2IF	94
TRISA		_	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	121
TRISC	TRISC7 ⁽¹⁾	TRISC6 ⁽¹⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	132

Legend: — = unimplemented location, read as '0'. Shaded cells are unused by the comparator module.

Note 1: PIC16(L)F1828 only.

20.1.3 SOFTWARE PROGRAMMABLE PRESCALER

A software programmable prescaler is available for exclusive use with Timer0. The prescaler is enabled by clearing the PSA bit of the OPTION_REG register.

Note:	The Watchdog Timer (WDT) uses its own
	independent prescaler.

There are eight prescaler options for the Timer0 module ranging from 1:2 to 1:256. The prescale values are selectable via the PS<2:0> bits of the OPTION_REG register. In order to have a 1:1 prescaler value for the Timer0 module, the prescaler must be disabled by setting the PSA bit of the OPTION_REG register.

The prescaler is not readable or writable. All instructions writing to the TMR0 register will clear the prescaler.

20.1.4 TIMER0 INTERRUPT

Timer0 will generate an interrupt when the TMR0 register overflows from FFh to 00h. The TMR0IF interrupt flag bit of the INTCON register is set every time the TMR0 register overflows, regardless of whether or not the Timer0 interrupt is enabled. The TMR0IF bit can only be cleared in software. The Timer0 interrupt enable is the TMR0IE bit of the INTCON register.

Note:	The Timer0 interrupt cannot wake the
	processor from Sleep since the timer is
	frozen during Sleep.

20.1.5 8-BIT COUNTER MODE SYNCHRONIZATION

When in 8-Bit Counter mode, the incrementing edge on the T0CKI pin must be synchronized to the instruction clock. Synchronization can be accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the instruction clock. The high and low periods of the external clocking source must meet the timing requirements as shown in **Section 30.0 "Electrical Specifications"**.

20.1.6 OPERATION DURING SLEEP

Timer0 cannot operate while the processor is in Sleep mode. The contents of the TMR0 register will remain unchanged while the processor is in Sleep mode.





EXAMPLE 23-1: NO SYNCHRONIZATION (MDSHSYNC = 0, MDCLSYNC = 0)





Carrier High (CARH)	
Carrier Low (CARL)	
Modulator (MOD)	
MDCHSYNC = 1 MDCLSYNC = 0	
Active Carrier State	CARH / both CARL / CARH / both CARL





3 80K (CBCP = 6 CBCE = 6) * Shift register SSP ISR gand bit countiare reset 83P18UF to ø 832188 386 0.461* *** 读出 7 10 14. 2000 14 49 Ą. 痰 -* 137 *

FIGURE 25-8: SLAVE SELECT SYNCHRONOUS WAVEFORM

25.5.6 CLOCK STRETCHING

Clock stretching occurs when a device on the bus holds the SCL line low effectively pausing communication. The slave may stretch the clock to allow more time to handle data or prepare a response for the master device. A master device is not concerned with stretching as anytime it is active on the bus and not transferring data it is stretching. Any stretching done by a slave is invisible to the master software and handled by the hardware that generates SCL.

The CKP bit of the SSP1CON1 register is used to control stretching in software. Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. Setting CKP will release SCL and allow more communication.

25.5.6.1 Normal Clock Stretching

Following an ACK if the R/W bit of SSP1STAT is set, a read request, the slave hardware will clear CKP. This allows the slave time to update SSP1BUF with data to transfer to the master. If the SEN bit of SSP1CON2 is set, the slave hardware will always stretch the clock after the ACK sequence. Once the slave is ready; CKP is set by software and communication resumes.

- **Note 1:** The BF bit has no effect on if the clock will be stretched or not. This is different than previous versions of the module that would not stretch the clock, clear CKP, if SSP1BUF was read before the 9th falling edge of SCL.
 - 2: Previous versions of the module did not stretch the clock for a transmission if SSP1BUF was loaded before the 9th falling edge of SCL. It is now always cleared for read requests.

25.5.6.2 10-bit Addressing Mode

In 10-bit Addressing mode, when the UA bit is set, the clock is always stretched. This is the only time the SCL is stretched without CKP being cleared. SCL is released immediately after a write to SSP1ADD.

Note:	Previous versions of the module did not
	stretch the clock if the second address byte
	did not match.

25.5.6.3 Byte NACKing

When AHEN bit of SSP1CON3 is set; CKP is cleared by hardware after the eighth falling edge of SCL for a received matching address byte. When DHEN bit of SSP1CON3 is set; CKP is cleared after the eighth falling edge of SCL for received data.

Stretching after the eighth falling edge of SCL allows the slave to look at the received address or data and decide if it wants to ACK the received data.

25.5.7 CLOCK SYNCHRONIZATION AND THE CKP BIT

Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. However, clearing the CKP bit will not assert the SCL output low until the SCL output is already sampled low. Therefore, the CKP bit will not assert the SCL line until an external I^2C master device has already asserted the SCL line. The SCL output will remain low until the CKP bit is set and all other devices on the I^2C bus have released SCL. This ensures that a write to the CKP bit will not violate the minimum high time requirement for SCL (see Figure 25-23).



FIGURE 25-23: CLOCK SYNCHRONIZATION TIMING





25.6.10 SLEEP OPERATION

While in Sleep mode, the I²C slave module can receive addresses or data and when an address match or complete byte transfer occurs, wake the processor from Sleep (if the MSSP1 interrupt is enabled).

25.6.11 EFFECTS OF A RESET

A Reset disables the MSSP1 module and terminates the current transfer.

25.6.12 MULTI-MASTER MODE

In Multi-Master mode, the interrupt generation on the detection of the Start and Stop conditions allows the determination of when the bus is free. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP1 module is disabled. Control of the I²C bus may be taken when the P bit of the SSP1STAT register is set, or the bus is Idle, with both the S and P bits clear. When the bus is busy, enabling the SSP interrupt will generate the interrupt when the Stop condition occurs.

In multi-master operation, the SDA line must be monitored for arbitration to see if the signal level is the expected output level. This check is performed by hardware with the result placed in the BCL1IF bit.

The states where arbitration can be lost are:

- Address Transfer
- Data Transfer
- A Start Condition
- A Repeated Start Condition
- An Acknowledge Condition

25.6.13 MULTI -MASTER COMMUNICATION, BUS COLLISION AND BUS ARBITRATION

Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDA pin, arbitration takes place when the master outputs a '1' on SDA, by letting SDA float high and another master asserts a '0'. When the SCL pin floats high, data should be stable. If the expected data on SDA is a '1' and the data sampled on the SDA pin is '0', then a bus collision has taken place. The master will set the Bus Collision Interrupt Flag, BCL1IF and reset the I²C port to its Idle state (Figure 25-32).

If a transmit was in progress when the bus collision occurred, the transmission is halted, the BF flag is cleared, the SDA and SCL lines are deasserted and the SSP1BUF can be written to. When the user services the bus collision Interrupt Service Routine and if the I^2C bus is free, the user can resume communication by asserting a Start condition.

If a Start, Repeated Start, Stop or Acknowledge condition was in progress when the bus collision occurred, the condition is aborted, the SDA and SCL lines are deasserted and the respective control bits in the SSP1CON2 register are cleared. When the user services the bus collision Interrupt Service Routine and if the I²C bus is free, the user can resume communication by asserting a Start condition.

The master will continue to monitor the SDA and SCL pins. If a Stop condition occurs, the SSP1IF bit will be set.

A write to the SSP1BUF will start the transmission of data at the first data bit, regardless of where the transmitter left off when the bus collision occurred.

In Multi-Master mode, the interrupt generation on the detection of Start and Stop conditions allows the determination of when the bus is free. Control of the I^2C bus can be taken when the P bit is set in the SSP1STAT register, or the bus is Idle and the S and P bits are cleared.

26.5 EUSART Operation During Sleep

The EUSART will remain active during Sleep only in the Synchronous Slave mode. All other modes require the system clock and therefore cannot generate the necessary signals to run the Transmit or Receive Shift registers during Sleep.

Synchronous Slave mode uses an externally generated clock to run the Transmit and Receive Shift registers.

26.5.1 SYNCHRONOUS RECEIVE DURING SLEEP

To receive during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for Synchronous Slave Reception (see Section 26.4.2.4 "Synchronous Slave Reception Setup:").
- If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- The RCIF interrupt flag must be cleared by reading RCREG to unload any pending characters in the receive buffer.

Upon entering Sleep mode, the device will be ready to accept data and clocks on the RX/DT and TX/CK pins, respectively. When the data word has been completely clocked in by the external device, the RCIF interrupt flag bit of the PIR1 register will be set. Thereby, waking the processor from Sleep.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the Global Interrupt Enable (GIE) bit of the INTCON register is also set, then the Interrupt Service Routine at address 004h will be called.

26.5.2 SYNCHRONOUS TRANSMIT DURING SLEEP

To transmit during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for Synchronous Slave Transmission (see Section 26.4.2.2 "Synchronous Slave Transmission Setup:").
- The TXIF interrupt flag must be cleared by writing the output data to the TXREG, thereby filling the TSR and transmit buffer.
- If interrupts are desired, set the TXIE bit of the PIE1 register and the PEIE bit of the INTCON register.
- Interrupt enable bits TXIE of the PIE1 register and PEIE of the INTCON register must set.

Upon entering Sleep mode, the device will be ready to accept clocks on the TX/CK pin and transmit data on the RX/DT pin. When the data word in the TSR has been completely clocked out by the external device, the pending byte in the TXREG will transfer to the TSR and the TXIF flag will be set. Thereby, waking the processor from Sleep. At this point, the TXREG is available to accept another character for transmission, which will clear the TXIF flag.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the Global Interrupt Enable (GIE) bit is also set then the Interrupt Service Routine at address 0004h will be called.

26.5.3 ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function registers, APFCON0 and APFCON1. To determine which pins can be moved and what their default locations are upon a Reset, see **Section 12.1** "**Alternate Pin Function**" for more information.

29.0 INSTRUCTION SET SUMMARY

Each PIC16 instruction is a 14-bit word containing the operation code (opcode) and all required operands. The opcodes are broken into three broad categories.

- · Byte Oriented
- · Bit Oriented
- · Literal and Control

The literal and control category contains the most varied instruction word format.

Table 29-3 lists the instructions recognized by the MPASM $^{\rm TM}$ assembler.

All instructions are executed within a single instruction cycle, with the following exceptions, which may take two or three cycles:

- Subroutine takes two cycles (CALL, CALLW)
- Returns from interrupts or subroutines take two cycles (RETURN, RETLW, RETFIE)
- Program branching takes two cycles (GOTO, BRA, BRW, BTFSS, BTFSC, DECFSZ, INCSFZ)
- One additional instruction cycle will be used when any instruction references an indirect file register and the file select register is pointing to program memory.

One instruction cycle consists of 4 oscillator cycles; for an oscillator frequency of 4 MHz, this gives a nominal instruction execution rate of 1 MHz.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

29.1 Read-Modify-Write Operations

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

TABLE 29-1: OPCODE FIELD DESCRIPTIONS

Field	Description					
f	Register file address (0x00 to 0x7F)					
W	Working register (accumulator)					
b	Bit address within an 8-bit file register					
k	Literal field, constant data or label					
х	Don't care location (= 0 or 1). The assembler will generate code with x = 0 . It is the recommended form of use for compatibility with all Microchip software tools.					
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.					
n	FSR or INDF number. (0-1)					
mm	Pre-post increment-decrement mode selection					

TABLE 29-2: ABBREVIATION DESCRIPTIONS

Field	Description			
PC	Program Counter			
TO	Time-out bit			
С	Carry bit			
DC	Digit carry bit			
Z	Zero bit			
PD	Power-down bit			

















20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Units		MILLIMETERS			
Dimension Lim	its	MIN	NOM	MAX	
Number of Pins	Ν	20			
Pitch	е	1.27 BSC			
Overall Height	А	-	-	2.65	
Molded Package Thickness	A2	2.05	-	-	
Standoff §	A1	0.10	-	0.30	
Overall Width	Е	10.30 BSC			
Molded Package Width	E1	7.50 BSC			
Overall Length	D	12.80 BSC			
Chamfer (Optional)	h	0.25	-	0.75	
Foot Length	L	0.40	-	1.27	
Footprint	L1	1.40 REF			
Lead Angle	Θ	0°	-	-	
Foot Angle	φ	0°	-	8°	
Lead Thickness	С	0.20	-	0.33	
Lead Width	b	0.31	-	0.51	
Mold Draft Angle Top	α	5°	-	15°	
Mold Draft Angle Bottom	β	5°	-	15°	

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- 3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.
- 5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-094C Sheet 2 of 2



20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

	MILLIMETERS			
Dimensio	n Limits	MIN	NOM	MAX
Number of Pins	Ν	20		
Pitch	е	0.65 BSC		
Overall Height	Α	-	-	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	-	-
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1	1.25 REF		
Lead Thickness	С	0.09	-	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	-	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B