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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	11
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-VQFN Exposed Pad
Supplier Device Package	16-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1824-i-ml

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Name	Function	Input Type	Output Type	Description
RC3/AN7/CPS7/C12IN3-/	RC3	TTL	CMOS	General purpose I/O.
$P2A^{(1,2)}/CCP2^{(1,2)}/P1C^{(1,2)}/$	AN7	AN	_	A/D Channel 7 input.
	CPS7	AN	_	Capacitive sensing input 7.
	C12IN3-	AN	_	Comparator C1 or C2 negative input.
	P2A		CMOS	PWM output.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
	P1C		CMOS	PWM output.
	SS	ST	_	Slave Select input.
	MDMIN	ST	_	Modulator source input.
RC4/C2OUT/SRNQ/P1B/TX ^(1,2) /	RC4	TTL	CMOS	General purpose I/O.
CK ^(1,2) /MDOUT	C2OUT	_	CMOS	Comparator C2 output.
	SRNQ	_	CMOS	SR latch inverting output.
	P1B	_	CMOS	PWM output.
	TX	_	CMOS	USART asynchronous transmit.
	СК	ST	CMOS	USART synchronous clock.
	MDOUT		CMOS	Modulator output.
RC5/P1A/CCP1/RX ^(1,2) /DT ^(1,2) /	RC5	TTL	CMOS	General purpose I/O.
MDCIN2	P1A	_	CMOS	PWM output.
	CCP1	ST	CMOS	Capture/Compare/PWM1.
	RX	ST	—	USART asynchronous input.
	DT	ST	CMOS	USART synchronous data.
	MDCIN2	ST	—	Modulator Carrier Input 2.
VDD	VDD	Power	—	Positive supply.
Vss	Vss	Power	-	Ground reference.

TABLE 1-2:	PIC16(L)F1824 PINOUT DESCRIPTION (CONTINUED)
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Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C^{TM} = Schmitt Trigger input with I^2C HV = High Voltage XTAL = Crystal levels

Note 1: Pin functions can be moved using the APFCONO and APFCON1 registers (Register 12-1 and Register 12-2).

2: Default function location.

	-	1	1	
Name	Function	Input Type	Output Type	Description
RA5/CLKIN/OSC1/T1OSI/	RA5	TTL	CMOS	General purpose I/O.
T1CKI/P2A ⁽¹⁾ /CCP2 ⁽¹⁾	CLKIN	CMOS	_	External clock input (EC mode).
	OSC1	XTAL	_	Crystal/Resonator (LP, XT, HS modes).
	T10SI	XTAL	XTAL	Timer1 oscillator connection.
	T1CKI	ST	—	Timer1 clock input.
	P2A	_	CMOS	PWM output.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
RB4/AN10/CPS10/SDA1/SDI1	RB4	TTL	CMOS	General purpose I/O.
	AN10	AN	_	A/D Channel 10 input.
	CPS10	AN	—	Capacitive sensing input 10.
	SDA1	l ² C	OD	I ² C data input/output.
	SDI1	CMOS	_	SPI data input.
RB5/AN11/CPS11/RX ^(1,2) /DT ^(1,2)	RB5	TTL	CMOS	General purpose I/O.
	AN11	AN	_	A/D Channel 11 input.
	CPS11	AN	_	Capacitive sensing input 11.
	RX	ST	—	USART asynchronous input.
	DT	ST	CMOS	USART synchronous data.
RB6/SCL1/SCK1	RB6	TTL	CMOS	General purpose I/O.
	SCL1	l ² C	OD	I ² C™ clock 1.
	SCK1	ST	CMOS	SPI clock 1.
RB7/TX ^(1,2) /CK ^(1,2)	RB7	TTL	CMOS	General purpose I/O.
	ТΧ	—	CMOS	USART asynchronous transmit.
	СК	ST	CMOS	USART synchronous clock.
RC0/AN4/CPS4/C2IN+/P1D ⁽¹⁾	RC0	TTL	CMOS	General purpose I/O.
	AN4	AN	—	A/D Channel 4 input.
	CPS4	AN	_	Capacitive sensing input 4.
	C2IN+	AN	_	Comparator C2 positive input.
	P1D	—	CMOS	PWM output.
RC1/AN5/CPS5/C12IN1-/P1C(1)	RC1	TTL	CMOS	General purpose I/O.
	AN5	AN	—	A/D Channel 5 input.
	CPS5	AN	—	Capture/Compare/PWM4.
	C12IN1-	AN	_	Comparator C1 or C2 negative input.
	P1C	_	CMOS	PWM output.
RC2/AN6/CPS6/C12IN2-/	RC2	TTL	CMOS	General purpose I/O.
P1D ^(1,2) /P2B ^(1,2) /MDCIN1	AN6	AN	_	A/D Channel 6 input.
	CPS6	AN	_	Capacitive sensing input 6.
	C12IN2-	AN	—	Comparator C1 or C2 negative input.
	P1D	—	CMOS	PWM output.
	P2B	—	CMOS	PWM output.
	MDCIN1	ST	—	Modulator Carrier Input 1.
L				

TABLE 1-3: PIC16(L)F1828 PINOUT DESCRIPTION (CONTINUED)

Legend:AN = Analog input or outputCMOS = CMOS compatible input or outputOD = Open DrainTTL = TTL compatible inputST = Schmitt Trigger input with CMOS levels I^2C^{TM} = Schmitt Trigger input with I^2C HV = High VoltageXTAL = Crystallevels

Note 1: Pin functions can be moved using the APFCONO and APFCON1 registers (Register 12-1 and Register 12-2).

2: Default function location.

FIGURE 2-1: CORE BLOCK DIAGRAM



5.0 OSCILLATOR MODULE (WITH FAIL-SAFE CLOCK MONITOR)

5.1 Overview

The oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 5-1 illustrates a block diagram of the oscillator module.

Clock sources can be supplied from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system clock source can be supplied from one of two internal oscillators and PLL circuits, with a choice of speeds selectable via software. Additional clock features include:

- Selectable system clock source between external or internal sources via software.
- Two-Speed Start-up mode, which minimizes latency between external oscillator start-up and code execution.
- Fail-Safe Clock Monitor (FSCM) designed to detect a failure of the external clock source (LP, XT, HS, EC or RC modes) and switch automatically to the internal oscillator.
- Oscillator Start-up Timer (OST) ensures stability of crystal oscillator sources

The oscillator module can be configured in one of eight clock modes.

- 1. ECL External Clock Low-Power mode (0 MHz to 0.5 MHz)
- 2. ECM External Clock Medium-Power mode (0.5 MHz to 4 MHz)
- 3. ECH External Clock High-Power mode (4 MHz to 32 MHz)
- 4. LP 32 kHz Low-Power Crystal mode.
- 5. XT Medium Gain Crystal or Ceramic Resonator Oscillator mode (up to 4 MHz)
- HS High Gain Crystal or Ceramic Resonator mode (4 MHz to 20 MHz)
- 7. RC External Resistor-Capacitor (RC).
- 8. INTOSC Internal oscillator (31 kHz to 32 MHz).

Clock Source modes are selected by the FOSC<2:0> bits in the Configuration Word 1. The FOSC bits determine the type of oscillator that will be used when the device is first powered.

The EC clock mode relies on an external logic level signal as the device clock source. The LP, XT, and HS clock modes require an external crystal or resonator to be connected to the device. Each mode is optimized for a different frequency range. The RC clock mode requires an external resistor and capacitor to set the oscillator frequency.

The INTOSC internal oscillator block produces low, medium, and high frequency clock sources, designated LFINTOSC, MFINTOSC, and HFINTOSC. (see Internal Oscillator Block, Figure 5-1). A wide selection of device clock frequencies may be derived from these three clock sources.

EXAMPLE 11-2: DATA EEPROM WRITE

		BANKSEL	EEADRL	i
		MOVLW	DATA_EE_ADDR	;
		MOVWF	EEADRL	;Data Memory Address to write
		MOVLW	DATA_EE_DATA	i
		MOVWF	EEDATL	;Data Memory Value to write
		BCF	EECON1, CFGS	;Deselect Configuration space
		BCF	EECON1, EEPGD	;Point to DATA memory
		BSF	EECON1, WREN	;Enable writes
		BCF	INTCON, GIE	;Disable INTs.
ſ		MOVLW	55h	i
	ce ed	MOVWF	EECON2	;Write 55h
	huird	MOVLW	0AAh	i
	Sec	MOVWF	EECON2	;Write AAh
	ш 0	BSF	EECON1, WR	;Set WR bit to begin write
		BSF	INTCON, GIE	;Enable Interrupts
		BCF	EECON1, WREN	;Disable writes
		BTFSC	EECON1, WR	;Wait for write to complete
		GOTO	\$-2	;Done



	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4	Q1 Q2 Q3 Q4
Flash ADDR	 ()	PC + 1	EEADRH,EEADRL	PC + 3	PC + 4	PC + 5
Flash Data		I STR (PC) X INSTI	R (PC + 1) EEDA		R (PC + 3) INST	R (PC + 4)
	INSTR(PC - 1) executed here	BSF EECON1,RD executed here	INSTR(PC + 1) executed here	Forced NOP executed here	INSTR(PC + 3) executed here	INSTR(PC + 4) executed here
RD bit	 	 			 	
EEDATH EEDATL Register	 	 	 	X		
EERHLT	ı 	 	، ا			

11.3 Flash Program Memory Overview

It is important to understand the Flash program memory structure for erase and programming operations. Flash program memory is arranged in rows. A row consists of a fixed number of 14-bit program memory words. A row is the minimum block size that can be erased by user software.

Flash program memory may only be written or erased if the destination address is in a segment of memory that is not write-protected, as defined in bits WRT<1:0> of Configuration Word 2.

After a row has been erased, the user can reprogram all or a portion of this row. Data to be written into the program memory row is written to 14-bit wide data write latches. These write latches are not directly accessible to the user, but may be loaded via sequential writes to the EEDATH:EEDATL register pair.

Note:	If the user wants to modify only a portion
	of a previously programmed row, then the
	contents of the entire row must be read
	and saved in RAM prior to the erase.

The number of data write latches is not equivalent to the number of row locations. During programming, user software will need to fill the set of write latches and initiate a programming operation multiple times in order to fully reprogram an erased row. For example, a device with a row size of 32 words and eight write latches will need to load the write latches with data and initiate a programming operation four times.

The size of a program memory row and the number of program memory write latches may vary by device. See Table 11-1 for details.

TABLE 11-1:FLASH MEMORY
ORGANIZATION BY DEVICE

Device	Erase Block (Row) Size/ Boundary	Number of Write Latches/ Boundary
PIC16(L)F1824	32 words,	32 words,
PIC16(L)F1828	EEADRL<4:0>	EEADRL<4:0>
	= 00000	= 00000

11.3.1 READING THE FLASH PROGRAM MEMORY

To read a program memory location, the user must:

- 1. Write the Least and Most Significant address bits to the EEADRH:EEADRL register pair.
- 2. Clear the CFGS bit of the EECON1 register.
- 3. Set the EEPGD control bit of the EECON1 register.
- 4. Then, set control bit RD of the EECON1 register.

Once the read control bit is set, the program memory Flash controller will use the second instruction cycle to read the data. This causes the second instruction immediately following the "BSF EECON1, RD" instruction to be ignored. The data is available in the very next cycle, in the EEDATH:EEDATL register pair; therefore, it can be read as two bytes in the following instructions.

EEDATH:EEDATL register pair will hold this value until another read or until it is written to by the user.

- Note 1: The two instructions following a program memory read are required to be NOPS. This prevents the user from executing a two-cycle instruction on the next instruction after the RD bit is set.
 - 2: Flash program memory can be read regardless of the setting of the CP bit.





24.4.3 ENHANCED PWM AUTO-SHUTDOWN MODE

The PWM mode supports an Auto-Shutdown mode that will disable the PWM outputs when an external shutdown event occurs. Auto-Shutdown mode places the PWM output pins into a predetermined state. This mode is used to help prevent the PWM from damaging the application.

The auto-shutdown sources are selected using the CCPxAS<2:0> bits of the CCPxAS register. A shutdown event may be generated by:

- A logic '0' on the FLT0 pin
- A logic '1' on a Comparator (Cx) output

A shutdown condition is indicated by the CCPxASE (Auto-Shutdown Event Status) bit of the CCPxAS register. If the bit is a '0', the PWM pins are operating normally. If the bit is a '1', the PWM outputs are in the shutdown state.

When a shutdown event occurs, two things happen:

The CCPxASE bit is set to '1'. The CCPxASE will remain set until cleared in firmware or an auto-restart occurs (see **Section 24.4.4 "Auto-restart Mode"**).

The enabled PWM pins are asynchronously placed in their shutdown states. The PWM output pins are grouped into pairs [PxA/PxC] and [PxB/PxD]. The state of each pin pair is determined by the PSSxAC and PSSxBD bits of the CCPxAS register. Each pin pair may be placed into one of three states:

- Drive logic '1'
- Drive logic '0'
- Tri-state (high-impedance)

Note 1: The auto-shutdown condition is a levelbased signal, not an edge-based signal. As long as the level is present, the autoshutdown will persist.

- 2: Writing to the CCPxASE bit is disabled while an auto-shutdown condition persists.
- 3: Once the auto-shutdown condition has been removed and the PWM restarted (either through firmware or auto-restart) the PWM signal will always restart at the beginning of the next PWM period.
- 4: Prior to an auto-shutdown event caused by a comparator output or FLT0 pin event, a software shutdown can be triggered in firmware by setting the CCPxASE bit of the CCPxAS register to '1'. The Auto-Restart feature tracks the active status of a shutdown caused by a comparator output or FLT0 pin event only. If it is enabled at this time, it will immediately clear this bit and restart the ECCP module at the beginning of the next PWM period.







25.5.3 SLAVE TRANSMISSION

When the R/W bit of the incoming address byte is set and an address match occurs, the R/W bit of the SSP1STAT register is set. The received address is loaded into the SSP1BUF register, and an ACK pulse is sent by the slave on the ninth bit.

Following the ACK, slave hardware clears the CKP bit and the SCL pin is held low (see **Section 25.5.6** "**Clock Stretching**" for more detail). By stretching the clock, the master will be unable to assert another clock pulse until the slave is done preparing the transmit data.

The transmit data must be loaded into the SSP1BUF register which also loads the SSP1SR register. Then the SCL pin should be released by setting the CKP bit of the SSP1CON1 register. The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time.

The ACK pulse from the master-receiver is latched on the rising edge of the ninth SCL input pulse. This ACK value is copied to the ACKSTAT bit of the SSP1CON2 register. If ACKSTAT is set (not ACK), then the data transfer is complete. In this case, when the not ACK is latched by the slave, the slave goes idle and waits for another occurrence of the Start bit. If the SDA line was low (ACK), the next transmit data must be loaded into the SSP1BUF register. Again, the SCL pin must be released by setting bit CKP.

An MSSP1 interrupt is generated for each data transfer byte. The SSP1IF bit must be cleared by software and the SSP1STAT register is used to determine the status of the byte. The SSP1IF bit is set on the falling edge of the ninth clock pulse.

25.5.3.1 Slave Mode Bus Collision

A slave receives a read request and begins shifting data out on the SDA line. If a bus collision is detected and the SBCDE bit of the SSP1CON3 register is set, the BCL1IF bit of the PIRx register is set. Once a bus collision is detected, the slave goes Idle and waits to be addressed again. User software can use the BCL1IF bit to handle a slave bus collision.

25.5.3.2 7-bit Transmission

A master device can transmit a read request to a slave, and then clock data out of the slave. The list below outlines what software for a slave will need to do to accomplish a standard transmission. Figure 25-18 can be used as a reference to this list.

- 1. Master sends a Start condition on SDA and SCL.
- 2. S bit of SSP1STAT is set; SSP1IF is set if interrupt on Start detect is enabled.
- Matching address with R/W bit set is received by the Slave setting SSP1IF bit.
- 4. Slave hardware generates an ACK and sets SSP1IF.
- 5. SSP1IF bit is cleared by user.
- 6. Software reads the received address from SSP1BUF, clearing BF.
- 7. R/\overline{W} is set so CKP was automatically cleared after the ACK.
- 8. The slave software loads the transmit data into SSP1BUF.
- 9. CKP bit is set releasing SCL, allowing the master to clock the data out of the slave.
- 10. SSP1IF is set after the ACK response from the master is loaded into the ACKSTAT register.
- 11. SSP1IF bit is cleared.
- 12. The slave software checks the ACKSTAT bit to see if the master wants to clock out more data.
 - **Note 1:** If the master ACKs the clock will be stretched.
 - ACKSTAT is the only bit updated on the rising edge of SCL (9th) rather than the falling.
- 13. Steps 9-13 are repeated for each transmitted byte.
- 14. If the master sends a not ACK; the clock is not held, but SSP1IF is still set.
- 15. The master sends a Restart condition or a Stop.
- 16. The slave is no longer addressed.







Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
INLVLB ⁽¹⁾	INLVLB7	INLVLB6	INLVLB5	INLVLB4	_	_	_	_	128
INLVLC	INLVLC7 ⁽¹⁾	INLVLC6 ⁽¹⁾	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	134
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	89
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	90
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	_	_	CCP2IE	91
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	93
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	_	_	CCP2IF	94
SSP1ADD	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	284
SSP1BUF	Synchronous Serial Port Receive Buffer/Transmit Register						234*		
SSP1CON1	WCOL	SSPOV	SSPEN	СКР	SSPM<3:0>			281	
SSP1CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	282
SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	283
SSP1MSK	MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0	284
SSP1STAT	SMP	CKE	D/A	Р	S	R/W	UA	BF	280
TRISB ⁽¹⁾	TRISB7	TRISB6	TRISB5	TRISB4	_	_	_	_	127
TRISC ⁽²⁾	_	_	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	127

SUMMARY OF REGISTERS ASSOCIATED WITH I²C[™] OPERATION **TABLE 25-3:**

— = unimplemented location, read as '0'. Shaded cells are not used by the MSSP module in I²C™ mode. Page provides register information. PIC16(L)F1828 only. Legend:

1:

Note

2: Unshaded cells apply to PIC16(L)F1824 only.

26.1.2.8 Asynchronous Reception Setup:

- Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Section 26.3 "EUSART Baud Rate Generator (BRG)").
- 2. Clear the ANSEL bit for the RX pin (if applicable).
- Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
- 4. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 5. If 9-bit reception is desired, set the RX9 bit.
- 6. Enable reception by setting the CREN bit.
- 7. The RCIF interrupt flag bit will be set when a character is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
- 8. Read the RCSTA register to get the error flags and, if 9-bit data reception is enabled, the ninth data bit.
- 9. Get the received eight Least Significant data bits from the receive buffer by reading the RCREG register.
- 10. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.

26.1.2.9 9-bit Address Detection Mode Setup

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable:

- Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Section 26.3 "EUSART Baud Rate Generator (BRG)").
- 2. Clear the ANSEL bit for the RX pin (if applicable).
- Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
- 4. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 5. Enable 9-bit reception by setting the RX9 bit.
- 6. Enable address detection by setting the ADDEN bit.
- 7. Enable reception by setting the CREN bit.
- The RCIF interrupt flag bit will be set when a character with the ninth bit set is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
- 9. Read the RCSTA register to get the error flags. The ninth data bit will always be set.
- 10. Get the received eight Least Significant data bits from the receive buffer by reading the RCREG register. Software determines if this is the device's address.
- 11. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.
- 12. If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and generate interrupts.



FIGURE 26-5: ASYNCHRONOUS RECEPTION

26.3.2 AUTO-BAUD OVERFLOW

During the course of automatic baud detection, the ABDOVF bit of the BAUDCON register will be set if the baud rate counter overflows before the fifth rising edge is detected on the RX pin. The ABDOVF bit indicates that the counter has exceeded the maximum count that can fit in the 16 bits of the SPBRGH:SPBRGL register pair. After the ABDOVF has been set, the counter continues to count until the fifth rising edge is detected on the RX pin. Upon detecting the fifth RX edge, the hardware will set the RCIF interrupt flag and clear the ABDEN bit of the BAUDCON register. The RCIF flag can be subsequently cleared by reading the RCREG register. The ABDOVF flag of the BAUDCON register can be cleared by software directly.

To terminate the auto-baud process before the RCIF flag is set, clear the ABDEN bit then clear the ABDOVF bit of the BAUDCON register. The ABDOVF bit will remain set if the ABDEN bit is not cleared first.

26.3.3 AUTO-WAKE-UP ON BREAK

During Sleep mode, all clocks to the EUSART are suspended. Because of this, the Baud Rate Generator is inactive and a proper character reception cannot be performed. The Auto-Wake-up feature allows the controller to wake-up due to activity on the RX/DT line. This feature is available only in Asynchronous mode.

The Auto-Wake-up feature is enabled by setting the WUE bit of the BAUDCON register. Once set, the normal receive sequence on RX/DT is disabled, and the EUSART remains in an Idle state, monitoring for a wake-up event independent of the CPU mode. A wake-up event consists of a high-to-low transition on the RX/DT line. (This coincides with the start of a Sync Break or a wake-up signal character for the LIN protocol.)

The EUSART module generates an RCIF interrupt coincident with the wake-up event. The interrupt is generated synchronously to the Q clocks in normal CPU operating modes (Figure 26-7), and asynchronously if the device is in Sleep mode (Figure 26-8). The interrupt condition is cleared by reading the RCREG register.

The WUE bit is automatically cleared by the low-to-high transition on the RX line at the end of the Break. This signals to the user that the Break event is over. At this point, the EUSART module is in Idle mode waiting to receive the next character.

26.3.3.1 Special Considerations

Break Character

To avoid character errors or character fragments during a wake-up event, the wake-up character must be all zeros.

When the wake-up is enabled the function works independent of the low time on the data stream. If the WUE bit is set and a valid non-zero character is received, the low time from the Start bit to the first rising edge will be interpreted as the wake-up event. The remaining bits in the character will be received as a fragmented character and subsequent characters can result in framing or overrun errors.

Therefore, the initial character in the transmission must be all '0's. This must be ten or more bit times, 13-bit times recommended for LIN bus, or any number of bit times for standard RS-232 devices.

Oscillator Startup Time

Oscillator start-up time must be considered, especially in applications using oscillators with longer start-up intervals (i.e., LP, XT or HS/PLL mode). The Sync Break (or wake-up signal) character must be of sufficient length, and be followed by a sufficient interval, to allow enough time for the selected oscillator to start and provide proper initialization of the EUSART.

WUE Bit

The wake-up event causes a receive interrupt by setting the RCIF bit. The WUE bit is cleared in hardware by a rising edge on RX/DT. The interrupt condition is then cleared in software by reading the RCREG register and discarding its contents.

To ensure that no actual data is lost, check the RCIDL bit to verify that a receive operation is not in process before setting the WUE bit. If a receive operation is not occurring, the WUE bit may then be set just prior to entering the Sleep mode.

28.0 IN-CIRCUIT SERIAL PROGRAMMING[™] (ICSP[™])

ICSP[™] programming allows customers to manufacture circuit boards with unprogrammed devices. Programming can be done after the assembly process allowing the device to be programmed with the most recent firmware or a custom firmware. Five pins are needed for ICSP[™] programming:

- ICSPCLK
- ICSPDAT
- MCLR/VPP
- VDD
- Vss

In Program/Verify mode the Program Memory, User IDs and the Configuration Words are programmed through serial communications. The ICSPDAT pin is a bidirectional I/O used for transferring the serial data and the ICSPCLK pin is the clock input. For more information on ICSP[™] refer to the "*PIC16F/LF182X/PIC12F/LF1822 Memory Programming Specification*" (DS41390).

28.1 High-Voltage Programming Entry Mode

The device is placed into High-Voltage Programming Entry mode by holding the ICSPCLK and ICSPDAT pins low then raising the voltage on MCLR/VPP to VIHH.

Some programmers produce VPP greater than VIHH (9.0V), an external circuit is required to limit the VPP voltage. See Figure 28-1 for example circuit.



FIGURE 28-1: VPP LIMITER EXAMPLE CIRCUIT

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RETFIE	Return from Interrupt				
Syntax:	[label] RETFIE				
Operands:	None				
Operation:	$\begin{array}{l} TOS \to PC, \\ 1 \to GIE \end{array}$				
Status Affected:	None				
Description:	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a 2-cycle instruction.				
Words:	1				
Cycles:	2				
Example:	RETFIE				
	After Interrupt PC = TOS GIE = 1				

RETURN	Return from Subroutine				
Syntax:	[label] RETURN				
Operands:	None				
Operation:	$TOS \rightarrow PC$				
Status Affected:	None				
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a 2-cycle instruction.				

RETLW	Return with literal in W		Pototo Loft f through Corry			
Syntax:	[<i>label</i>] RETLW k	RLF				
Operands:	$0 \le k \le 255$	Syntax:	[<i>label</i>] RLF f,d			
Operation:	$k \rightarrow (W);$ TOS \rightarrow PC	Operands:	$0 \le f \le 127$ $d \in [0,1]$ See description below			
Status Affected	None	Operation:				
	The W register is leaded with the 9 hit	Status Affected: C				
Description.	literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.	Description:	The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.			
Words:	1					
Cycles:	2					
Example:	CALL TABLE;W contains table	Words:	1			
	;offset value . :W now has table value	Cycles:	1			
TABLE	•	Example:	RLF REG1,0			
	• ADDWF PC ;W = offset RETLW k1 ;Begin table RETLW k2 ; • • RETLW kn ; End of table		Before Instruction REG1 = 1110 0110 C = 0 - - After Instruction REG1 = 1110 0110 W = 1100 1100 - C = 1 - -			
	Before Instruction W = 0x07 After Instruction W = value of k8					

PIC16LF	1824/8	$\begin{tabular}{lllllllllllllllllllllllllllllllllll$									
PIC16F1824/8				$\begin{tabular}{lllllllllllllllllllllllllllllllllll$							
Param. No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions				
D001	Vdd	Supply Voltage (VDDMIN, VDDMAX)									
		PIC16LF1824/8	1.8 2.5		3.6 3.6	V V	Fosc ≤ 16 MHz: Fosc ≤ 32 MHz (Note 2)				
D001		PIC16F1824/8	1.8 2.5	_	5.5 5.5	V V	Fosc ≤ 16 MHz: Fosc ≤ 32 MHz (Note 2)				
D002*	Vdr	RAM Data Retention Voltage ⁽¹⁾									
		PIC16LF1824/8	1.5	-	_	V	Device in Sleep mode				
D002*		PIC16F1824/8	1.7	—	—	V	Device in Sleep mode				
D002A*	VPOR	Power-on Reset Release Voltage	_	1.6	_	V					
D002B*	VPORR	Power-on Reset Rearm Voltage									
		PIC16LF1824/8	—	0.8	—	V	Device in Sleep mode				
D002B*		PIC16F1824/8	—	1.4	—	V	Device in Sleep mode				
D003	VADFVR	Fixed Voltage Reference Voltage for ADC	-8	_	6	%	1.024V, VDD ≥ 2.5V 2.048V, VDD ≥ 2.5V 4.096V, VDD ≥ 4.75V				
D003A	VCDAFVR	Fixed Voltage Reference Voltage for Comparator and DAC	-11	—	7	%	$\begin{array}{l} 1.024V, \ VDD \geq 2.5V\\ 2.048V, \ VDD \geq 2.5V\\ 4.096V, \ VDD \geq 4.75V \end{array}$				
D004*	SVDD	VDD Rise Rate to ensure internal Power-on Reset signal	0.05	—	_	V/ms	See Section 7.1 "Power-on Reset (POR)" for details.				

30.1 DC Characteristics: PIC16(L)F1824/8-I/E (Industrial, Extended)

These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

2: PLL required for 32 MHz operation.

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$							
Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions			
		Program Memory High Voltage Programming Specifications								
D110	VIHH	Voltage on MCLR/VPP/RA5 pin	8.0	—	9.0	V	(Note 3, 4)			
D111	IDDVPP	Programming/Erase Current on VPP, High Voltage Programming	—	—	10	mA				
D112	VBE	VDD for Bulk Erase	2.7	—	VDDMAX	V				
D113	VPEW	VDD for Write or Row Erase	VDDMIN	_	VDDMAX	V				
D114	IPPPGM	Programming/Erase Current on VPP, Low Voltage Programming	—	1.0	—	mA				
D115	IDDPGM	Programming/Erase Current on VDD, High or Low Voltage Programming	—	5.0	—	mA				
		Data EEPROM Memory								
D116	ED	Byte Endurance	100K	—	—	E/W	-40°C to +85°C			
D117	Vdrw	VDD for Read/Write	VDDMIN	—	VDDMAX	V				
D118	TDEW	Erase/Write Cycle Time	—	4.0	5.0	ms				
D119	TRETD	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated			
D120	TREF	Number of Total Erase/Write Cycles before Refresh ⁽²⁾	1M	10M	—	E/W	-40°C to +85°C			
		Program Flash Memory								
D121	Eр	Cell Endurance	10K	_	_	E/W	-40°C to +85°C (Note 1)			
D122	VPRW	VDD for Read/Write	VDDMIN	—	VDDMAX	V				
D123	Tiw	Self-timed Write Cycle Time	—	2	2.5	ms				
D124	TRETD	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated			

30.5 Memory Programming Requirements

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Self-write and Block Erase.

2: Refer to Section 11.2 "Using the Data EEPROM" for a more detailed discussion on data EEPROM endurance.

3: Required only if single-supply programming is disabled.

4: The MPLAB[®] ICD 2 does not support variable VPP output. Circuitry to limit the ICD 2 VPP voltage must be placed between the ICD 2 and target system when programming or debugging with the ICD 2.







FIGURE 31-6: IDD MAXIMUM, XT AND EXTRC OSCILLATOR, PIC16F1824/8 ONLY



FIGURE 31-12: IDD, LFINTOSC MODE (Fosc = 31 kHz), PIC16F1824/8 ONLY

